

Charge trapping and retention behaviors of Ge nanocrystals distributed in the gate oxide near the gate synthesized by low-energy ion implantation

M. Yang, T. P. Chen,^{a)} J. I. Wong, C. Y. Ng, Y. Liu, and L. Ding
*School of Electrical and Electronic Engineering, Nanyang Technological University,
 Singapore 639798, Singapore*

S. Fung
Physics Department, The University of Hong Kong, Hong Kong

A. D. Trigg and C. H. Tung
Institute of Microelectronics, 11 Science Park Road, Singapore 117685, Singapore

C. M. Li
*School of Chemical and Biomedical Engineering, Nanyang Technological University,
 Singapore 639798, Singapore*

(Received 28 February 2007; accepted 16 May 2007; published online 27 June 2007)

A layer of Ge nanocrystals (nc-Ge) distributed in the gate oxide near the gate of a metal-oxide-semiconductor structure is synthesized with low-energy Ge ion implantation followed by thermal annealing at 800 °C. The behaviors of charge trapping and charge retention in the nc-Ge have been studied. For a positive charging voltage, only electron trapping occurs, and the trapped electrons show a long retention time. However, for a negative charging voltage, both the hole trapping and electron trapping occur simultaneously, and the hole trapping is dominant if the magnitude of the charging voltage is small or the charging time is short. Due to the relatively easier loss of the trapped holes, the net charge trapping in the nc-Ge exhibits a continuous shift toward a more negative value with the waiting time. © 2007 American Institute of Physics.

[DOI: [10.1063/1.2749470](https://doi.org/10.1063/1.2749470)]

I. INTRODUCTION

Si and Ge nanocrystals have a promising application in nonvolatile memory (NVM) devices.^{1–5} Although many works have been devoted to Si nanocrystal (nc-Si), Ge nanocrystal (nc-Ge) was believed to have a better performance due to its smaller band gap.^{4,5} The nc-Ge embedded in a SiO₂ layer can be fabricated with various techniques such as wet oxidation of Si_{1-x}Ge_x film,⁴ chemical vapor deposition,^{5,6} cosputtering,⁷ and ion implantation.^{8,9} In a NVM device based on the nc-Ge, the structure of gate/control oxide/nc-Ge layer/tunnel oxide/Si substrate is usually formed with the nc-Ge layer located near the Si substrate.^{5,10,11} In the present study, the above structure is simplified by using a single low-energy ion implantation into a SiO₂ thin film and eliminating the deposition of the control oxide. In this simplified structure, the nc-Ge is distributed in a narrow layer in the gate oxide near the gate rather than the substrate. The simplified structure shows the memory effect and exhibits some interesting behaviors of charge trapping and retention. It is observed that both electrons and holes can be stored in the nc-Ge depending on the polarity and magnitude of the charging voltage as well as the charging time. It is also observed that the electron storage has a much longer retention time as compared to the hole storage.

II. EXPERIMENTAL DETAILS

The fabrication of the metal-oxide-semiconductor (MOS) structure with the nc-Ge distributed near the gate in the gate oxide began with the growth of a 32 nm SiO₂ thin film on the *p*-type Si substrate at 950 °C by dry oxidation. Subsequently, Ge ions were implanted into the SiO₂ film with a dosage of 1×10^{16} cm⁻² at the energy of 4 keV. According to the stopping and range of ions in matter (SRIM) simulation, a Gaussian distribution (range=7.7 nm and straggle=2.2 nm) of Ge ions in the SiO₂ film with the peak (the peak concentration is 1.1×10^{22} at./cm³) located near the SiO₂ surface was obtained. The implanted samples were then annealed at 800 °C in N₂ ambient for 40 min to induce the formation of nc-Ge. Cross-sectional transmission electron microscopy (TEM) was used to reveal the structural information of the annealed samples. Aluminum was deposited and patterned to form the top and bottom electrodes. At the same time, a control sample without Ge ion implantation was also prepared under identical conditions. To investigate the behaviors of charge trapping and retention in the nc-Ge, the charging experiment and the capacitance-voltage (*C-V*) measurement were performed in a dark environment at room temperature with a Keithley 4200 semiconductor characterization system and a HP 4284A LCR meter.

III. RESULTS AND DISCUSSIONS

Figure 1 shows the TEM image for the sample with the nc-Ge distributed in the SiO₂ thin film. The inset of Fig. 1

^{a)}Electronic mail: echentp@ntu.edu.sg

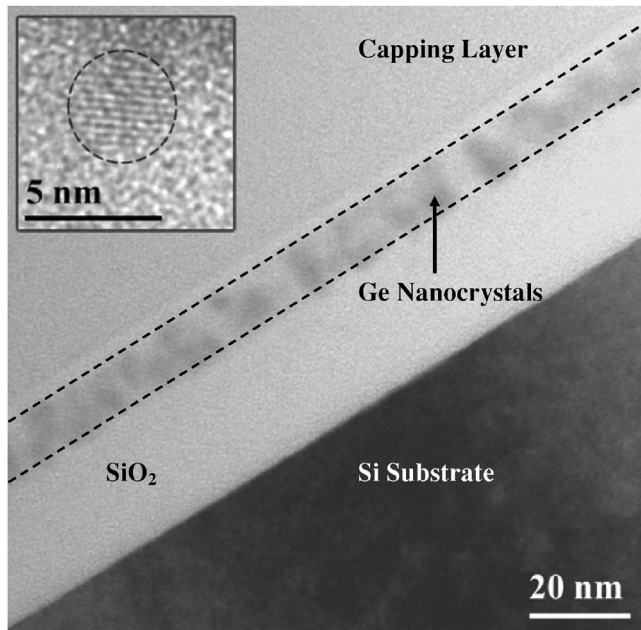


FIG. 1. Cross-sectional TEM image showing a narrow layer of nc-Ge located in the surface region of the SiO₂ thin film. The inset shows the TEM image of a single nc-Ge.

shows the TEM image of a single nc-Ge with a size of about 4 nm. A narrow layer of nc-Ge near the surface of the SiO₂ film is clearly observed. The width of the nc-Ge layer is about 10.5 nm, the oxide thickness between the nc-Ge layer and the Si substrate is about 25 nm, and the oxide thickness between the surface of the SiO₂ film and the nc-Ge layer is about 4 nm. The total thickness of the SiO₂ film containing the nc-Ge is 39.5 nm, which is about 20% larger than the thickness of the unimplanted oxide. This observation consists with the previous studies in which the oxide swellings with an increase by ~20%–80% in the oxide thickness after ion implantation and annealing were observed.^{9,12,13} The oxide swelling could be due to various reasons such as the additional spaces occupied by the implanting species and the annealing effect.¹²

The charging behaviors of the nc-Ge are studied by examining the shifts in the *C-V* characteristic after the application of a constant charging voltage (V_G) to the gate electrode. Figure 2 shows the typical *C-V* shifts for the charging voltages of +25 and –25 V and the charging time of 1 s. A clear flatband voltage shift (ΔV_{fb}) with respect to the virgin *C-V* curve indicates the memory effect of the device structure. It is interesting to notice that both of the charging voltages (i.e., +25 and –25 V) cause a shift in the flatband voltage toward the positive side, suggesting that both of them lead to a buildup of negative charges in the thin film structure. Since no ΔV_{fb} can be observed for the control sample without the nc-Ge, the positive shift in the flatband voltage is attributed to the trapping of electrons in the nc-Ge distributed in the SiO₂ film. The ΔV_{fb} is related to the density of charges trapped in the nc-Ge by¹

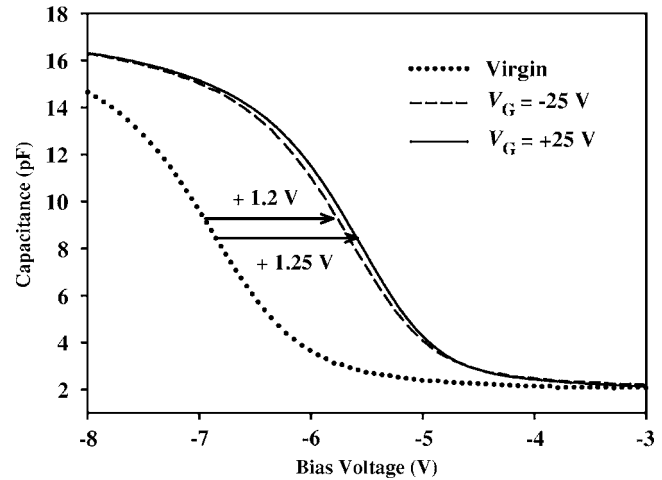


FIG. 2. Shifts in the high-frequency (1 MHz) *C-V* characteristics after the charging at $V_G = +25$ or –25 V for 1 s.

$$\Delta V_{fb} = -\frac{Q_{\text{charge}}}{\epsilon_{\text{SiO}_2}} \left(t_g + \frac{1}{2} \frac{\epsilon_{\text{SiO}_2}}{\epsilon_{\text{Ge}}} d_{\text{nc-Ge}} \right), \quad (1)$$

where Q_{charge} is the density of the charges trapped in the nc-Ge, ϵ_{SiO_2} and ϵ_{Ge} represent the permittivity of the SiO₂ and Ge, respectively, t_g is the oxide thickness between the gate electrode and the nc-Ge layer, and $d_{\text{nc-Ge}}$ is the dimension of the nc-Ge. Note that the negative sign in Eq. (1) accounts for the fact that the trapping of negative charges in the nc-Ge leads to a positive ΔV_{fb} . As examples, the Q_{charge} estimated with Eq. (1) are -9.62×10^{-7} and -9.23×10^{-7} C/cm² for $V_G = +25$ and –25 V, respectively.

To study the influence of both the polarity and magnitude of the charging voltage on the charge trapping in the nc-Ge, the Q_{charge} was measured for both positive and negative V_G with a magnitude varying from 7 to 30 V at the fixed charging time of 1 s. The results are shown in Fig. 3. It is evident from Fig. 3 that the charging behavior for positive V_G is different from that for negative V_G . As shown in the figure, a positive charging voltage always results in a negative Q_{charge} regardless of the voltage magnitude. In contrast, a negative charging voltage leads to either a positive or a negative Q_{charge} depending on the magnitude of the voltage. In the case of positive V_G , for V_G less than +21 V, the Q_{charge} remains at a small negative value with a magnitude less than 1×10^{-7} C/cm², indicating that only a small amount of electrons are trapped in the nc-Ge. However, when the V_G goes beyond +21 V, the Q_{charge} is still negative, but its magnitude increases rapidly (for example, $Q_{\text{charge}} = -27 \times 10^{-7}$ C/cm² for $V_G = +30$ V) and is approximately a linear function of the V_G . As will be discussed later, the rapid increase in the magnitude of Q_{charge} is due to the strong electron injection from the Si substrate under the influence of a large positive gate voltage. On the other hand, in the case of negative V_G , the Q_{charge} is positive when the magnitude of V_G is less than 19 V, and the maximum Q_{charge} (3.2×10^{-7} C/cm²) occurs at $V_G = -16$ V. When the magnitude of V_G is larger than 19 V, the Q_{charge} becomes negative and its magnitude rapidly increases as the magnitude of the V_G is further increased. It is obvious that in the case of negative V_G both hole trapping

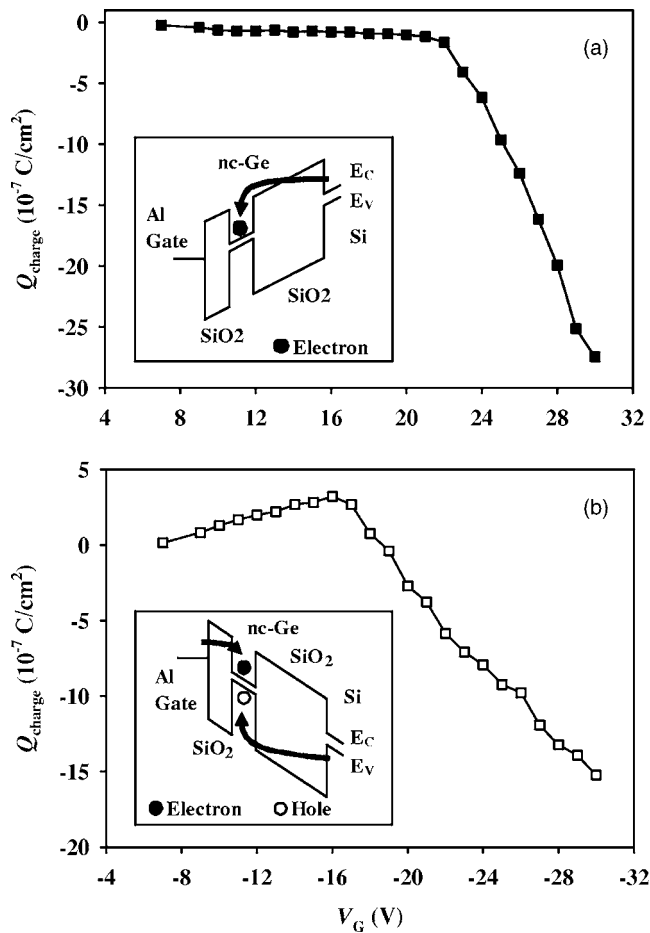


FIG. 3. Density (Q_{charge}) of trapped charges as a function of the charging voltage (V_G): (a) positive charging voltage and (b) negative charging voltage. The charging time is fixed at 1 s. The insets show the charging mechanisms under a positive or negative V_G .

and electron trapping in the nc-Ge occur. As will be discussed later, under a negative V_G , the hole trapping and electron trapping are two competing processes, and the magnitude of the V_G determines which one is dominant. This behavior is different from the situation of a conventional memory structure where the nc-Ge layer is located near the Si substrate.⁹ In a conventional structure, the electron trapping caused by a negative V_G is insignificant because the thick control oxide prevents the electron injection from the gate.

The results shown in Fig. 3 indicate that the positive V_G results in only electron trapping, whereas the negative V_G leads to both electron trapping and hole trapping simultaneously. As shown in the inset of Fig. 3(a), under the influence of a positive V_G , electrons are injected from the Si substrate and trapped in the nc-Ge. When the magnitude of V_G is larger than 21 V, the electric field in the oxide between the Si substrate and the nc-Ge layer is higher than 5 MV/cm, leading to the occurrence of Fowler-Nordheim (FN) tunneling across the oxide. Therefore, the electron injection is drastically enhanced, resulting in a rapid increase in the electron trapping in the nc-Ge. On the other hand, as shown in the inset of Fig. 3(b), under the influence of a negative V_G , the injection of the holes from the Si substrate and the injection of electrons from the gate occur at the same time, leading to

the trapping of both holes and electrons in the nc-Ge. In this case, the density of the net trapped charges in the nc-Ge is given by

$$Q_{\text{charge}} = Q_{\text{hole}} - Q_{\text{electron}}, \quad (2)$$

where the Q_{hole} and Q_{electron} are the trapped-hole density and trapped-electron density, respectively. The behavior shown in Fig. 3(b) is a consequence of the competition between these two charging processes. Obviously, Q_{charge} is positive if the hole trapping dominates, and it is negative if the electron trapping dominates. Figure. 3(b) indicates that in the case of a negative V_G , when its magnitude is less than 18 V, the hole trapping is dominant, but the electron trapping increases rapidly when the magnitude of V_G is larger than 16 V. The rapid increase of the electron trapping is due to the occurrence of electron tunneling from the gate electrode. When the magnitude of the negative V_G is larger than 18 V, the electron tunneling from the gate surpasses the hole injection from the substrate, leading to a net negative charge trapping in the nc-Ge. This situation is in contrast to that of a conventional memory device where the nc-Ge is located near the substrate. For the conventional memory device, a negative V_G is usually used during the erasing process to expel the trapped electrons from the nc-Ge, and the negative V_G itself does not cause the electron trapping in the nc-Ge because of the thick control oxide which can effectively suppress the electron tunneling from the gate (note that only the trapping of positive charges in the nc-Ge is observable in the case of over-erasing).

Further investigation on the charging mechanisms is carried out by varying the charging time from 5 μs to 5 s for a given V_G , and the result is shown in Fig. 4. The result consists with the above-mentioned charging mechanisms. As shown in Fig. 4(a), the Q_{charge} is always negative regardless of the charging time for a positive V_G . This is because only electron injection from the substrate occurs under a positive V_G . It can be observed in Fig. 4(a) that for the $V_G = +25$ V, the electron trapping in the nc-Ge starts to increase rapidly when the charging time is longer than 1 ms. This starting time is prolonged when the V_G is reduced. Obviously, this is related to the V_G dependence of the electron injection from the substrate. On the other hand, as shown in Fig. 4(b), for the charging by a negative V_G , both positive and negative Q_{charge} could be observed depending on the magnitude of the V_G and the charging time. As discussed earlier, under a negative V_G , the two competing processes (i.e., the hole injection from the substrate and the electron injection from the gate) occur simultaneously. For $V_G = -15$ and -18 V, the Q_{charge} is positive (i.e., the hole trapping is dominant) and increases gently with the charging time. The increase of the Q_{charge} with the charging time for $V_G = -15$ V is even faster than that for $V_G = -18$ V. This is because the electron injection under $V_G = -15$ V is less significant. For $V_G = -20$ V, a small amount of positive charge trapping could be observed for a charging time shorter than 1 ms, but the electron trapping becomes dominant when the charging time is longer than 1 ms. For $V_G = -23$ and -25 V, the electron trapping is dominant, and the amount of the Q_{charge} increases with the charging time. When the charging time is longer than 1 s, the

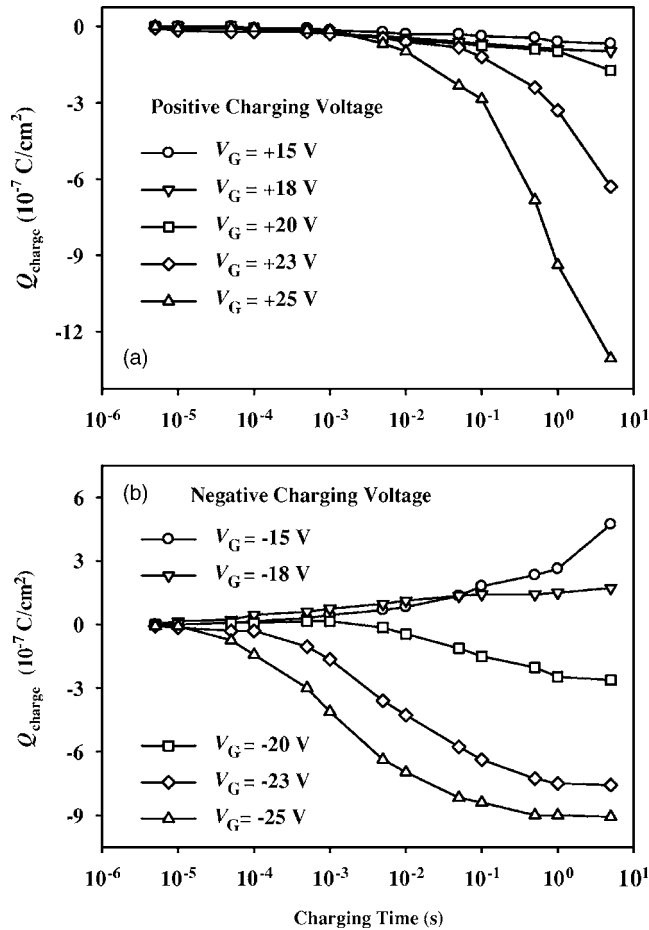


FIG. 4. Density (Q_{charge}) of trapped charges as a function of the charging time for different charging voltages (V_G): (a) positive charging voltages and (b) negative charging voltages.

electron trapping is saturated. Such phenomenon is due to the strong Coulomb interaction between the trapped electrons in the nc-Ge and the negatively biased gate electrode (note that the nc-Ge layer is close to the gate electrode).

The difference in charging process between positive and negative V_G has an impact on the charge retention. The charge retention characteristics of the memory structure are shown in Fig. 5. The charge retention experiment was carried out for both positive V_G [Fig. 5(a)] and negative V_G [Fig. 5(b)] with a fixed charging time of 1 s. For the charging under a positive V_G , as discussed above, only electrons are trapped in the nc-Ge, and thus the Q_{charge} behavior in the charge retention experiment is simple, i.e., the Q_{charge} remains negative and a decrease in its magnitude could be observed. As can be seen in Fig. 5(a), for both the charging voltages of +18 and +25 V, the Q_{charge} remains unchanged for the waiting time up to 10^4 s, and then only a slight loss of the trapped electrons is observed. The result indicates that the two oxide layers sandwiching the nc-Ge layer, as shown in the inset of Fig. 5(a), have a good capability to prevent the release of the trapped electrons. However, the charge retention behavior for a negative charging voltage is quite different. As shown in Fig. 5(b), for the $V_G = -18 \text{ V}$, the Q_{charge} is positive when the waiting time is shorter than 10^3 s, but later it becomes negative and shifts continuously toward a more

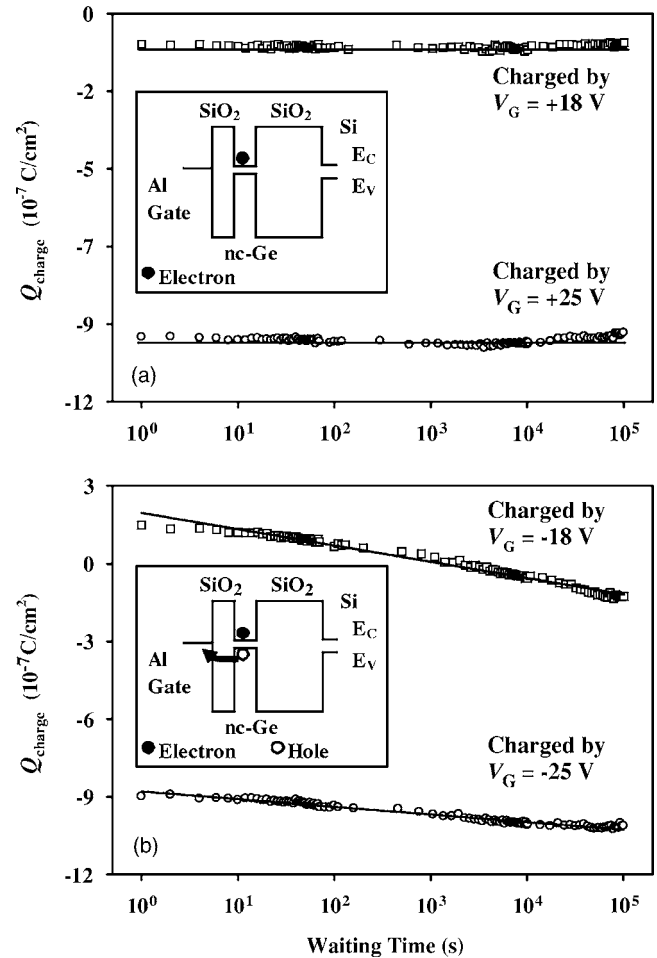


FIG. 5. Charge retention characteristics for (a) positive charging voltages and (b) negative charging voltages. The charging time is fixed at 1 s. The insets show the energy band diagrams during the retention experiment.

negative value (i.e., its magnitude increases) with the waiting time. For the $V_G = -25 \text{ V}$, the Q_{charge} is always negative regardless of the waiting time, and it also shifts continuously toward a more negative value with the waiting time. However, the rate of the change in Q_{charge} for $V_G = -25 \text{ V}$ is lower than that for $V_G = -18 \text{ V}$. As discussed earlier, both electrons and holes are trapped in the nc-Ge under a negative charging voltage. However, the above results indicate that the loss of the trapped holes is much faster than that of the trapped electrons. Therefore, with the faster loss of the trapped holes, the Q_{charge} can change from positive to negative as observed in the case of charging by $V_G = -18 \text{ V}$, and it shifts continuously toward a more negative value with time. As the hole trapping for $V_G = -18 \text{ V}$ is more significant than that for $V_G = -25 \text{ V}$, the rate of the change in Q_{charge} for $V_G = -18 \text{ V}$ is larger than that for $V_G = -25 \text{ V}$ as mentioned above. The faster loss of the trapped holes could be due to the fact that the trapped holes can easily recombine with the electrons moving from the Al gate electrode.

IV. CONCLUSION

In summary, we have synthesized a narrow layer of nc-Ge located near the gate in the gate oxide of the MOS structure using the low-energy Ge ion implantation and the

thermal annealing at 800 °C. The charge trapping and charge retention in the nc-Ge have been studied. For a positive charging voltage (V_G), only electron trapping occurs, which is due to the electron injection from the p -type substrate. The electron trapping depends strongly on the magnitude of the V_G and the charging time. It increases rapidly with the V_G when the FN tunneling across the oxide between the nc-Ge layer and the substrate occurs. However, for a negative V_G , both the hole trapping due to the hole injection from the substrate and the electron trapping due to the electron injection from the gate occur, and these two competing mechanisms determine whether the net charge trapping in the nc-Ge is positive or negative. The hole trapping could be dominant if the magnitude of V_G is small and the charging time is short, and the electron trapping becomes dominant when the magnitude of V_G is large and the charging time is sufficiently long. For a positive V_G , the electron trapping shows good retention. In contrast, for a negative V_G , due to the easier loss of the trapped holes, the net charge trapping in the nc-Ge shows a continuous shift toward a more negative value with the waiting time, and the shift strongly depends on the magnitude of the V_G and the charging time.

ACKNOWLEDGMENTS

This work has been financially supported by the Ministry of Education Singapore under Project No. ARC 1/04.

- ¹S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbé, and K. Chan, *Appl. Phys. Lett.* **68**, 1377 (1996).
- ²H. I. Hanafi, S. Tiwari, and I. Khan, *IEEE Trans. Electron Devices* **43**, 1553 (1996).
- ³C. Y. Ng, T. P. Chen, L. Ding, and S. Fung, *IEEE Electron Device Lett.* **27**, 231 (2006).
- ⁴Y. C. King, T. J. King, and C. Hu, *IEEE Trans. Electron Devices* **48**, 696 (2001).
- ⁵M. Kanoun, C. Buseret, A. Poncet, A. Souifi, T. Baron, and E. Gautier, *Solid-State Electron.* **50**, 1310 (2006).
- ⁶T. Baron, B. Pelissier, L. Perniola, F. Mazen, J. M. Hartmann, and G. Rolland, *Appl. Phys. Lett.* **83**, 1444 (2003).
- ⁷W. K. Choi, V. Ng, S. P. Ng, H. H. Thio, Z. X. Shen, and W. S. Li, *J. Appl. Phys.* **86**, 1398 (1999).
- ⁸J. Y. Zhang, X. M. Bao, and Y. H. Ye, *Thin Solid Films* **323**, 68 (1998).
- ⁹S. Duguay, J. J. Grob, A. Slaoui, Y. Le Gall, and M. Amann-Liess, *J. Appl. Phys.* **97**, 104330 (2005).
- ¹⁰K. Das *et al.*, *Appl. Phys. Lett.* **84**, 1386 (2004).
- ¹¹A. Kanjilal *et al.*, *Appl. Phys. Lett.* **82**, 1212 (2003).
- ¹²P. Normand *et al.*, *Appl. Phys. Lett.* **83**, 168 (2003).
- ¹³P. Normand, D. Tsoukalas, E. Kapetanakis, J. A. Van Den Berg, D. G. Armour, J. Stoemenos, and C. Vieud, *Electrochem. Solid-State Lett.* **1**, 88 (1998).