A Diagrammatic Approach to Search for Minimum Sampling Frequency and Quantization Resolution for Digital Control of Power Converters

C. W. Fung*, *Student Member, IEEE*, C. P. Liu, *Member, IEEE*, M. H. Pong*, *Senior Member, IEEE*
*Department of Electrical and Electronic Engineering, The University of Hong Kong

***Abstract* — A diagrammatic approach to find out the minimum sampling frequency and quantization resolution for digital control of power converters is proposed. The proposed solution algorithm combines consideration on both time sampling and quantization resolution axes to search for the minimum required digital controller settings. Experiments results are presented to justify the proposed algorithm.**

***Index Terms* — Digital Control, Switching Converter, Sampling, Quantization Resolution**

I. INTRODUCTION

Digital control offers many advantages to switching power converters such as immunity to noise and component variations, fast design process and easy to implement control algorithms [8-12]. However, due to the high cost of DSP, applications are limited to high power applications like motor drives and expensive systems. Applications of digital controller to low cost, mass produced ACDC power converters is still very limited. In order to make digital control practical to mass produced power supply products it is important to find out the minimum configuration required for a digital power supply in order to minimizes microcontroller cost.

There are researches on time-sampling and quantization resolution requirement for digital power converters [1-5]. However, none of them combine considerations of both sampling rate and quantization resolution simultaneously. It is promising that this dual consideration will lead to a minimum digital power converter controller configuration.

This paper provides a diagrammatic method to find out a minimum requirement of digital controller with considerations on both time sampling and quantization resolution dimensions. A solution algorithm to minimize both sampling rate and quantization resolution is also presented in this paper. MATLAB based software is developed to carry out this method by computers. Experimental result verifies this method.

II. BACKGROUND

Unlike conventional analog controllers, digital controllers can be highly nonlinear. Nonlinear effects of digital power converter are not desired because they would introduce loop instability and oscillations in the converter. Digital controller for power converters has two nonlinear effects: quantization and modulation effects [1-4].

Here quantization refers to the discretion of the desired output and the accuracy is governed by the number of bits used [3,4,7]. For example, the waveform shown in black in Fig. 1 will be generated instead of the grey one when the system is subject to a quantization resolution shown in dotted line.

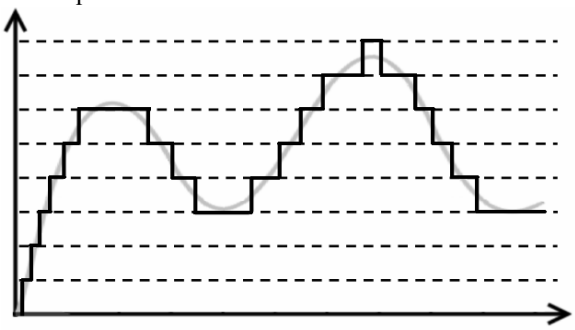


Fig. 1 Quantization Effect

Modulation effect is discretion effect on the time axis which is governed by the sampling frequency and computation speed [1,2,5]. Fig. 2 shows a grey analogue waveform sampled to become a quantized and distorted waveform.

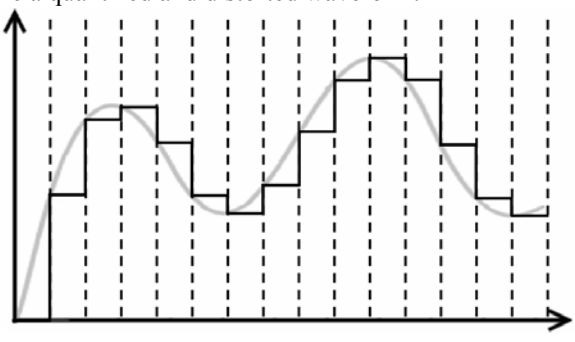


Fig. 2 Modulation Effect

It is our aim to find out the minimum requirement in terms of these two effects for digital controlled power converters.

III. Effects of Quantization and Modulation on Digital Controlled Power Converter

A. Resolution of A/D converter and Digital PWM Generator

Researchers pointed out that to satisfy specifications for the output voltage regulation, resolution of the A/D converters have to have error lower than the allowed variation of the output voltage [1,3,4,7]. Insufficient A/D resolution would lead to undesired steady state error in output voltage. For example, for an A/D converter with resolution of 0.1V, it is impossible for it to distinguish a 5.00V from 5.04V. Microprocessor cannot react to small errors in the controlled voltage until the error is accumulated higher than half of the quantization resolution.

The minimum required resolution for A/D converter [1] can be calculated by the following equation:

$$\text{A/D Resolution} = \text{int}\left[\frac{\text{Full Range A/D Voltage}}{\text{Reference Voltage}} \times \frac{\text{Output Voltage}}{\text{Output Voltage Variation}}\right]$$

Due to limited resolution of the Digital PWM Generator, only a set of duty cycles can be generated. Oscillation between different duty levels, so known as limit cycle oscillation [4,7,13,14], would be observed if D/A resolution is not enough. This would produce output ripples in steady state which may exceed the allowed voltage variation. The minimum resolution required for DPWM depends on steady-state operating conditions in the circuit and the A/D resolution.

The minimum required resolution for digital PWM generator [1] can be calculated by the following equation:

$$\text{Digital PWM Resolution} = \text{int}\left[\text{ADC Resolution} + \ln\left(\frac{\text{Reference Voltage}}{\text{Full Range A/D Voltage} \times \text{Duty}}\right)\right]$$

B. Resolution of Time Sampling

Modulation effect is caused by limited time sampling frequency due to sample and hold in A to D converters and computational delay. The computational unit cannot determine the required duty cycle until the data taken from A/D converter is ready. After getting the output voltage level, the digital controller spends extra clock cycles to compute the required duty cycle. The combined effect of these two delays installs a constant time delay in the control loop. This time delay would result in extra phase shift in the control loop, especially when the testing frequency is high. This extra phase shift would reduce the phase margin of the converter, or even cause loop instability when it is too large. The time sampling frequency for a stable system can be obtained by Z-domain loop analysis [1,2,5,6].

IV. Theory

A. Combined effect of Time-Sampling and Quantization Resolution in Digital Control

There are research work on time-sampling and quantization resolution. However, still none of them combine the considerations on both sampling rate and quantization resolution. The following mapping is constructed by applying the equations shown in the previous section separately:

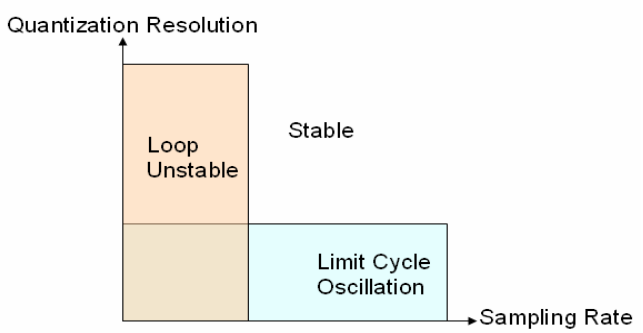


Fig. 3 2D Mapping on Sampling Rate and Quantization Resolution

In this mapping, the boundary between stable and unstable is made up by two straight lines, which are parallel to X and Y axes. It is because the minimum requirement for both sampling rate and quantization resolution are independent of each other.

However, in real digital systems sampling and quantization effects do not exist separately, especially when both sampling and quantization resolution are low.

Poor quantization resolution would result in limit cycle oscillations. However, the effect of time-sampling and quantization resolution cannot be considered separately when choosing digital controller, especially when both of them are limited. This is because the time-delay effect in time sampling would enhance the effect of limit-cycle oscillation, causing larger steady state oscillations. When limit cycle oscillation occurs digital power converters give unstable voltage waveform shown below:

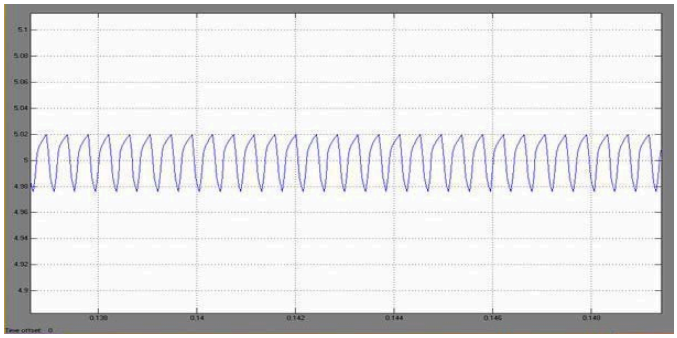


Fig. 4 Limit Cycle Oscillation

Let us consider a sinusoidal input signal as shown in Fig 5 in solid line. After it is subjected to a quantization resolution of 0.2V, the maximum quantization error is 0.1V. That means the signal after quantization (broken line) should have an error of ±0.1V.

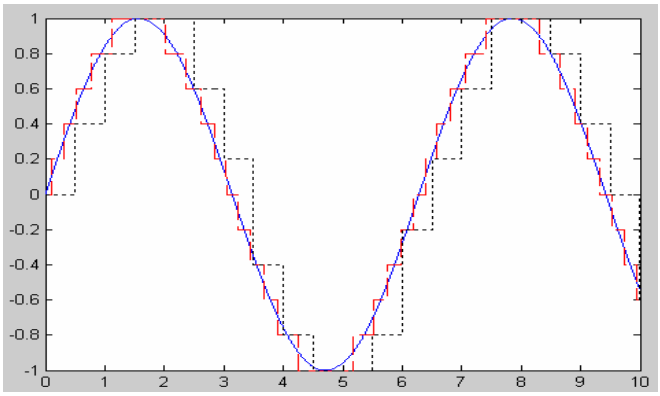


Fig. 5 Quantization and the Combination of the 2 Effects on Sinusoidal Signal

In most cases sampling rate and quantization resolution are designed separately. That means to find the minimum required sampling rate or quantization resolution while assuming the other value to be constant. However, this is based on the assumption that sampling rate and quantization are independent of each other and actually this is not true.

Actually quantization resolution can cause limit cycle oscillation in power converters which was supposed to be caused by sampling rate only. Oscillation can occur because of insufficient quantization of output PWM to specify the desired output level.

When considering sampling together with quantization effect, the maximum error between the original signal and the sampled signal is no longer ±0.1V. Quantized signal subjected to a sampling of 0.5 time unit would result in a waveform as shown in dotted line which is much worse. The maximum error between the signal after quantization and sampling can be as high as ±0.35V. It is because the signal voltage can move further away from the quantization level within the sampling time, when the signal is hold within the period. The decrease of effective quantization resolution due to sampling makes digital controlled power converters more likely to suffer from limit cycle oscillations.

Insufficient time-sampling will produce phase lag in the control loop of a power converter. In the extreme cases, a total phase lag of over 180 degree in the whole control loop would result in loop instability. When the loop is unstable digital power converters may give oscillating voltage waveform as shown below:

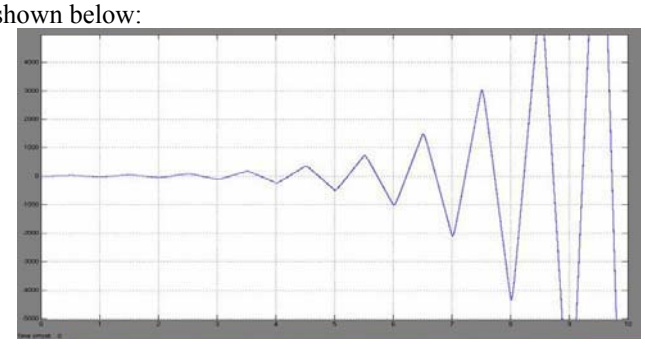


Fig. 6 Loop Unstable Voltage Waveform

Sampling will also add to voltage error. In Fig. 7 a sinusoidal input signal is shown in solid line, a sampling time of 0.5 time unit would cause a distorted waveform shown in dash dotted line. It can be observed that the sampled signal would have a delay from the original signal, where the maximum delay time is equal to the sampling time.

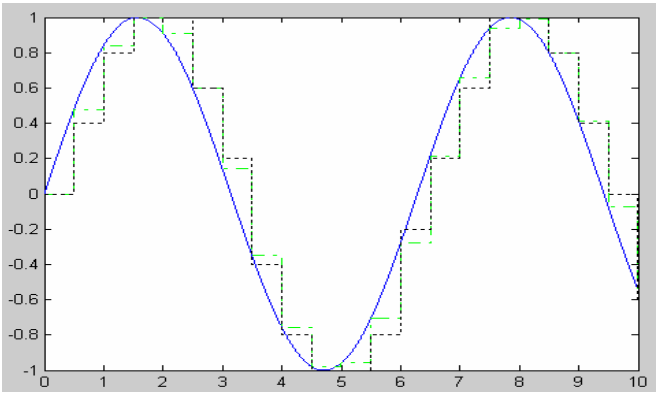


Fig. 7 Sampling Effect and the Combination of the 2 Effects on Sinusoidal Signal

For a sinusoidal signal as shown subject to 0.5 time unit sampling and 0.2V quantization, the maximum delay from the original signal is 0.65 time unit, which is longer than the sampling time itself.

The effects of quantization and sampling are interdependent. When the effect of sampling and quantization are considered together, the boundary of stability is no longer the rectangular shape shown in Fig. 3. In fact, it is found that the quantization resolution required to avoid limit cycle oscillation is higher when sampling rate is low; and the sampling requirement to avoid converter loop instability is higher when quantization resolution is low. It is needed to modify the shape of the 2D mapping on sampling rate and quantization resolution as shown in Fig. 8.

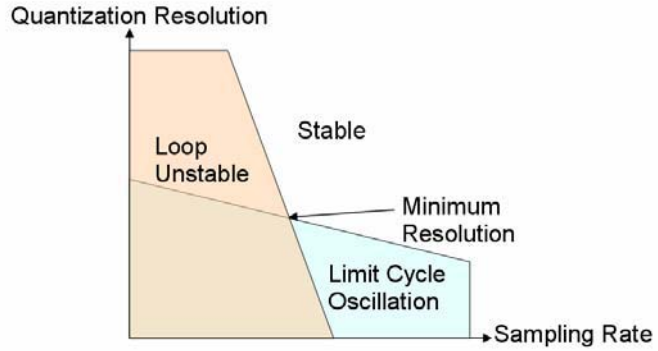


Fig. 8 2D Mapping on Sampling Rate and Quantization Resolution

It is proposed that the effect of sampling rate on limit cycle oscillation and the effect of quantization resolution on loop stability are linearly related in log scale, making a trapezoidal shape in the 2D mapping.

A computer simulation model is established based on Simulink to study the interdependent effect. This model simulates voltage response of a digital controlled power converter. Converter specifications including converter topology, switching frequency, input voltage, output voltage and current are the input variables of this model.

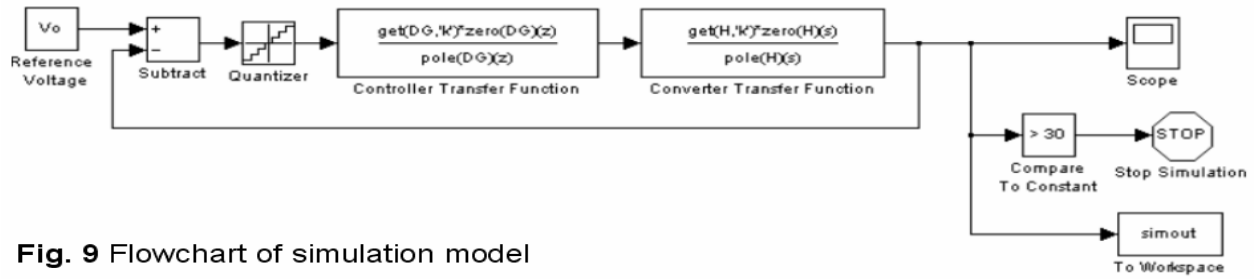


Fig. 9 Flowchart of simulation model

B. Computer Simulation Model for Digital Power Converters

In Fig. 9, the system flow chat of the simulation model is shown. It contains two main functional blocks. The converter transfer function blocks simulates voltage response of the power converter according to the converter specification. Controller transfer fuction block represents the digital controller used to control power converter. The controller characterstic is determined by the transfer function and sampling frequency of the microcontroller which is represented in Z-domain. The time sampling effect of digital controller is simulated in this block. A quantizer block in series with the controller transfer to simulate the quantization resolution effect of the digital controller. These blocks form a closed loop to simulate the closed loop stability of the digital controlled power converter.

Converter stability is determined by the simulated output voltage. There are three cases to detect instability in this computer simulation model. They are loop stability, limit cycle oscillation and steady state error.

Loop stability is the first to detect in this model. Output voltage with uncontrolled enchancing oscillation over time is detected by the simulation model and regarded as loop unstable case. Limit cycle oscillation is output voltage oscillation among different output levels in steady state. It is detected by simulating the ampitude of output oscillation in the steady state (say 5 seconds after disturbance). Steady state error is detected by comparing the permitted voltage variation and the difference between steady output and the desired value.

A buck converter with 12V input, 5V 12A output at 66kHz switching frequency is simulated using Simulink.

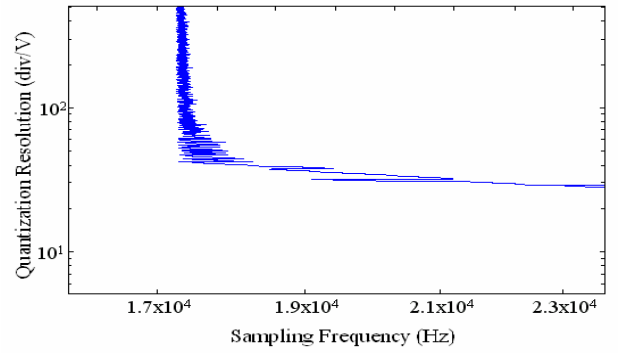


Fig. 10 Simulated Boundary of Stability

From simulation, a full mapping of minimum sampling frequency required for each quantization resolution can be plotted.

The shape of the simulated mapping is not quite the same as the simple map in Figure 3. This shows the minimum requirement of time sampling and quantization resolution are dependent on each other.

V. Problem Formulation

To specify the minimum requirement of sampling frequency and quantization resolution, it is necessary to formulate the boundary of loop unstable and limit cycle oscillation. By using equation fitting technique, specific relations for the buck converter can be represented by two equations like those that follow:

$$\ln(\text{Quantization Resolution}) = -69.947 \bullet \ln(\text{Sampling Frequency}) + 689.98$$

-dotted line

$$\ln(\text{Quantization Rsolution}) = -1.4573 \bullet \ln(\text{Sampling Frequency}) + 18.033$$

-solid line

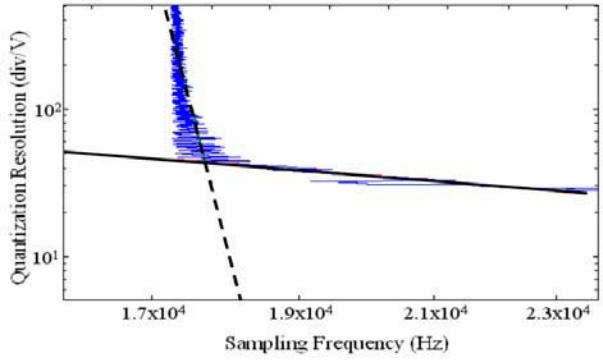


Fig. 11a Equations Fitted to the Simulated Mapping

To cover all variations and possible errors in the simulation, we need to add a safety factor to our prediction. It is found that a safety factor of 20% is enough in experiments. The two equations become:

$$\ln(\text{Quantization Resolution}) = (-69.947 \bullet \ln(\text{Sampling Frequency}) + 689.98) \bullet 1.2$$

$$\ln(\text{Quantization Rsolution}) = (-1.4573 \bullet \ln(\text{Sampling Frequency}) + 18.033) \bullet 1.2$$

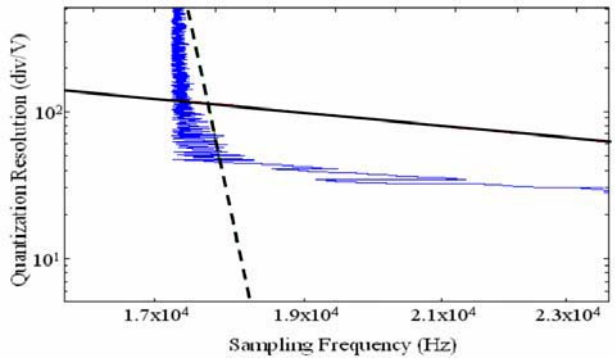


Fig. 11b 20% Safety Factor Inserted to the Equations

These two equations are the constrains to optimize the sampling frequency and quantization resolution of the digital control system.

To optimize the sampling frequency and quantization resolution of the system, it is also necessary to set limits for the digital control system. In this case, the sampling frequency and the quantization resolution limits are set to be 10 MHz and 16 bit, which the best configuration possible.

So the search for minimum configurationis carried out under the following constrains:

$$\ln(\text{Quantization Resolution}) \geq (-69.947 \bullet \ln(\text{Sampling Frequency}) + 992.4) \bullet 1.2$$

$$\ln(\text{Quantization Rsolution}) \geq (-1.4573 \bullet \ln(\text{Sampling Frequency}) + 25.937) \bullet 1.2$$

$$\text{Quantization Resolution} \leq \frac{2^{16}}{\text{Full Range A/D Voltage}}$$

$$\text{Sampling Frequency} \leq 10\text{MHz}$$

where

Quantization Resolution = A/D resolution in division per V

Sampling Frequency=Microcontroller sampling frequency in Hz

VI. Search for Minimum Sampling Frequency and Quantization Resolution

Since there are two variables, sampling frequency and quantization resolution, needed to minimize in this optimization problem.

An objective function

$$\min\{\text{Quantization Resolution} + \text{Sampling Frequency} \bullet 200\}$$

is used to demonstrate the search of minimum microcontroller requirement of digital controlled buck converter.

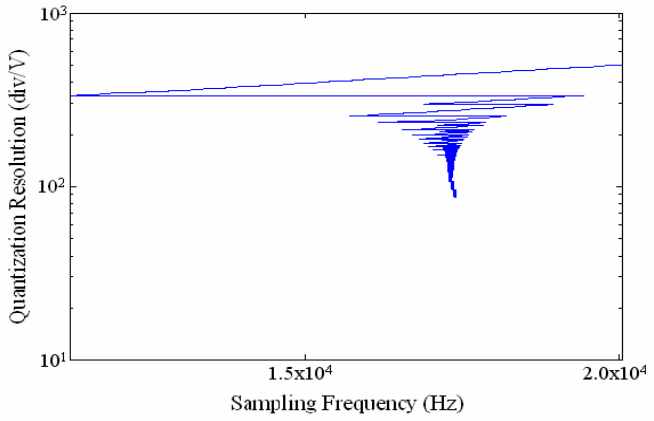


Fig. 12 Iteration Process to Obtain Equilibrium Point

With the objective function and constrains set in the previous section, the minimum sampling frequency and quantization resolution for digital controller can be found. By using an initial starting point of 20 kHz sampling frequency and 500div/V quantization resolution, a searching process is launched to find out the minimum configuration required.

Under these constrains and the objective function, a search iterative procedure is then applied to determine the optimal solution. In this case, there is only one equilibrium point in the system, which is the minimum sampling frequency and quantization resolution required in the system.

The equilibrium point obtained after the search iterative procedure is on (18231, 88) in this particular case. That means a microprocessor of at least 18231Hz sampling rate and 88 divisions per volt A/D quantization resolution need to be used.

VII. Solution Algorithm

An algorithm to find the minimum sampling frequency and quantization resolution for digital controlled power converter is developed and employed. The flowchart of this algorithm is shown in Figure 13.

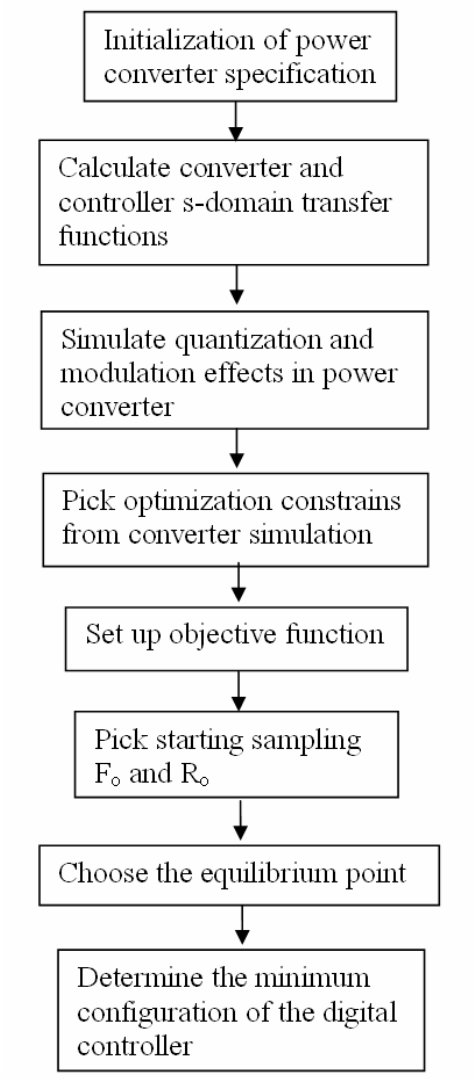


Fig. 13 Flowchart for Solving the Minimum Sampling Frequency and Quantization Resolution for Digital Controlled Power Converters

This solution algorithm starts with the initization of power converter specifications. Converter topology, switching frequency, input voltage, output voltage and current are specified in this block. With this specifications, s-domain converter transfer function can be calculated. S-domain controller transfer function is constructed by using pole-zero compensation method.

The computer simulation model described in the pervious section is then used to simulate quantization and modulation effects of the power converter. Boundary of stability is formulated by the simulation results. With an objective function to be minimized, the searching process starts by an initial guess F_o and R_o

The search for equililbrum point is an iterative process. The number of iterating times can be lower if a near initial point is chosen. Minimium configuration of the digital controller required for the power converter is then obtained by the searching process.

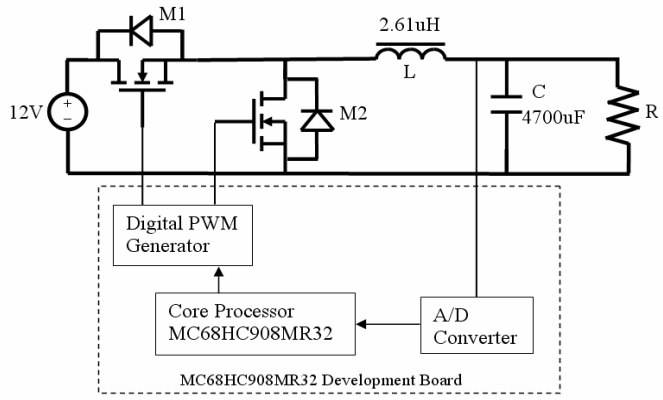
VIII. Experimental Results

A set of experiments on two fundamental power converter topologies, buck and boost converters, is used to verify the result obtained from the solution algorithm. They represents control charactistics for all buck and boost devied power converter topologies.

Buck Converter

The tested digital controlled buck converter is designed to generate the output voltage regulated at 5V (with 2% allowed variation) at the output power of 60W, from an input voltage of 12V.

The test bed used to validate the solution algorithm is shown below. The setup consists of a Motorola MC68HC908MR32 development board [15] and the buck converter power stage.



By using the solution algrithm with 20% safety factor added, expermiental results show that all untable cases are below the minimium configuration.

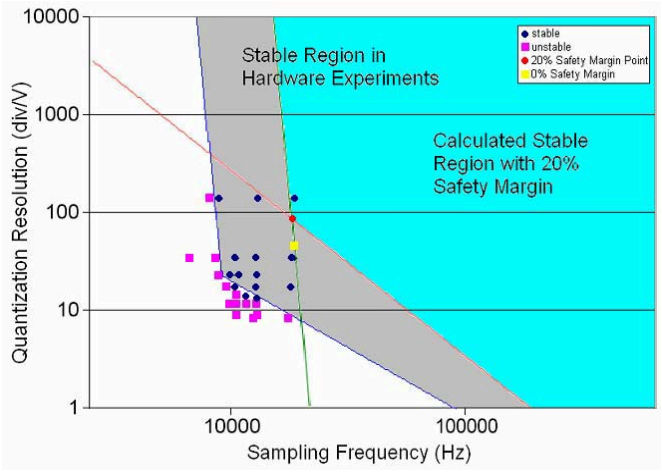
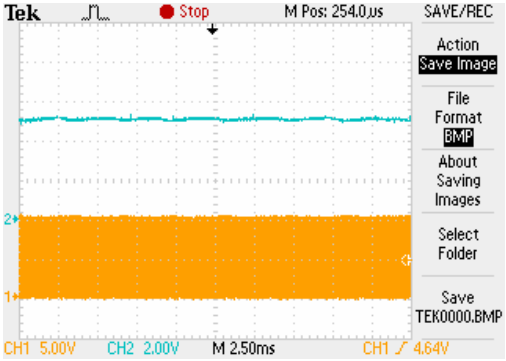
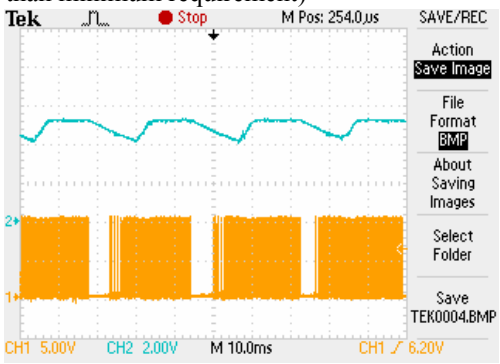


Fig. 14 Designed Boundary and Experiment Results for Buck Converter

a) Stable Operation
Time sampling frequency = 18500 Hz
Quantization resolution = 132.5 div/V
(higher than minimum requirement)

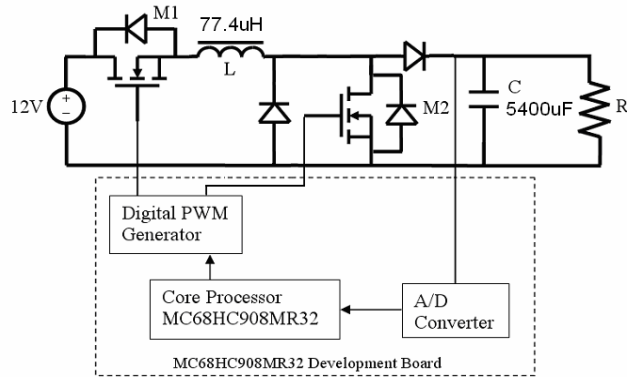


b) Unstable Operation
Time sampling frequency = 8820 Hz
Quantization resolution = 34.1 div/V
(lower than minimum requirement)



Boost Converter

The tested digital controlled boost converted is designed to generate output voltage regulated at 12V (with 2% allowed variation) at the output power of 60W, from an input voltage of 5V.



By using the solution algrithm with 20% safety factor added, expermiental results show that all untable cases are below the minimium configuration.

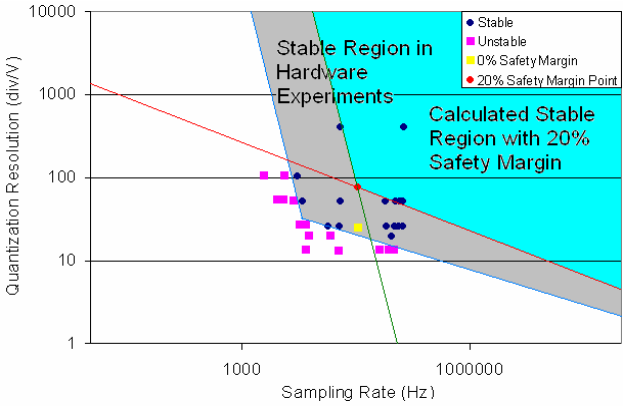


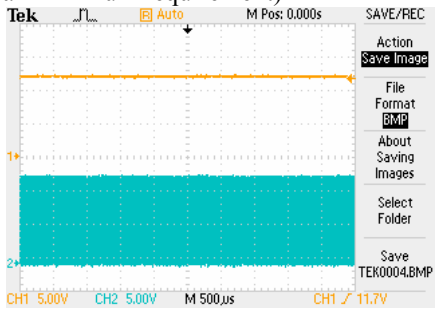
Fig. 15 Designed Boundary and Experiment Results for Boost Converter

a) Stable Operation

Time sampling frequency = 19236 Hz

Quantization resolution = 51.2 div/V

(higher than minimum requirement)

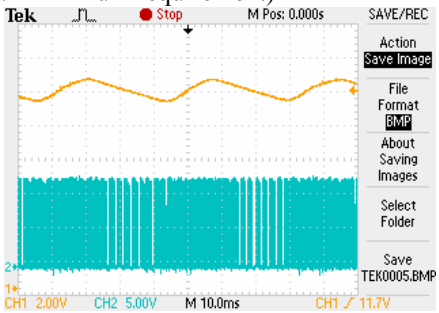


b) Unstable Operation

Time sampling frequency = 14739 Hz

Quantization resolution = 19.2 div/V

(lower than minimum requirement)



IX. Conclusions

A solution algorithm to search for minimum sampling frequency and quantization resolution for digital control of power converters is presented in this paper. The proposed algorithm combines considerations on quantization and modulation effects to find out optimization constrains in terms of loop stability and limit cycle oscillation.,A diagrammatic method is used to find out the minimum sampling frequency and quantization resolution required for the digital system. This algorithm is applied and tested on buck and boost converter control systems to test for stability. Experiment results verify the algorithm.

References

[1] Prodic, A., Maksimovic, D., Erickson, R.W. "Design and implementation of a digital PWM controller for a high-frequency switching DC-DC power converter" in The 27th Annual Conference of the IEEE Volume 2, 29 Nov.-2 Dec. 2001 Page(s):893 - 898

[2] Duan, Y., Jin, H., "Digital controller design for switchmode power converters" in APEC '99. Fourteenth Annual Volume 2, 14-18 March 1999 Page(s):967 - 973

[3] Hao Peng, Maksimovic, D., Prodic, A., Alarcon, E. "Modeling of quantization effects in digitally controlled DC-DC converters" in PESC 04. 2004 IEEE 35th Annual Volume 6, 20-25 June 2004 Page(s):4312 - 4318

[4] Peterchev, A.V., Sanders, S.R. "Quantization resolution and limit cycling in digitally controlled PWM converters" in IEEE Transactions on Power Electronics Volume 18, Issue 1, Part 2, Jan. 2003 Page(s):301 - 308

[5] Van de Sype, D.M., De Gusseme, K., Van den Bossche, A.R., Melkebeek, J.A. "Small-signal z-domain analysis of digitally controlled converters" in PESC 04. 2004 IEEE 35th Annual Volume 6, 20-25 June 2004 Page(s):4299 - 4305

[6] Rajasekaran, V., Jian Sun; Heck, B.S. "Bilinear discrete-time modeling for enhanced stability prediction and digital control design [of switching power converters]" in PESC 02. 2002 IEEE 33rd Annual Volume 2, 23-27 June 2002 Page(s):803 - 808

[7] White, S. "Quantizer-induced digital controller limit cycles" in Transactions on IEEE Volume 14, Issue 4, Aug 1969 Page(s):430 – 432

[8] Wu, A.M., Jinwen Xiao, Markovic, D., Sanders, S.R. "Digital PWM control: application in voltage regulation modules" in PESC 99. 30th Annual IEEE Volume 1, 27 June-1 July 1999 Page(s):77 - 83

[9] Patella, B.J., Prodic, A., Zirger, A., Maksimovic, D. "High-frequency digital PWM controller IC for DC-DC converters" in Transactions on IEEE Volume 18, Issue 1, Part 2, Jan. 2003 Page(s):438 - 446

[10] Kranz, C. "Complete digital control method for PWM DCDC boost converter" in PESC '03. 2003 IEEE 34th Annual Volume 2, 15-19 June 2003 Page(s):951 - 956

[11] Monti A., Santi E., Dougal R.A., Riva, M. "Rapid prototyping of digital controls for power electronics" in IEEE Transactions on Power Electronics Volume 18, Issue 3, May 2003 Page(s):915 - 923

[12] Saggini, S. Ghioni, M. Geraci, A. "An innovative digital control architecture for low-Voltage, high-current DC-DC converters with tight voltage regulation" in IEEE Transactions on Power Electronics Volume 19, Issue 1, Jan. 2004 Page(s):210 – 218

[13] Stefanutti, W., Mattavelli, P., Saggini, S., Garcea, G. **"**Energy-based approach for predicting limit cycle oscillations in voltage-mode digitally-controlled dc-dc converters" in Applied Power Electronics Conference and Exposition, 2006. APEC '06. Twenty-First Annual IEEE 19-23 March 2006 Page(s):7 pp.

[14] Saggini, S., Stefanutti, W., Trevisan, D., Mattavelli, P., Garcea, G. "Prediction of limit-cycles oscillations in digitally controlled DC-DC converters using statistical approach" in Industrial Electronics Society, 2005. IECON 2005. 32nd Annual Conference of IEEE 6-10 Nov. 2005 Page(s):6 pp.

[15] Freescale MC68HC908MR32 Microcontroller datasheet