Simple Modeling for Conducted Common-Mode Current in Switching Circuits

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ABSTRACT:
Common mode current strongly depends on stray capacitance of each circuit node, especially those with high dv/dt and di/dt. To build a simple model for conducted common mode current in switching circuit a computer software based on Partial Element Equivalent Circuit (PEEC) method is used to calculate the parasitic elements of the printed circuit board (PCB). Simulation results agree well with experimental results up to 10 MHz.

I. INTRODUCTION

It is well known that differential mode DM noise is caused by switching operations of the circuit. However, common mode CM noise, a dominant component of EMI, is more complicated and not readily understood. Therefore, conducted Electromagnetic Interference (EMI) is a major concern for power electronics engineers. Accurate EMI prediction using parasitic elements extraction are necessary.

Paul[1] presented a model for common mode noise and represented the noise source by a current source. However, he did not elaborate on the formation of the noise current, and the model is inadequate for switching circuits. Nakahara[2] presented a high frequency model for common mode noise in switching power converter, where he used a voltage source to represent the switching action. Unfortunately, not all stray capacitances to ground are considered in his model.

Considering the influences of stray capacitance, a simplified model for a switching circuit is presented in this paper. It is true that conducted CM current is mainly caused by switching operations and stray capacitances. Hence stray capacitance of every node to earth are considered in the model[3]. Switching action is modelled by a switched voltage source.

The parasitic elements of the PCB tracks are calculated by using computer software "StatMod" (capacitance calculation) based on the PEEC method. Simulation of the proposed model is done by Pspice simulator.

Simulation results are compared with the experimental measurement, satisfactory comparison is achieved up to 10 MHz and confirms the validity of this model.

II. ASSUMPTIONS FOR SIMPLIFICATION

The conductive CM current in a switching circuit is caused by dv/dt at each node of a switching circuit and its associated stray capacitance. By this proposition we draw the following rules to build up a simple CM current model for a switching circuit with high dv/dt.

1. Replace an active semiconductor switch by a voltage source with the same voltage waveform as seen across the semiconductor switch. This is the first step to simplify a switching circuit. Very often a full semiconductor model has too many parameters to manipulate and does not allow an engineer to study the effect of dv/dt on the power circuit easily. An independent voltage source is a simple way to represent such an effect.
2. Present stray capacitance at each circuit node to the model, since stray capacitance at each circuit node to earth forms a path for common mode current. Stray capacitance, which should be represented accurately and very often, is dictated by layout and the shape of the printed circuit board conductor of that node. Such a capacitance is usually too small and too difficult to be measured. Therefore we use a Finite Element Analysis (FEA) software program called " StatMod" to calculate the capacitance concerned according to the shape of the printed circuit board trace.
3. Introduce an AC equivalent circuit to the model. Noise measurement usually ignores DC component in a circuit. Therefore a DC source can be ignored. This can simplify the model to a considerable extent.
4. Represent all components by their high frequency AC equivalent circuits. The frequency range in the conducted EMI range goes up to 30MHz. At such high frequencies, many passive components can no longer be represented by their ideal models. The proper equivalent circuit can be measured and used in the model.

III. MODELING

A typical switching circuit is shown in Fig.1. The switching circuit is connected to a Line Impedance Stabilization Network (LISN), which provides a stable line impedance (50 Ω). And prevents also the external noise from contaminating the measurements over the frequency range of the conducted CM noise. A high frequency equivalent circuit

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of this switching circuit is shown in Fig. 2.

It is well known that at high frequency the impedance of a real input capacitor and a resistor in an actual circuit shown in Fig.1 are appropriately modeled as shown in Fig.2 [8], where the dashed block represents the high frequency equivalent circuit of the LISN.

The other parameters in this equivalent circuit shown in Fig.2, such as the equivalent series resistances (ESR) and equivalent series inductances (ESL) of the input capacitor and the resistor, can be experimentally determined by using an impedance analyzer HP4194.

The circuit model used for the simulation was represented with the input capacitor impedance and the resistor impedance as a function of the parasitic elements, which are necessary for the investigation of the high frequency behavior as shown in table 1.

Table 1 The Pspice models for passive components of the circuit

Components	Circuit symbole	Pspice-Model
Resistor	r	L2 197.365n R2 449.468 C5 210.27n
Capacitor	C	L1 184.891 C4 215.643n R1 0.1275

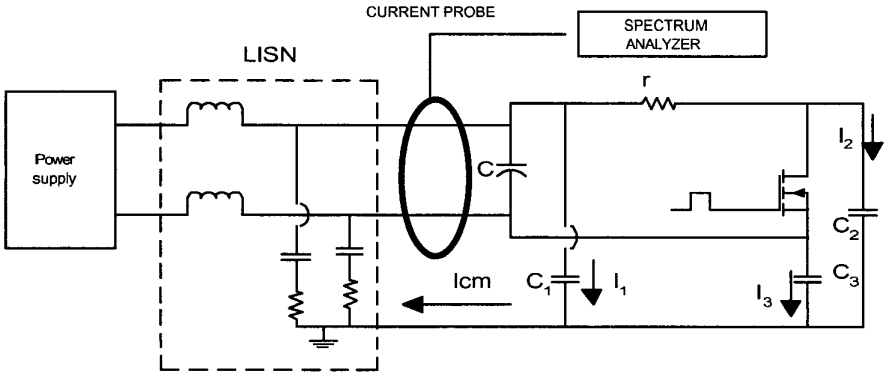

Fig.1 Actual circuit schematic

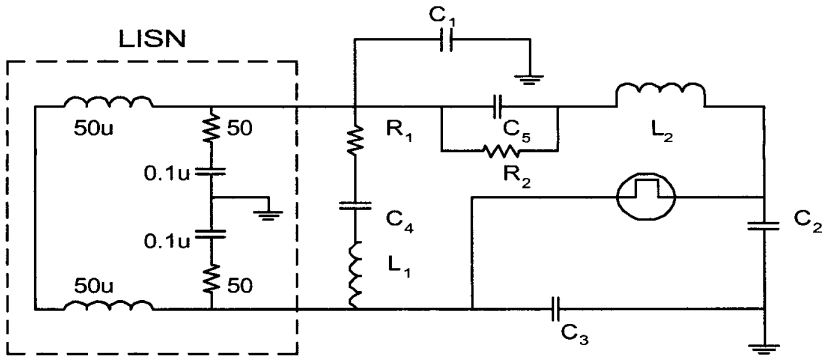

Fig.2 Conducted CM model for the switching circuit in Fig.1

While C_1, C_2, and C_3 are referred to the stray capacitances of the traces of the PCB layout, which can be calculated by means of the StatMod software. This software can be used for parasitic parameters calculation. It is achieved by discretizing the structure of the circuit layout in small elements and calculating its parasitic parameters by using simplified Maxwell equations with high accuracy. Its consists of field simulation program working in a frequency domain and can calculate the self capacitances and their matrix representations of the conductor system as shown bellow rather than using traditional equations as used in [13,14].

A lumped capacitance matrix (values in Farad) form is shown below:

$$\begin{pmatrix} 4.54e-12 & 0.00e+00 & 0.00e+00 \\ 0.00e+00 & 15.7e-12 & 0.00e+00 \\ 0.00e+00 & 0.00e+00 & 9.5e-12 \end{pmatrix}$$

The simplified model used in this paper has three conductors with a shape shown in Fig.3,where the conductors are defined as three polygons placed horizontally on the top layer of the dielectric, and the ground plane is placed on the bottom layer. After drawing and running tasks, StatMod program can automatically calculate the self capacitances of the conductors C_{d1}, C_{d2} and C_{d3} .

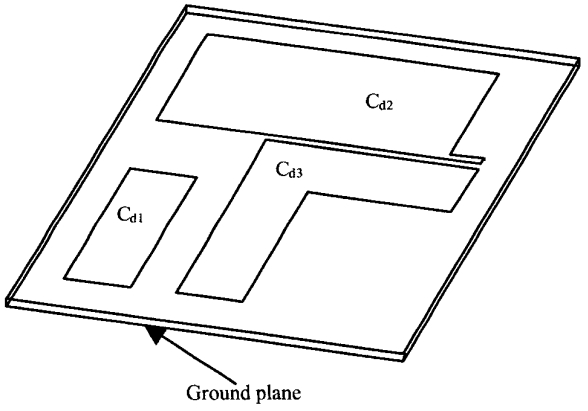

Fig.3 Conductor system schematic used for self-capacitances calculation

IV EMI PREDICTION OF CM CURRENT

Based on the simple model shown in Fig.2 and the extraction method of PCB traces described above, prediction of conducted CM current in the switching circuit is able to be performed as shown in Fig.4, where a comprehensive flow chart is illustrated.

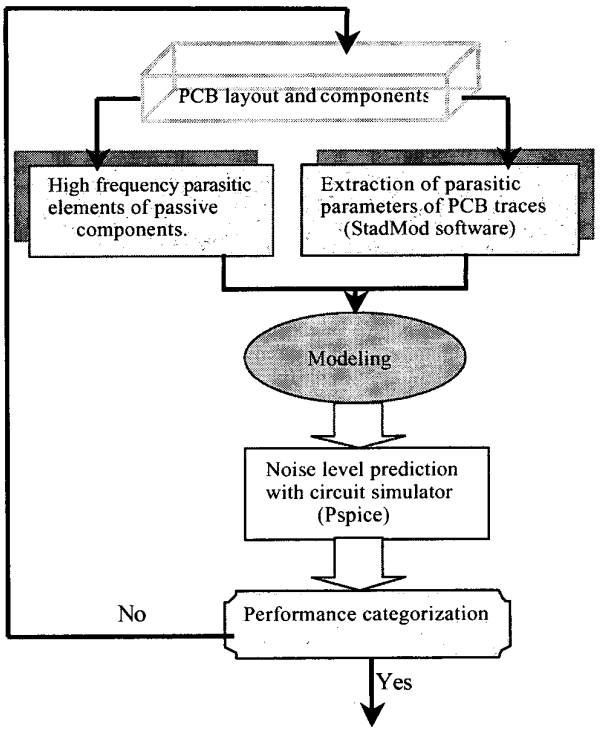

Fig.4 Prediction of EMI behavior of the switching circuit

First of all, the switching power circuit topology is selected and its layout is properly made. Then combine all essential parasitic parameters of the passive components modeled with high frequency elements, and of PCB layout traces calculated with StatMod computer software. The next step is to predict and analyze conducted CM noise for the modeled circuit using circuit simulator PSpice. And then compare the noise level with EMI compliance standards. If the simulation result doesn't meet the EMI compliance, the designer will be informed to modify the layout. Then the prediction will process another time until EMI compliance is satisfied.

V. SIMULATION AND EXPERIMENTAL RESULTS

The simulation result of CM current noise summing of the currents through the three stray capacitances to earth is represented in Fig.5. Experimental measurement is carried out using the circuits shown in Fig. 1. Two input power leads are passed through a high frequency current transformer simultaneously to measure the common mode current involved. The experimental result is shown in Fig. 6. The experimental measurement result agrees reasonably well with the simulated result up to 10 MHz. To be able to compare the simulation and experimental results we have to use the conversion relationship [8] as follows:

$$k(dBuV) = 20\log U/Ur \qquad (1)$$

Where
k: Voltage ratio
U: Measured voltage.
Ur: Reference voltage equal to 1uV.
The sensitivity of the current probe used is equal to 2 (1/ Ω). Then the voltage measured across the probe determines the current:

$$I = 2 \times U \qquad (2)$$

In the comparison of the predicted and the measured conducted CM noise, the amount of the attenuation 10dB of transient limiter with frequency range of 9KHZ-200MHz and the gain of 28dB of the amplifier with a frequency range of 9KHz-1.3GHz should be taken into consideration.
The trend of the simulated result follows the measured one in the lower frequency range(under 10MHz).

VI. PROPOSED MODEL PERSPECTIVE

The modeling approach used in this paper can be extended to the switching mode power supply SMPS. In this case the magnetic component must be accurately modeled and the core affect on the common mode noise must be also taken into consideration in order to provide satisfied simulation results[4] . In addition to the eddy current generated by the core, which causes uneven current distribution in each trace and it also can be accounted for during parasitic parameters extraction[11]. As a matter of fact, the losses and the energy storage in the windings of a magnetic component depend not only on the physical characteristics of the component, but also on its working mode. The frequency and the waveforms of both the current and the voltage affect clearly the performance of the magnetic component. Therefore these factors should be taken into account when modeling magnetic component. Furthermore, the model must involve high frequency losses in the core and in the windings (skin and proximity effects) in a frequency range up to 30MHz (upper limit of conducted EMI standards). In this case, it is possible to simulate the generation, transmission and the damping of high frequency ringing in the magnetic component.
More realistic agreement between the simulation and the measurements over wide conducted EMI frequency range in magnitude values and envelop shapes can be obtained, if complete extraction of parasitic elements, such as green wire inductance L_g, which is responsible of blocking the Conducted CM noise flowing trough the green wire path, is performed[9,1]. The neglected self- mutual inductance L_{ci}, for each PCB trace might affect the conducted CM current noise flowing through these conductors. Likewise, the capacitances C_P and C_N from drain node (hot node) to input line, can contribute to significant EMI noise[15] too. The neglected parasitic parameters are shown in Fig.7 drawn with dashed lines.

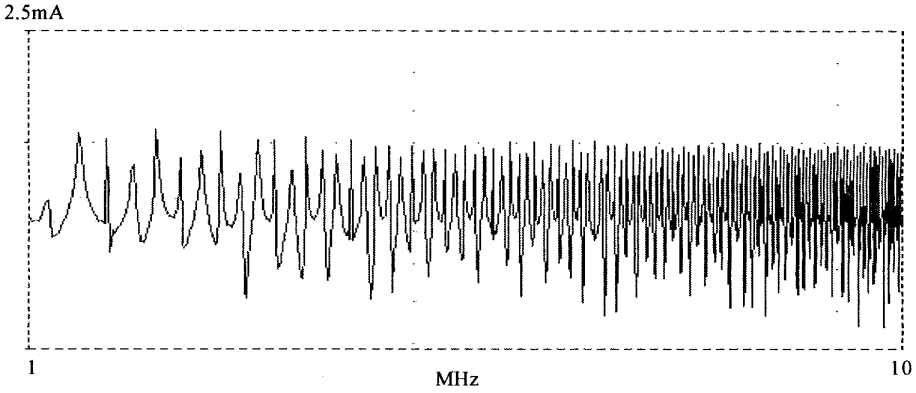

Fig.5. Simulated CM noise currents in the frequency range 1MHz to 10MHz.

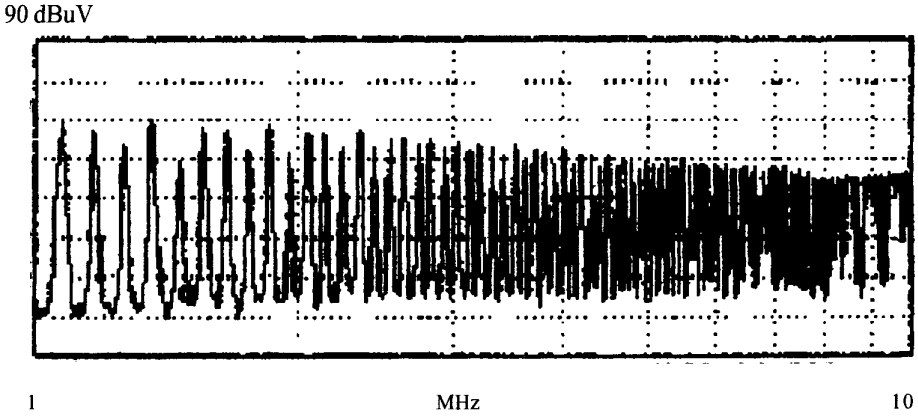

Fig.6 Experimental result of the conducted CM noise Current.

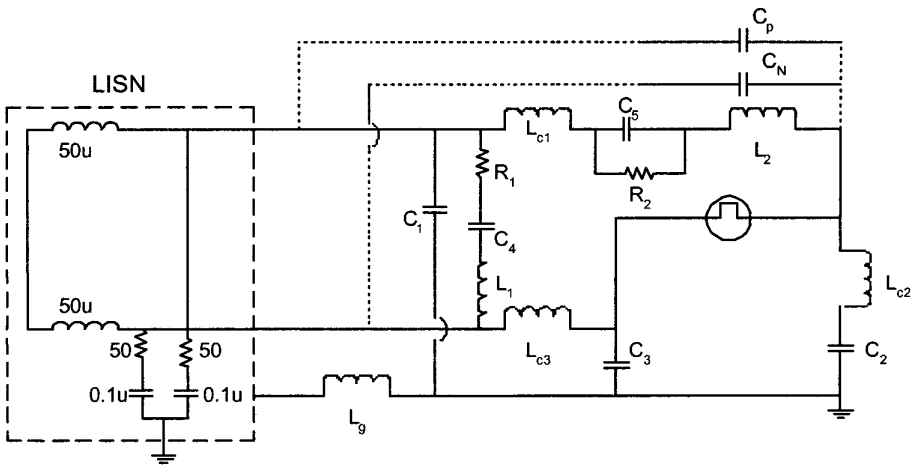

Fig.7 Model with additional stray parameters having possible effect on conducted CM noise.

VII. CONCLUSION

A set of rules to establish a simple comprehensive model for a switching circuit is presented in this paper. These rules are applied to a simple switching circuit and a comprehensive model is established by simplified parasitic elements extraction. Simulation results agree well with experimental results up to 10MHz. The rules can be applied to switching Mode Power Supply SMPS and produce a comprehensible model too. Also the results establish a fact that common mode current is largely affected by stray capacitance of all nodes in a switching circuit with considerable dv/dt.

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