Effects of Mismatch on CMOS Double-Balanced Mixers: A Theoretical Analysis

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***Abstract*—Effects of mismatch on CMOS double-balanced mixers are studied. The mixer is analyzed as a two-stage circuit. The effects of mismatch, including second-order intermodulation, feedthrough and degradation of conversion gain, are discussed for each stage. A relation between processing-induced variances of transistor parameters and mixer performance is derived.**

I. INTRODUCTION

Processing-induced device mismatch causes time-independent random variations in physical quantities of identically designed devices [1–5]. The impact of MOS transistor mismatch becomes more important as dimensions of devices are reduced and the available signal swing decreases [1]. Mismatch is a fundamental design parameter for precision analog circuit design [2]. As critical blocks in wireless transceivers, mixers are very susceptible to mismatch effects. The double-balanced CMOS mixer [6][7], as shown in Fig.1, is a commonly used topology in CMOS integrated receivers for frequency translation of radio-frequency (RF) carrier signals by converting a local-oscillator (LO) and the incoming RF signal into an intermediate-frequency (IF). Under normal conditions, this mixer produces only odd harmonics at its output $i_{out}(t)$. In the presence of mismatch, however, the input transistor pair (M1 and M2) introduces second-order intermodulation, which feeds through the cascaded mismatched switch pairs and cause undesirable spectral components at baseband. This is not a critical issue in high IF architectures, because a band pass filter following the mixer can eliminate the spurious signals in baseband. Therefore, in conventional double-conversion (Heterodyne) receivers that convert RF signals into high IFs, mixers are only required to have a high third-order intercept point (IP3) [8] in order to meet system linearity specifications. However, in zero and low IF architectures, the even-order distortion terms are also of particular concern [9]. As the direct-conversion receiver architecture [10], in which a zero IF is used, has been attracting attention as a possible solution to a single-chip receiver, mismatch effects in CMOS mixers deserve attention.

Mismatch in a mixer is induced by factors both intrinsic and extrinsic to the transistors. The intrinsic factors are those arising from transistor devices whereas the extrinsic ones include asymmetries in other parts of circuit such as wire length, feed-in and feed-out resistors. While the even-order distortion terms are also induced by factors such as single-ended input and output of a double-balanced mixer [11] in addition to mismatch, only effects originating from intrinsic transistor mismatch are considered in this study.

This paper introduces a theoretical analysis of mismatch effects on CMOS double-balance mixer. The model used to characterize MOSFET mismatch will be presented in Section II. The effects of mismatch effects on the input V-I converter and switch pairs are discussed in Section III.

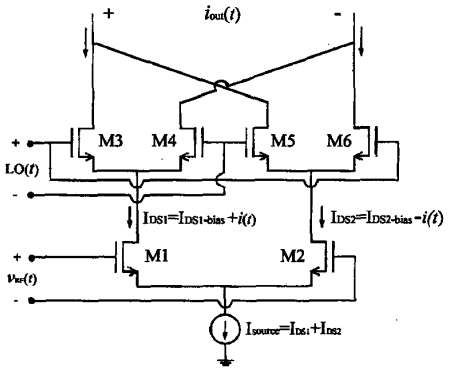

Fig.1. Double-balanced CMOS mixer.

II. MISMATCH MODEL

A MOSFET model is needed for the mismatch study. This model should be detailed enough such that it reflects accurately the behavior of sub-micrometer transistors. An acceptable MOSFET model in the saturation region is [12]

$$I_{DS}=\frac{1}{2}\beta\frac{(V_{GS}-V_T)^2}{1+\theta(V_{GS}-V_T)}\ , \tag{1}$$

where I_{DS} is the drain current, V_{GS} is the gate-source voltage, V_T is the threshold voltage, $\beta=C_{OX}\mu\frac{W}{L}$ is the current factor, with C_{OX} being the gate-oxide capacitance per unit-area, μ as the carrier mobility, W and L being the width and length of the transistor respectively. The parameter θ is the effective mobility [13], which includes the effects of surface scattering and the source series resistance. For a minimum-length device of an existing 0.8-μm technology, it was estimated to be 0.9 V^{-1}. For a different 0.25-μm technology, it was found to be approximately 2.5 V^{-1} [14].

Within this model, the parameter set $\left\{\frac{\Delta\beta}{\beta},\Delta V_T,\Delta\theta\right\}$ is used for matching description. The mismatch model can be derived by differentiating Eq.(1) with respect to the parameter set, resulting in

$$\frac{\Delta I_{DS}}{I_{DS}}=\frac{\Delta\beta}{\beta}+\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial V_T}\Delta V_T+\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial\theta}\Delta\theta\ . \tag{2}$$

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Assuming Gaussian distribution for the mismatch parameters [1], these parameters can be characterized by their variances: $\sigma^2\frac{\Delta\beta}{\beta}, \sigma^2_{\Delta V_T}, \sigma^2_{\Delta\theta}$, and their correlations coefficients. The variance of mismatch in the current is thus given by

$$\sigma^2\frac{\Delta I_{DS}}{I_{DS}} = \sigma^2\frac{\Delta\beta}{\beta} + \left(\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial V_T}\right)^2\sigma^2_{\Delta V_T} + \left(\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial\theta}\right)^2\sigma^2_{\Delta\theta} + \text{correlation terms} \quad (3)$$

The values of these standard deviations and correlation coefficients can be evaluated by various means [1–5]. In this paper, we assume that all of these values have been determined.

III. MISMATCH ANALYSIS IN MIXER

The operation of a double-balanced mixer can be modeled by the diagram in Fig.2. The RF input stage is a transconductance converter. This stage corresponds to transistors M1 and M2 in Fig.1. The LO signal drives the switching stage that is implemented by transistors M3–M6. There is also a feedthrough path from the RF input stage to the output of mixer in the presence of mismatch in the switch pairs [15], as we will discuss below.

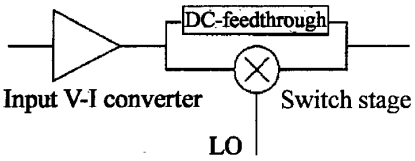

Fig. 2. Mixer model with input V-I converter, switch stage and DC-feedthrough path [15].

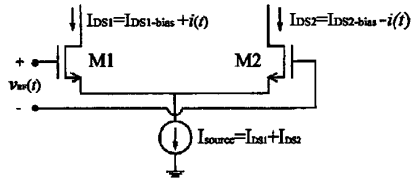

Fig.3. Input V-I converter

A. Mismatch effects on input V-I converter

Let us first consider the input V-I converter, as shown in Fig.3. It is convenient for later exposition to express V_{GS} of the transistor as a function of I_{DS}. We thus invert Eq.(1):

$$V_{GS} = f(I_{DS},\beta,\theta,V_T) = \frac{\theta}{\beta}I_{DS}\cdot\left(1+\sqrt{1+\frac{2\beta}{\theta^2 I_{DS}}}\right)+V_T \quad (4)$$

In the presence of mismatch, the values of the parameters in Eq.(4) are different for the two transistors. Using the subscripts 1 and 2 to denote parameters of the transistors, we can express Eq.(4) as a Taylor series:

$$\begin{cases} v_{GS1} = \Delta V_{GS1} = \Delta f_1(I_{DS1}) = f_1' i_1 + \frac{f_1''}{2}i_1^2 + \frac{f_1'''}{6}i_1^3 + \cdots \\ v_{GS2} = \Delta V_{GS2} = \Delta f_2(I_{DS2}) = f_2' i_2 + \frac{f_2''}{2}i_2^2 + \frac{f_2'''}{6}i_2^3 + \cdots \end{cases} \quad (5)$$

where f is the function in Eq.(4) with the subscripts denoting different parameters values of M1 and M2, f, f', f'' and f''' are the derivatives of this function respect to I_{DS}, and the number of primes denotes the order of the derivative.

Taking the difference between the expressions in Eq.(5) and noting that $v_{RF} = v_{GS1} - v_{GS2}$ and $i_1 = -i_2 = i$, we obtain the input signal v_{RF} as a function of the output current i:

$$v_{RF} = \Delta V_{GS1} - \Delta V_{GS2} = (f_1' + f_2')i + \frac{f_1'' - f_2''}{2}i^2 + \frac{f_1''' + f_2'''}{6}i^3 + \cdots \quad (6)$$

To express i in terms of v_{RF}, Eq.(6) can be rewritten as

$$i = \frac{1}{f_1' + f_2'}v_{RF} - \frac{1}{2}\frac{f_1'' - f_2''}{(f_1' + f_2')^3}v_{RF}^2 + \left[\frac{1}{2}\frac{(f_1'' - f_2'')^2}{(f_1' + f_2')^5} - \frac{1}{6}\frac{f_1''' + f_2'''}{(f_1' + f_2')^4}\right]v_{RF}^3 + \cdots \quad (7)$$

Because the mismatch in parameters is small compared with their values, we can approximate Eq.(7) by

$$i = \frac{1}{2f'}v_{RF} - \frac{1}{16}\frac{\Delta f''}{f'^3}v_{RF}^2 - \frac{1}{48}\frac{f'''}{f'^4}v_{RF}^3, \quad (8)$$

where $f' = \frac{f_1' + f_2'}{2}$, $f''' = \frac{f_1''' + f_2'''}{2}$ and $\Delta f'' = f_1'' - f_2''$.

Without transistor mismatch, $\Delta f'' = 0$. The even-order term in Eq.(8) vanishes. Only odd harmonic terms appear at the output of the V-I converter. Furthermore, as we will prove later, the ideally matched switch pairs in double-balanced mixer will also prevent even-order terms in the input stage from appearing at the output of switch stage.

Equating the first-order and second-order terms in Eq.(8), the second-order intercept point (IIP2) [6] is

$$v_{IIP2} = \frac{\frac{1}{2f'}}{\frac{1}{16}\frac{\Delta f''}{f'^3}} = \frac{8f'^2}{\Delta f''} = \frac{8f'^2}{f'''\cdot\Delta I_{DS}} = \frac{8f'^2}{f'''\cdot I_{DS}}\cdot\frac{1}{\frac{\Delta I_{DS}}{I_{DS}}} \quad (9)$$

Substituting Eq.(2) into Eq.(9), we obtain the relation between v_{IIP2} and the transistor mismatch parameters.

B. Mismatch effects on switch pair

Now let us consider the effects of mismatch on the switch pairs. Without loss of generality, consider only the left switch pair shown in Fig.1. The output of the RF V-I converter stage is $I_{DS1} = I_{DS1-bias} + i(t)$. We define the switch point of two transistors to be the point when the output differential current ($I_{DS3} - I_{DS4}$) is zero. To further simplify the analysis, assume that the circuit switches sharply. Thus, in the absence of mismatch, for positive values of the LO voltage, M3 switches ON and M4 switches OFF, and a current equal to I_{DS1} appears in the left branch. In the next half period, the current switches to the right branch. Thus, the output is a square-wave at frequency of ϖ_{LO} with no DC value, where ϖ_{LO} is the angular frequency of the LO. In the presence of mismatch, a bias voltage is needed to make the output differential current zero. This voltage arises from transistor mismatch and is time-independent if we ignore the effect of temperature. So we can say that the circuit has a DC offset voltage V_{offset} [16]. This offset voltage can be calculated by the following functions:

$$\begin{cases} V_{GS} + \Delta V = f(I_{DS},\beta+\Delta\beta,\theta+\Delta\theta,V_T+\Delta V_T) \\ V_{GS} = f(I_{DS},\beta,\theta,V_T) \end{cases} \quad (10)$$

$$V_{offset} = \Delta V \approx \frac{\partial f}{\partial \beta}\Delta\beta + \frac{\partial f}{\partial \theta}\Delta\theta + \frac{\partial f}{\partial V_T}\Delta V_T , \quad (11)$$

where $f(\bullet)$ denotes the function in (4).

Since the offset voltage arises from manufacture variations, we can characterize it statistically as follows:

$$\sigma^2_{V_{offset}} = \left(\beta \cdot \frac{\partial f}{\partial \beta}\right)^2 \sigma^2_{\frac{\Delta\beta}{\beta}} + \left(\frac{\partial f}{\partial \theta}\right)^2 \sigma^2_{\Delta\theta} + \left(\frac{\partial f}{\partial V_T}\right)^2 \sigma^2_{\Delta V_T} , \quad (12)$$

+ correlation terms

The transfer characteristic of the switch pair can thus be represented by the superposition of a periodic pulse and a square-wave as showed in Fig.4. [17].

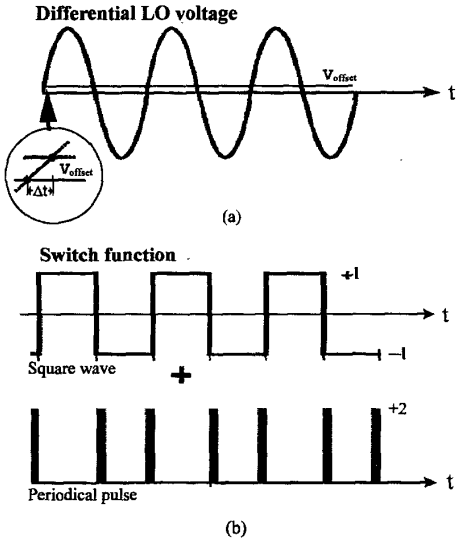

Fig.4. Mixer output current can be represented by the superposition of a periodic pulse and a square wave in the presence of offset voltage [17].

Transistor mismatch can thus be represented by a skew in the switching time Δt. It is determined by the offset voltage V_{offset} and the slope of the LO voltage S at switching time:

$$\Delta t = \frac{V_{offset}}{S} . \quad (13)$$

Using the symbols $\Pi(t)$ and $\Lambda_{\Delta t}(t)$ respectively to represent a square-wave with no DC value at an angular frequency ϖ_{LO} and a periodic pulse with pulse width Δt and an angular frequency of $2\varpi_{LO}$, and letting i_{out} to be the output current of the double-balanced mixer in Fig.1, we can write i_{out} as

$$\begin{aligned} i_{out} &= [I_{DS1-bias} + i(t)][\Pi(t) + \Lambda_{\Delta t_1}(t)] \\ &\quad - [I_{DS2-bias} - i(t)][\Pi(t) + \Lambda_{\Delta t_2}(t)] \end{aligned} \quad (14)$$

The equation can be re-written as

$$\begin{aligned} i_{out} = &\underbrace{[I_{DS1-bias} \cdot \Lambda_{\Delta t_1}(t) - I_{DS2-bias} \cdot \Lambda_{\Delta t_2}(t)]}_{\text{DC-Feedthrough}} \\ &+ \underbrace{i(t)[2\Pi(t) + \Lambda_{\Delta t_1}(t) + \Lambda_{\Delta t_2}(t)]}_{\text{mixed output signal}} \end{aligned} , \quad (15)$$

i) Feedthrough

Only the DC component of the first term in (15) affects the output of the mixer. Thus, the DC-feedthrough signal at the output of mixer is

$$\begin{aligned} I_{DC-Feedthrouh} &= I_{DS1-bias}\frac{4V_{offset1}}{T \cdot S} - I_{DS2-bias}\frac{4V_{offset2}}{T \cdot S} \\ &= \frac{4}{T \cdot S}\left[I_{DS-bias} \cdot \Delta V_{offset} - \Delta I_{DS-bias} \cdot V_{offset}\right] \\ &\approx \frac{2}{T \cdot S} I_{source} \cdot \Delta V_{offset} \end{aligned} , \quad (16)$$

where $I_{source} = 2I_{DS-bias} = I_{DS1-bias} + I_{DS2-bias}$, $\Delta I_{DS-bias} = I_{DS1-bias} - I_{DS2-bias}$, $V_{offset} = \frac{V_{offset1} + V_{offset2}}{2}$, $\Delta V_{offset} = V_{offset1} - V_{offset2}$ and T is the period of the LO. For a sine-wave LO, $T \cdot S = 2\pi \cdot (2V_{LO}) = 4\pi V_{LO}$, where V_{LO} is the amplitude of the LO and the factor of two accounts for the fact that ΔV_{offset} is compared to a differential LO signal with an amplitude of $2V_{LO}$ [12]. So we can get

$$I_{DC-feedthrough} = \frac{I_{source}}{2\pi V_{LO}} \Delta V_{offset} . \quad (17)$$

Since $V_{offset1}$ and $V_{offset2}$ are two independent random variables with the same distribution, the variance of the feedthrough gain can be calculated as

$$\begin{aligned} \sigma^2_{\frac{I_{DC-feedthrough}}{I_{source}}} &= \left(\frac{2}{T \cdot S}\right)^2 \sigma^2_{V_{offset1} - V_{offset2}} \\ &= \left(\frac{2}{T \cdot S}\right)^2 \cdot 2\sigma^2_{V_{offset}} = \frac{1}{2\pi^2 V_{LO}^2}\sigma^2_{V_{offset}} \end{aligned} . \quad (18)$$

ii) Conversion Gain

The desired output signal at the output of the mixer is the first-order term of the mixed output signal in Eq.(15)

$$\begin{aligned} i_{out-desired} = &-\frac{4}{\pi}\left[1 + \left(\frac{e^{-j\varpi\Delta t_1} - 1}{2}\right)^2 + \left(\frac{e^{-j\varpi\Delta t_2} - 1}{2}\right)^2\right] \cdot i(t), \\ \approx &-\frac{4}{\pi}\left[1 + \left(\frac{-j\varpi\Delta t_1}{2}\right)^2 + \left(\frac{-j\varpi\Delta t_2}{2}\right)^2\right] \cdot i(t) \end{aligned} \quad (19)$$

where $j = \sqrt{-1}$ and $\varpi = \varpi_{LO}$. Substituting Eq.(13) into Eq.(19), we obtain

$$\text{Gain}_{\text{switch}} = \frac{i_{out-desired}}{i} = \frac{4}{\pi}\left(1 - \frac{1}{16}\frac{V_{offset1}^2 + V_{offset2}^2}{V_{LO}^2}\right), \quad (20)$$

Using the expression for $V_{offset1}$ and $V_{offset2}$ in the prior section, the expected value of the conversion gain is

$$E_{\text{Gain}_{\text{switch}}} = \frac{4}{\pi}\left(1 - \frac{1}{8}\frac{\sigma^2_{V_{offset}}}{V_{LO}^2}\right) \quad (21)$$

iii) Gain of the second-order intermodulation (IM2)

When two close tones at ϖ_{RF1} and ϖ_{RF2} are presented at the input of RF V-I converter, the sum and the differential frequencies can be generated at the input of the switch pairs. The non-zero DC term of the mixed output signal in Eq.(15) will

transfer the differential frequencies to the output of the mixer, causing even-order distortion. The IM2 conversion gain and its variance can be calculated as

$$Gain_{IM2} = \frac{4}{T \cdot S}\left(V_{offset1} - V_{offset2}\right) = \frac{\Delta V_{offset}}{\pi V_{LO}}, \quad (22)$$

$$\sigma^2_{Gain_{IM2}} = \frac{2}{\pi^2 V_{LO}^2}\sigma^2_{V_{offset}} \quad (23)$$

C. Overall effects of Cascaded V-I Converter and Switch Pair

So far, the effects of mismatch on RF input V-I converter and switch pair has been discussed separately. To analyze the combined effects of mismatch in each stage, the second-order intermodulation product and the overall conversion gain of the cascaded stages will be examined.

First, consider the second-order intermodulation product. Using the equations we derived in prior sections, we obtain

$$\frac{i_{IM2}}{v_{RF}} = \frac{1}{16}\frac{\Delta f''}{f'^3}\cdot\frac{\Delta V_{offset}}{\pi V_{LO}} = \left(\frac{1}{16}\frac{f'''}{f'^3}\frac{I_{DS-bias}}{\pi V_{LO}}\right)\left(\frac{\Delta I_{DS-bias}}{I_{DS-bias}}\right)\Delta V_{offset} \quad (24)$$

The variance of second-order intermodulation transconductance is

$$\sigma^2_{\frac{i_{IM2}}{v_{RF}}} = 2\left(\frac{1}{16}\frac{f'''}{f'^3}\frac{I_{DS-bias}}{\pi V_{LO}}\right)^2 \sigma^2_{\frac{\Delta I_{DS-bias}}{I_{DS-bias}}}\sigma^2_{V_{offset}}. \quad (25)$$

The overall conversion gain of the desired signal is

$$Gain = \frac{i_{out-desired}}{v_{RF}} = Gain_{switch}\cdot\frac{1}{2f'} = \frac{2}{\pi}\left(1 - \frac{1}{16}\frac{V^2_{offset1} + V^2_{offset2}}{V^2_{LO}}\right)\cdot\frac{1}{f'} \quad (26)$$

Similar to the calculation in the prior section, the expected value of conversion gain is

$$E_{Gain} = \frac{2}{\pi}\left(1 - \frac{1}{8}\frac{\sigma^2_{V_{offset}}}{V^2_{LO}}\right)\cdot\frac{1}{f'}. \quad (27)$$

For a mixer with minimum-length transistors in a 0.8-μm technology, the expected loss in gain is less than 5%. This effect can be alleviated by decreasing I_{source}, increasing V_{LO}, or using larger size transistors in mixer.

IV. CONCLUSIONS

Processing-induced mismatch in CMOS double-balanced mixer can cause adverse effects such as DC feedthrough, decrease in IIP2, and the reduction in conversion gain. A relation between the variances of the mismatch parameters and the mismatch effects on the mixer has been presented. This model can provide estimates of the needed degree of transistor matching.

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