

# Implementation of CMRC on HBT Power Amplifier for WCDMA Application

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## Abstract

An InGaP/GaAs heterojunction bipolar transistor (HBT) is developed. By using this HBT, a power amplifier is designed for WCDMA user equipment, band-1 power class-2 application. The HBT power amplifier demonstrates a maximum output power ( $P_{out}$ ) of 29.4dBm and a PAE of 48% at the frequency of 1.95GHz. When it operates in WCDMA standard, it achieves a  $P_{out}$  of 27dBm and a PAE of 32.4%. The Adjacent Channel Leakage power Ratio (ACLR) is -33dBc. To further improve the PAE, ACLR and IM3 performance, a CMRC circuit has been implemented on the HBT amplifier. The effect of CMRC on PAE and ACLR is investigated using a low power HBT amplifier. The results show that the ACLR can be improved by the CMRC.

## 1. Introduction

Standby and operating times are the key concerns for mobile devices. In this regard, it is important to note that power amplifier circuits consume most of the power from the battery package. As power amplification is the last stage in the uplink circuit, it should be designed to be linear operating for less power dissipation and less interference to users' surroundings.

InGaP/GaAs heterojunction bipolar transistor (HBT) is a kind of device which has the unique features of high linearity and high efficiency. These features make HBT more suitable for mobile devices applications. High efficiency HBT MMIC with a PAE of 40% and a  $P_{out}$  of 28dBm [1] and high linearity HBT amplifier module with an output power of 26.3 dBm and a PAE of 50% and ACLR of -35dBc [2] have been developed for WCDMA mobile products.

Compact Microstrip Resonance Cell is widely used for filtering, harmonics cancellation [3] and oscillator circuits [4]. It has been applied on SiGe power amplifier [5], which operates up to 14dBm. In this experiment, it is the first time that Compact Microchip Resonance Cell has been applied to HBT power amplifier. It is used as a linearizer for the amplifier.

This HBT amplifier is designed for WCDMA Band-1 power class-2 user equipment. The original circuit will consume over 400mA at low output power, the PAE is only 4% to 10%. This paper proposes the idea that the biasing current of the circuit during low power operation is reduced to half, with Compact Microstrip Resonance Cell (CMRC) implemented to the amplifier so as to improve the PAE and ACLR.

## 2. Device structure and process description

InGaP/GaAs HBTs were grown by MOCVD on a GaAs substrate. The device structure consists of a 600 nm  $n^+$ -GaAs sub-collector, a 700 nm  $n^-$ -GaAs collector, a 100 nm  $p^+$ -GaAs base, a 40 nm  $n$ -In<sub>0.5</sub>Ga<sub>0.5</sub>P emitter layer, and a 150 nm  $n^+$ -GaAs emitter cap layer, a 50 nm  $n^+$ -In<sub>x</sub>Ga<sub>1-x</sub>As graded layer ( $x$  from 0 to 0.6), and a 50 nm  $n^+$ -In<sub>x</sub>Ga<sub>1-x</sub>As contact layer ( $x=0.6$ ). The HBTs were fabricated using a non self-aligned process. Standard photolithography and chemical wet selective etching were used in the device processing. The InGaP layer was etched using a solution of dilute HCl and the InGaAs and GaAs layers were etched with H<sub>3</sub>PO<sub>4</sub>: H<sub>2</sub>O<sub>2</sub>: H<sub>2</sub>O. Emitter and base metal are Ti/Pt/Au and collector metal is AuGe/Ni/Au. A thin depleted InGaP ledge with a length of 0.8  $\mu$ m was used as a passivation layer for the extrinsic base surface to reduce the surface recombination current. To reduce thermal resistance, the substrates were thinned to 100  $\mu$ m and a gold plated heat sink structure was used. Figure 1 shows the HBT device structure.

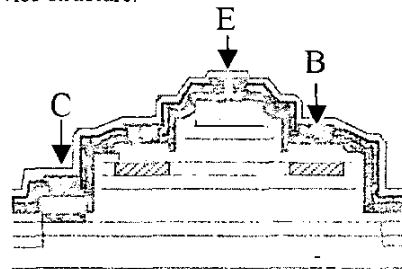


Fig. 1 HBT device structure

### 3. Circuitry Design

The transistor is a single stage with 4 1/4W cells consisting of 104 fingers [6]. The emitter area is  $3494\mu\text{m}^2$ . It is mounted on RT/Duroid PCB with dielectric constant 2.33 and thickness 0.254mm. The amplifier is biased at  $V_{CE} = 3.5\text{V}$  and the layout is designed to an optimized matching network. Figure 2 shows the configuration of the amplifier circuit.

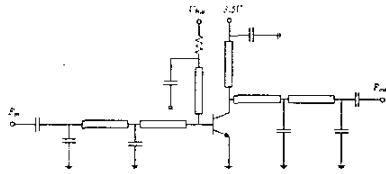


Figure 2 Schematic of HBT amplifier

The PAE, gain and  $P_{\text{out}}$  are shown in Figure 3, which are tested with 1.95GHz pure tone. The PAE is measured as 37.65% at 28dBm output. Signal with symbol rate 3,840,000 Sym/s and QPSK modulation is used to test the amplifier in WCDMA mode. Figure 4 shows the PAE, channel power and ACLR versus input power in WCDMA mode.

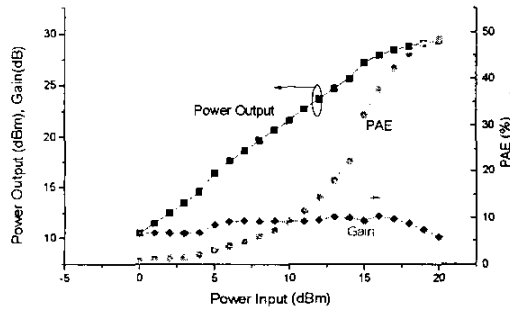


Figure 3 Power Added Efficiency, Power output and Power Gain measurement for Pure tone

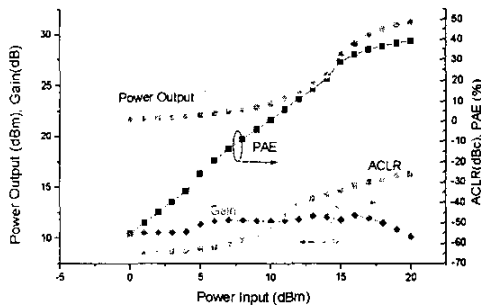


Figure 4 PAE and Channel Power of WCDMA signal

The Adjacent Channel Leakage Power Ratio (ACLR) is measured with channel bandwidth set to 4.096MHz and resolution bandwidth set to 30KHz. When the output power is 27dBm, the amplifier yields a PAE of 30% and ACLR of -33dBc.

The linearity of the amplifier is evaluated by injecting two pure tones with 5 MHz spacing to the amplifier. The IM3 product is measured in linear operation region of the circuit. The OIP3 is found as 45.7dBm

When the amplifier is operating in lower power output range, the PAE will also be lower compared with the high power output section. One more power amplifier is used for low power operation. This idea has been evaluated and has demonstrated significant improvement to PAE in low transmission power. In this design, there are two approaches: 1) alternate amplifier for lower power output, and 2) alternate path with CMRC and biasing current of the same amplifier is reduced to half in low power range. In this document, the second approach will be evaluated. There is an increment of PAE, and CMRC is implemented at the input port of the amplifier for compensating the degradation of linearity. The circuit block and structure of CMRC are shown in Figure 5 and 6 respectively.

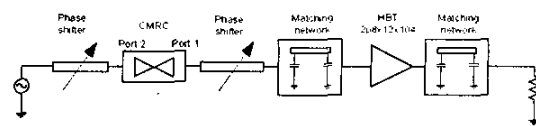


Figure 5 HBT amplifier with Compact Microstrip Resonance Cell



Figure 6 Structure of CMRC

The input return loss of the CMRC at fundamental frequency is 14dB and less than 0.5dB at second harmonic frequencies. The insertion loss at fundamental frequency is less than 0.4dB. The second harmonics are within the stop band of CMRC. The phase shifter is used to tune the reflection of second harmonics from the amplifier until it cancels the second harmonics component generated from the power amplifier. Figure 7 shows the frequency response of CMRC.

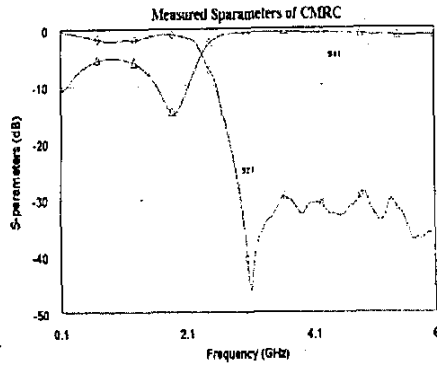


Figure 7 Measured S-parameters of CMRC structure

### 3. Result

Figure 8 shows that the gain compression and PAE of the amplifier is improved at the saturation region. Figure 9 shows that the amplifier with CMRC has average 3 dB lower ACPR and IM3 products compared with the original circuit. When the output power reaches 22dBm, ACPR reduces from -32.6dBc to -36.2dBc, and PAE increases from the original circuit 9.7% to 16.5%.

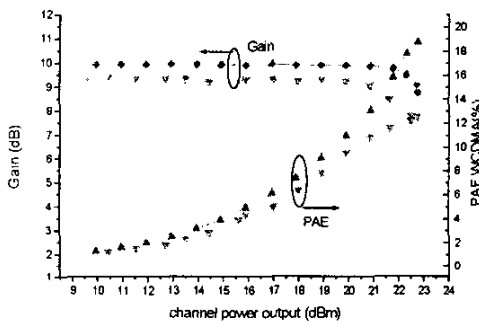


Figure 8 Increment of PAE of linearized circuit

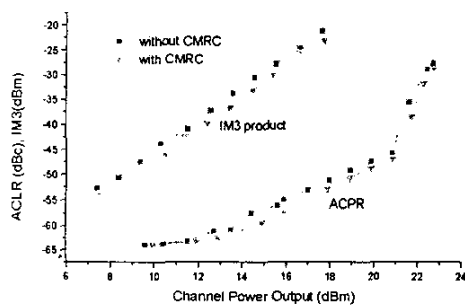


Figure 9 Adjacent channel power measurement and IM3 compare between CMRC circuit with original circuit

### 4. Summary

An amplifier circuit for WCDMA Band-1 power class-2 user equipment is presented. Figure 10 summarizes the PAE of the two operating sections of output power. During low output power operation, the biasing current is reduced to maintain a high PAE. CMRC is implemented in this mode and it linearizes the amplifier. This path of amplification is operating up to 22dBm with PAE of 16% and ACLR of -34dBc. For power output above this power range, the original path is used instead. It can deliver 27dBm with PAE of 32.4% and ACLR of -33dBc. The measurement result shows that this approach can help maintain a high PAE for most of the operating power.

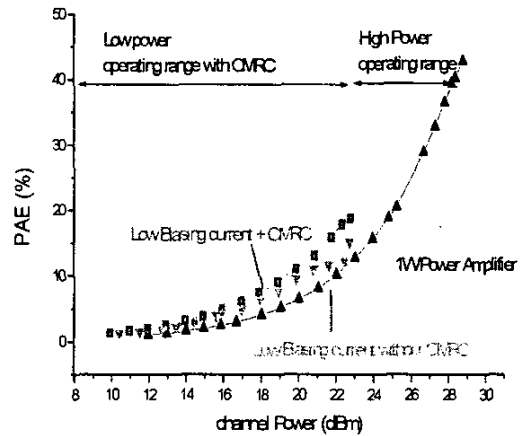


Figure 10 PAE of Power amplifier circuit with two output power ranges

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