

Influence of Si Nanocrystal Distributed in the Gate Oxide on the MOS Capacitance

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Abstract—In this paper, the authors have studied the influence of silicon nanocrystal (nc-Si) distributed in the gate oxide on the capacitance for the circumstances that the nc-Si does not form conductive percolation tunneling paths connecting the gate to the substrate. The nc-Si is synthesized by Si-ion implantation. The effective dielectric constant of the gate oxide in the nc-Si distributed region is calculated based on a sublayer model of the nc-Si distribution and the Maxwell–Garnett effective medium approximation. After the depth distribution of the effective dielectric constant is obtained, the MOS capacitance is determined. Two different nc-Si distributions, i.e., partial and full nc-Si distributions in the gate oxide, have been considered. The MOS capacitance obtained from the modeling has been compared to the capacitance measurement for a number of samples with various gate-oxide thicknesses, implantation energies and dosages, and an excellent agreement has been achieved for all the samples. A detailed picture of the influence of implantation energy and implantation dosage on the MOS capacitance has been obtained.

Index Terms—Dielectric constant, MOS capacitance, silicon nanocrystal.

I. INTRODUCTION

RESEARCH on silicon nanocrystals (nc-Si) embedded in the gate oxide of a MOS structure has been carried out intensively over the past decade due to the potential applications of nc-Si in memory device applications [1]–[12]. One of the promising techniques to incorporate nc-Si into SiO₂ is Si-ion implantation followed by high-temperature annealing. With this technique, the fabrication is fully compatible with the mainstream CMOS process, and the distribution of nc-Si in the gate oxide can be easily controlled. When the nc-Si is embedded in the SiO₂ film, the dielectric constant of the film will be different from that of pure SiO₂ film. Therefore, for memory devices with the nc-Si embedded in the gate oxide, the inclusion of the nc-Si will definitely affect the MOS capacitance as a result of the change in the dielectric

constant of the gate oxide. The effect of the nc-Si on the MOS capacitance has been observed experimentally [13]. The change in the MOS capacitance due to the influence of the nc-Si will then affect the electrical characteristics of the device. Obviously, a precise knowledge on the influence of the nc-Si on the MOS capacitance is very useful to the design and modeling of the memory devices. In particular, an approach to calculate the MOS capacitance, with the nc-Si distribution in the gate oxide taken into account, is highly desirable. However, a quantitative study on the influence of nc-Si on the MOS capacitance is still lacking.

In the present paper, we have developed an approach to the calculation of the MOS capacitance for any nc-Si distribution in the gate oxide, for the circumstances that the nc-Si does not form conductive percolation tunneling paths connecting the gate to the substrate. The approach is based on the calculation of the effective dielectric constant of the gate oxide in the nc-Si distributed region with a sublayer model of nc-Si distribution and the Maxwell–Garnett effective medium approximation (EMA). The MOS capacitance calculated using this approach has been compared to the capacitance measurement for a number of samples with various gate-oxide thicknesses, implantation energies and dosages, and an excellent agreement has been achieved for all the samples. A detailed picture of the influence of implantation energy and implantation dosage on the MOS capacitance has been obtained.

II. MODELING

The distribution of the nc-Si in the gate oxide can be obtained from the stopping and range of ions in matter (SRIM) simulation. There are two cases of nc-Si distribution in the gate oxide: partial and full distributions in the gate oxide. For the partial distribution, the oxide can be divided into two regions: the nc-Si distributed region and the pure SiO₂ region (i.e., without nc-Si). One example of the partial distribution, which is achieved with the ion implantation energy of 2 keV for a 30-nm gate oxide, is shown in Fig. 1(a). For the full distribution, nc-Si is distributed in the entire gate oxide. Note that for the full distribution, the nc-Si concentration should not be too high to avoid the formation of conductive percolation tunneling paths connecting the gate to the substrate. Fig. 1(b) shows one example of the full distribution achieved with the ion implantation energy of 8 keV for a 30-nm gate oxide. The SRIM simulation shows that for a 30-nm gate oxide, the full distribution can be achieved with implantation energy higher than 7 keV.

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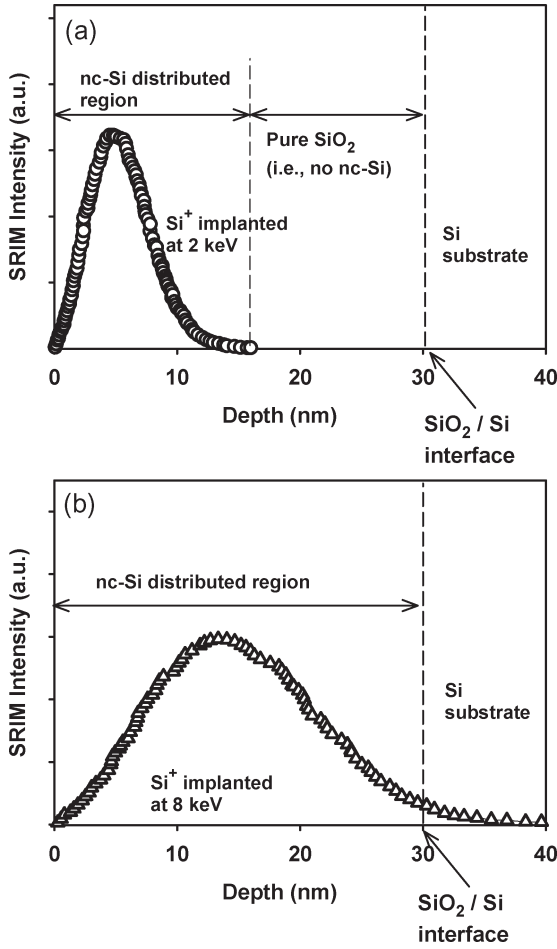


Fig. 1. Distribution of nc-Si in a 30-nm gate oxide obtained from SRIM simulation. (a) Partial distribution under the ion implantation energy of 2 keV. (b) Full distribution under the implantation energy of 8 keV.

From the nc-Si SRIM profile, we can obtain the depth distribution of the nc-Si volume fraction in the SiO₂. The volume fraction can be expressed as

$$v(x) = \frac{QI(x)}{N_{\text{Si}} \int_0^{d_{\text{max}}} I(x) dx} \quad (1)$$

where Q is the dosage of implanted Si ions, N_{Si} is the silicon density, d_{max} is the maximum depth of the Si-implantation profile, i.e., the width of the nc-Si distributed region. Note that d_{max} is equal to the gate-oxide thickness for the case of full distribution, and $I(x)$ is the Si SRIM intensity. The information of the volume fraction is required for the calculation of the effective dielectric constant of SiO₂ containing nc-Si, as discussed below.

As the nc-Si volume fraction varies with the depth in the oxide, the effective dielectric constant of the oxide is not uniform and should vary with the depth also. The nc-Si distributed region [note that its width is equal to d_{max} of (1)] can be virtually divided into m ($m = 30, 40,$ and 100 for $30, 40,$ and 100 nm of SiO₂ thickness, respectively, in the present study) sublayers with equal thickness of (d_{max}/m) nm (namely: sublayer 1, sublayer 2, ..., sublayer m) starting from the surface to the depth of d_{max} . The nc-Si volume fraction within a sublayer is

approximately constant. Thus, the effective dielectric constant ε_i ($i = 1, 2, \dots, m$) of the i th sublayer can be calculated with the Maxwell-Garnett EMA, as given by [14]

$$\frac{\varepsilon_i - \varepsilon_{\text{SiO}_2}}{\varepsilon_i + 2\varepsilon_{\text{SiO}_2}} = v_i \frac{\varepsilon_{\text{nc-Si}} - \varepsilon_{\text{SiO}_2}}{\varepsilon_{\text{nc-Si}} + 2\varepsilon_{\text{SiO}_2}} \quad (2)$$

where v_i ($i = 1, 2, \dots, m$) is the volume fraction of the nc-Si in the i th sublayer, $\varepsilon_{\text{nc-Si}}$ is the static dielectric constant of nc-Si, and $\varepsilon_{\text{SiO}_2}$ is the dielectric constant of pure SiO₂.

The screening dielectric constant of nc-Si can be theoretically calculated with the formula below [15]

$$\varepsilon_{\text{nc-Si}}(D) = 1 + \frac{\varepsilon_b - 1}{1 + \left(\frac{1.38}{D}\right)^{1.37}} \quad (3)$$

where ε_b is the dielectric constant of bulk crystalline silicon (note that in [15], the two constants 1.37 and 1.38 used in (3) are obtained under the assumption of $\varepsilon_b = 11.4$). This ε_b value is slightly different from the widely used value 11.9 [16], and D is the diameter of nc-Si in the unit of nanometer. As discussed later, the mean nc-Si size is 4.5 nm as determined from the X-ray diffraction (XRD) measurement. The $\varepsilon_{\text{nc-Si}}$ calculated with (3) is 9.7 under the assumption of $D = 4.5$ nm. This $\varepsilon_{\text{nc-Si}}$ value is consistent with that from the optical study reported in [17]. Most importantly, the calculated MOS capacitance based on this $\varepsilon_{\text{nc-Si}}$ value is in excellent agreement with the measured capacitance, indicating that the $\varepsilon_{\text{nc-Si}}$ value is correct. The details will be discussed later.

After determining the dielectric constant of the nc-Si, the effective dielectric constant ε_i ($i = 1, 2, \dots, m$) of each sublayer of the nc-Si distributed region can be calculated with (2). With the depth distribution of the effective dielectric constant taken into account, the MOS capacitance in the accumulation regime is calculated, as described below. For the case of partial nc-Si distribution in the gate oxide, the MOS capacitance (C) per unit area can be expressed as

$$\frac{1}{C} = \sum_{i=1}^m \left[\frac{m\varepsilon_i\varepsilon_0}{d_{\text{max}}} \right]^{-1} + \left[\frac{3.9 \times \varepsilon_0}{T_{\text{oxide}} - d_{\text{max}}} \right]^{-1} \quad (4)$$

where T_{oxide} is the gate-oxide thickness, and ε_0 is the permittivity in vacuum. On the other hand, for the case of full nc-Si distribution in the gate oxide, the MOS capacitance is given by

$$\frac{1}{C} = \sum_{i=1}^m \left[\frac{m\varepsilon_i\varepsilon_0}{T_{\text{oxide}}} \right]^{-1} \quad (5)$$

It should be pointed out that the above calculations of the MOS capacitance [i.e., (4) and (5)] are valid only for the circumstances that the nanocrystals themselves are not charged and discharged in response to the small ac signal applied during a capacitance measurement. If there is a high concentration of nanocrystals distributed throughout the gate oxide, these nanocrystals can form conductive percolation tunneling paths

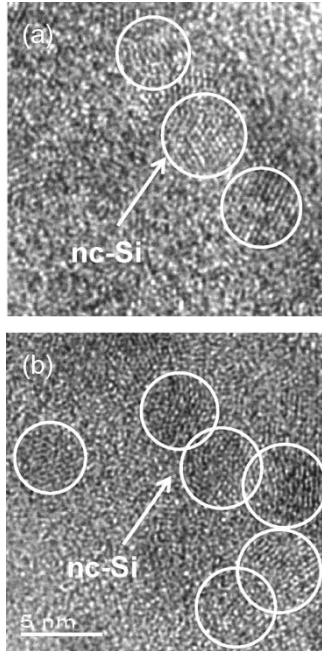


Fig. 2. TEM image of nc-Si embedded in a 30-nm gate oxide. (a) Partial distribution under the implantation energy of 2 keV. (b) Full distribution under the implantation energy of 10 keV.

connecting the substrate to the gate [18]. Thus, they can be charged and discharged easily under the influence of the ac signal. In this case, the nanocrystal acts like a capacitor and, therefore, the MOS capacitance should be calculated based on an equivalent circuit that takes the contribution of the nanocrystal capacitance into account [18].

III. EXPERIMENTAL

The gate oxide was thermally grown to 30, 40, and 100 nm, respectively, on p-type (100) Si wafers in dry oxygen at 950 °C. Si⁺ ions with a dosage ranging from 3×10^{14} to 8×10^{16} cm⁻² were then implanted to the gate oxide at various implantation energies from 2 to 28 keV. Thermal annealing was carried out at 1000 °C in N₂ ambient for 1 h to induce nc-Si formation for all samples. Fig. 2 shows the cross-sectional transmission electron microscopy (TEM) images of nc-Si embedded in the gate oxide for both partial nc-Si distribution [Fig. 2(a)] and full nc-Si distribution [Fig. 2(b)]. For both cases, from the TEM measurement, the nc-Si size is found to be $\sim 4 - 5$ nm for all the samples used in the present study. The average size of nc-Si can also be determined from the full width of half maximum (FWHM) of the Bragg peak after correction for instrumental broadening in the XRD measurement [14], [19]. Fig. 3 shows an example of the XRD measurement. The mean size of the nc-Si obtained from the XRD measurement is 4.5 ± 0.3 nm for all the samples, and it is found to be insensitive to the annealing temperature/time. For the capacitance measurement, aluminum was deposited and patterned to form the top and bottom electrodes. Capacitance–voltage (*C–V*) measurement was performed at the frequency of 1 MHz with an HP4284A LCR meter.

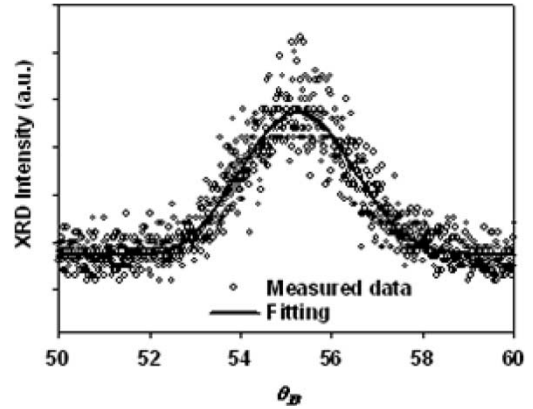


Fig. 3. Example of XRD measurement of nc-Si embedded in the gate oxide. The gate-oxide thickness and the implantation energy of the sample used in this measurement are 30 nm and 2 keV, respectively.

IV. RESULTS AND DISCUSSIONS

To verify the above modeling approach and to check the correctness of the $\epsilon_{\text{nc-Si}}$ ($= 9.7$, which corresponds to the nc-Si size of 4.5 nm) value, MOS capacitance measurement under a strong accumulation has been carried out on many samples with various gate-oxide thicknesses, implantation energies, and dosages. Table I summarizes the comparison between the measured capacitance and the capacitance calculated using $\epsilon_{\text{nc-Si}} = 9.7$, with (4) for the partial distribution or (5) for the full distribution. The agreement between the measurement and the calculation can be easily described by the ratio $R = \text{calculated capacitance}/\text{measured capacitance}$. As can be seen in the table, the R value is very close to one (in the range from 0.982 to 1.002) for all the samples. This indicates that the calculation is in excellent agreement with the measurement. On the other hand, we have also compared the measured capacitance with the capacitances calculated with $\epsilon_{\text{nc-Si}} = 9.7$ and $\epsilon_{\text{nc-Si}} = 11.9$ (the value of the bulk crystalline silicon) for various implantation energies, as shown in Fig. 4. It is evident from Fig. 4 that $\epsilon_{\text{nc-Si}} = 9.7$ can yield an excellent agreement between the calculation and the measurement while such an agreement cannot be achieved with $\epsilon_{\text{nc-Si}} = 11.9$. Therefore, it can be concluded that both the above modeling approach and the $\epsilon_{\text{nc-Si}} (= 9.7)$ value are reliable and accurate.

Fig. 4 also shows the influence of implantation energy on the MOS capacitance. The capacitance is calculated at various implantation energies ranging from 1 to 11 keV for the fixed implantation dosage of 1×10^{16} cm⁻² and the gate-oxide thickness of 30 nm. According to the SRIM output, for a 30-nm gate oxide, the partial distribution corresponds to the implantation energies lower than 7 keV, while the full distribution is achieved with implantation energies higher than 7 keV. For the partial distribution, as the implantation energy increases, the width (d_{max}) of the nc-Si distributed region increases, but the effective dielectric constant ϵ_i ($i = 1, 2, \dots, m$) decreases as the nc-Si volume fraction (v_i) decreases when d_{max} increases for a constant implantation dosage. Thus, the overall effect of implantation energy on the MOS capacitance for the partial distribution is that the MOS capacitance first decreases with the implantation energy and then it

TABLE I
COMPARISON BETWEEN THE MEASURED AND CALCULATED MOS CAPACITANCE FOR VARIOUS SAMPLES. THE CALCULATION IS BASED ON (4) FOR THE PARTIAL DISTRIBUTION OR (5) FOR THE FULL DISTRIBUTION

nc-Si distribution	SiO ₂ thickness (nm)	Implantation energy (keV)	Dosage (cm ⁻²)	Measured capacitance (F/m ²)	Calculated capacitance (ε _{nc} =9.7) (F/m ²)	$R = \frac{\text{calculated cap.}}{\text{measured cap.}}$
Partial distribution	30	2	1×10 ¹⁶	1.209×10 ⁻³	1.209×10 ⁻³	1.000
	30	5	1×10 ¹⁶	1.211×10 ⁻³	1.211×10 ⁻³	1.000
	100	28	8×10 ¹⁶	3.907×10 ⁻⁴	3.913×10 ⁻⁴	1.002
Full distribution	30	8	3×10 ¹⁴	1.153×10 ⁻³	1.153×10 ⁻³	1.000
	30	8	2×10 ¹⁵	1.169×10 ⁻³	1.163×10 ⁻³	0.995
	30	8	1×10 ¹⁶	1.209×10 ⁻³	1.21×10 ⁻³	1.001
	30	10	3×10 ¹⁶	1.335×10 ⁻³	1.328×10 ⁻³	0.995
	40	18	5×10 ¹⁶	1.033×10 ⁻³	1.014×10 ⁻³	0.982

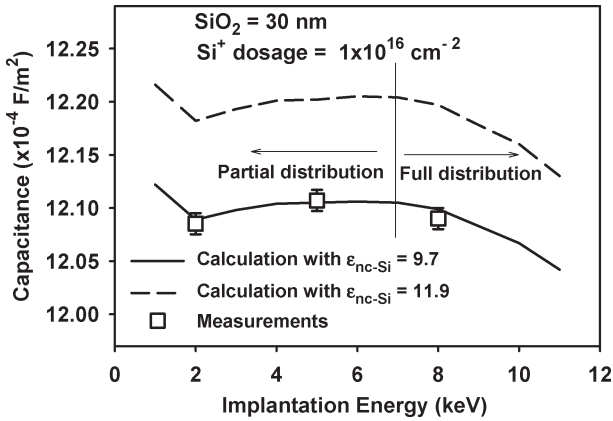


Fig. 4. Influence of Si⁺ implantation energy on the MOS capacitance. The gate-oxide thickness is 30 nm, and the implantation dosage is 1 × 10¹⁶ cm⁻².

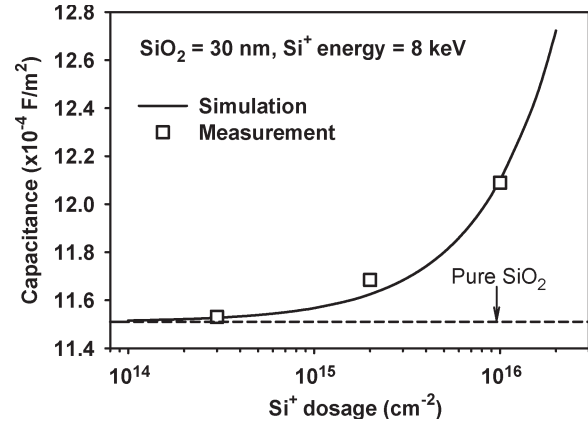


Fig. 5. Influence of Si⁺ dosage on the MOS capacitance. The gate-oxide thickness is 30 nm, and the implantation energy is 8 keV.

increases slowly when the energy is larger than ~ 2 keV, as shown in Fig. 4. For the full distribution, when the implantation energy is larger than 7 keV, some of the Si ions are implanted into the Si substrate and, thus, the effective dielectric constant ε_i (i = 1, 2, . . . , m) decreases as the nc-Si volume fraction (v_i) decreases with the implantation energy. Therefore, as given by (5), the MOS capacitance decreases with the implantation energy. Such a picture is also shown in Fig. 4.

Fig. 5 shows the MOS capacitance calculated with (5) as a function of the implantation dosage. The gate-oxide thickness is 30 nm, the implantation energy is fixed at 8 keV, which corresponds to the full distribution, and the ε_{nc-Si} value used is 9.7. For comparison, the measured MOS capacitances for the implantation dosages of 3 × 10¹⁴, 2 × 10¹⁵, and 1 × 10¹⁶ cm⁻² are also included in Fig. 5. As can be seen in the figure, there is a good agreement between the calculation and the measurement. Fig. 5 shows that the MOS capacitance increases with the implantation dosage, and the increase becomes significant when the dosage is higher than ~ 3 × 10¹⁴ cm⁻². The increase of the MOS capacitance is due to the increase of the effective

dielectric constant as a result of the increase in the nc-Si volume fraction with the dosage.

It has been clear from the above discussions that the increase in the MOS capacitance is actually due to the increase in the effective dielectric constant of the gate oxide as a result of the introduction of the nc-Si into the gate oxide. As the nc-Si volume fraction is a function of the depth, the effective dielectric constant also varies with the depth. We have calculated the depth distribution of the effective dielectric constant in the gate oxide based on (2). Fig. 6 shows the effective dielectric constant as a function of the depth in a 30-nm gate oxide for the partial distribution [Fig. 6(a)] and the full distribution [Fig. 6(b)]. For the case of partial distribution, the sample was implanted with 1 × 10¹⁶ cm⁻² of Si⁺ at 2 keV. There is a large increment of 1.12 in the effective dielectric constant at the peak position of the nc-Si distribution as compared to the dielectric constant of pure SiO₂. The effective dielectric constant is the same as the dielectric constant (3.9) of pure SiO₂ when the depth is larger than ~ 15 nm as there is no nc-Si in the region. For the case of full distribution, the sample was implanted with 1 × 10¹⁶ cm⁻² of Si⁺ at 8 keV. The effective dielectric constant at the peak

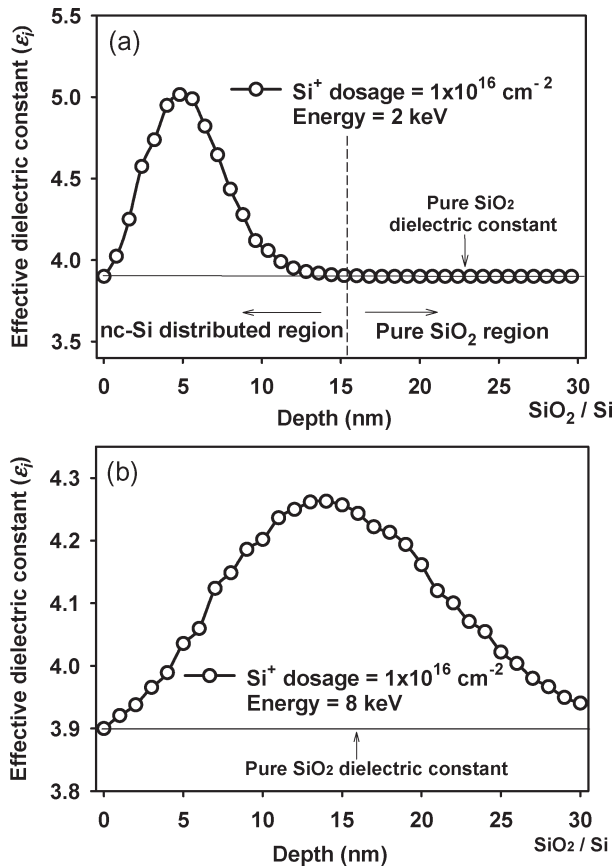


Fig. 6. Depth distribution of the effective dielectric constant of the gate oxide. (a) Partial distribution under the implantation energy of 2 keV. (b) Full distribution under the implantation energy of 8 keV. For both cases, the gate-oxide thickness is 30 nm, and the implantation dosage is $1 \times 10^{16} \text{ cm}^{-2}$.

position of the nc-Si distribution is larger than the dielectric constant of pure SiO_2 by 0.36. For both the partial and full distributions, the depth distribution of the effective dielectric constant follows the nc-Si distribution approximately.

V. CONCLUSION

In this paper, nc-Si embedded in the gate oxide is synthesized by Si-ion implantation. The influence of nc-Si distribution in the gate oxide on the MOS capacitance has been investigated through modeling and experiment for the circumstances that the nc-Si does not form conductive percolation tunneling paths connecting the gate to the substrate. The nc-Si volume fraction as a function of the depth in the gate oxide is calculated from the SRIM simulation. With the nc-Si volume fraction obtained, the effective dielectric constant of the gate oxide in the nc-Si distributed region can be calculated based on a sublayer model and the Maxwell-Garnett EMA. After the depth distribution of the effective dielectric constant is obtained, the MOS capacitance is determined. Two different nc-Si distributions, i.e., partial and full nc-Si distributions in the gate oxide, have been considered. MOS capacitance measurement has been carried out on many samples with various gate-oxide thicknesses, implantation energies, and dosages to verify the modeling of the MOS capacitance. An excellent agreement between the measurement and the modeling has been achieved.

A detailed picture of the influence of the implantation energy and the implantation dosage on the MOS capacitance has been obtained. In addition, the depth distribution of the effective dielectric constant of the gate oxide is also determined for the two nc-Si distributions.

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