Si Ion-Induced Instability in Flatband Voltage of Si+-Implanted Gate Oxides

C. Y. Ng, T. P. Chen, L. Ding, Q. Chen, Y. Liu, P. Zhao, Ampere A. Tseng, and S. Fung

Abstract—Effect of the trapped Si ions in a 30-nm gate oxide implanted with Si+ at a very low energy (1.3 keV) on the flatband voltage after various thermal annealing has been examined. For the annealing at 700 °C for 20 min, although only 0.1% of the implanted Si ions remained, it can cause a flatband voltage shift of -21.3 V, and the flatband voltage shift reduces with time under a negative gate voltage showing neutralization of the trapped ions by the injected electrons from the gate. However, the annealing at 900 °C for 20 min has reduced the number of the remaining ions to the lowest limit corresponding to a flatband voltage shift of -0.1 V, and the application of the negative voltage does not change the flatband voltage. A higher annealing temperature or a longer annealing time does not show further improvement, suggesting that the annealing at 900 °C for 20 min is sufficient for eliminating the effect of the trapped ions.

Index Terms—Annealing, flatband voltage, low energy ion beam, silicon nanocrystal (nc-Si).

I. INTRODUCTION

Recently, the memory application of Si nanocrystals (nc-Si) embedded in SiO_2 films has attracted a great interest [1]–[6]. One of the promising techniques for the incorporation of nc-Si in SiO_2 films is Si ion implantation into SiO_2 films grown by thermal oxidation of a Si substrate. With this technique, nc-Si with a size less than ~ 5 nm can be formed by subsequent thermal annealing in the Si-rich $SiOx (x < 2)$ films resulting from the Si ion implantation [7]. The memory effect of nc-Si embedded in SiO_2 thin films synthesized with low to very-low energy Si+ implantation followed by subsequent annealing has been demonstrated by several research groups [5], [8]–[10]. Different annealing processes including annealing temperature and annealing time have been reported in different studies [10]–[12]. Now, there is a question concerning the Si ions trapped in the SiO_2 matrix. Although the Si ions can be removed by a high-temperature annealing, there may be still some Si ions remaining if the annealing temperature is not high enough or annealing time is not long enough. The remaining Si ions affect the flatband voltage, and they can cause the instability in the flatband voltage as the Si ions can be neutralized by the injected electrons during the memory operation. On the other hand, although increasing the annealing temperature and prolonging the annealing time can eliminate the ions, too much thermal budget is harmful and, thus, an optimized annealing process is required. To the best of our knowledge, currently, there are no detailed studies reported on the remaining Si ions and their effect on the performance and the stability of the memory devices. In the present work, we have conducted a study on the annealing effect on the flatband voltage as well as on the instability of the flatband voltage due to the remaining Si ions.
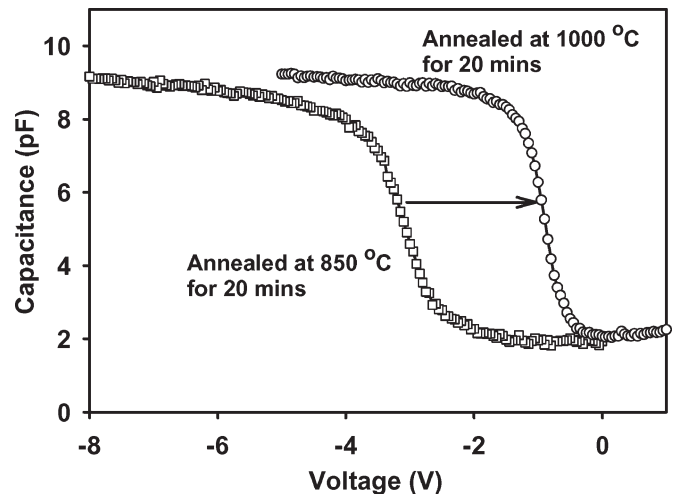
Fig. 1. Comparison of the C–V characteristics between two annealing temperatures (850 °C and 1000 °C). The annealing time is 20 min for both samples.

II. DEVICE FABRICATION AND MEASUREMENT

Thirty-nanometer SiO_2 thin film was thermally grown in dry oxygen at 950 °C on a boron-doped p-type Si(100) wafer. Si+ ions with a dose of 8×10^{16} cm^{-2} were then implanted into the SiO_2 thin films at the energy of 1.3 keV. Thermal annealing was carried out in N_2 ambient at various annealing temperatures for different annealing times. The peak of Si concentration is found at the depth of about 5 nm as obtained from the secondary ion-mass spectroscopy (SIMS) measurement and the stopping and range of ions in matter (SRIM) simulation. The annealing experiments were carried out with either a constant annealing time or a constant annealing temperature. For the former case, the annealing time is set at 20 min and the annealing temperature varies from 500 to 1100 °C. For the latter case, the annealing temperature is set at 1000 °C and the annealing time varies from 20 to 100 min. As-implanted (no annealing) sample is also included in this study. Platinum thin films were deposited and patterned to form the top and bottom electrodes. Capacitance–voltage (C–V) measurements were performed at the frequency of 1 MHz with an HP4284A LCR meter while current–voltage (I–V) measurements were conducted at room temperature with a Keithley 4200 semiconductor characterization system.

III. RESULTS AND DISCUSSIONS

As typical examples, the C–V characteristics of two different samples annealed at 850 and 1000 °C, respectively, for 20 min, are shown in Fig. 1. The C–V curves were obtained by sweeping the voltage to the negative direction (i.e., from the depletion to the accumulation). The two samples show a flatband voltage difference of ~ 2.3 V. This indicates that thermal annealing has a strong impact on the flatband voltage. The flatband voltage of the sample annealed at 850 °C is more negative than that of the sample annealed at 1000 °C. This shows that thermal annealing leads to the reduction of positive charges trapped in the SiO_2 matrix. The positive charges are the Si ions that are trapped in the SiO_2 during the Si-ion implantation. They can be released by a high-temperature annealing.

The effect of the Si ions on the flatband voltage and the reduction of the Si ions by annealing are further evident in Fig. 2. Fig. 2 shows the initial flatband voltage shift as a function of annealing temperature
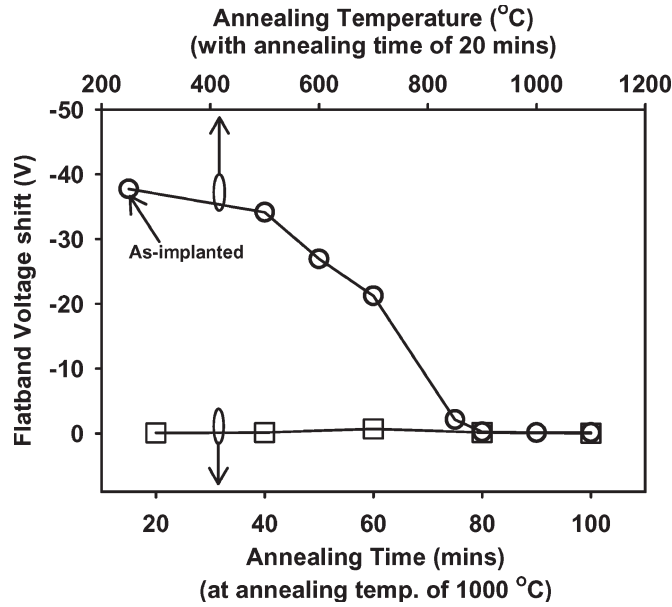
Fig. 2. Flatband voltage shift as a function of both annealing temperature and annealing time.

Fig. 3. Number of trapped Si ions as a function of both annealing temperature and annealing time.

and annealing time. The flatband voltage shift (δv_{fb}) is measured with respect to the flatband voltage of a 30-nm pure SiO_2 sample. Note that in this figure, the "as-implanted" samples have also experienced some thermal annealing (~ 250 °C for ~ 20 min) during the deposition of top and bottom platinum electrodes. As shown in this figure, the as-implanted sample has the largest negative flatband voltage shift (~ -38 V), while the flatband voltage shift gradually reduces as the annealing temperature increases. At annealing temperatures > 900 °C, no further reduction in the flatband voltage shift is observed, and the δv_{fb} is ~ -0.1 V. This shows that the annealing temperature has reached a saturation point and no further reduction in the flatband voltage shift can be obtained. For the case of annealing temperature fixed at 1000 °C, an almost constant δv_{fb} ranging from -0.2 to -0.1 V is observed for annealing time longer than 20 min, as shown in Fig. 2. The dependence of the flatband voltage shift on both the annealing temperature and annealing time shown in Fig. 2 clearly indicates that an annealing at 900 °C for 20 min is good enough as a higher annealing temperature or a longer annealing time does not reduce the flatband voltage shift further. This has an important implication for memory device fabrication when excess thermal budget must be avoided.

From the flatband voltage shift, the number of trapped Si ions can be determined, as discussed in the following. The distribution of the charge density $\rho(x)$ due to the trapped Si ions in the SiO_2 thin film can be assumed to be proportional to the distribution of the implanted Si in the SiO_2 thin film, i.e., $\rho(x) = Af(x)$, where A is a coefficient depending on thermal annealing, and $f(x)$ is the distribution of the implanted Si. In this study, $f(x)$ is experimentally determined from SIMS measurement. It is observed that $f(x)$ is slightly different for different annealing. The number of trapped Si ions is found to be

$$N = \frac{(C_{\mathrm{ox}}\delta v_{\mathrm{fb}})}{1.6 \times 10^{-19}} \frac{T_{\mathrm{ox}} \int_0^{T_{\mathrm{ox}}} f(x)dx}{\int_0^{T_{\mathrm{ox}}} xf(x)dx} \quad \text{ions/cm}^2 \qquad (1)$$

where T_{ox} is the oxide thickness, and C_{ox} ($= \varepsilon_r \varepsilon_0 / T_{\mathrm{ox}}$, where ε_r is the dielectric constant of SiO_2, and ε_0 is the permittivity in vacuum) is the oxide capacitance per unit area. Therefore, from the flatband
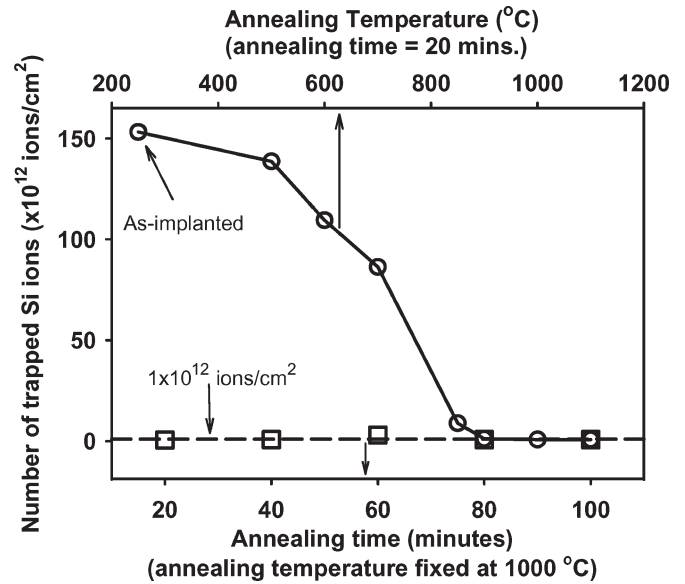
voltage shifts shown in Fig. 2, the number of trapped Si ions as a function of annealing temperature and annealing time can be calculated with (1), and the results are shown in Fig. 3. As can be seen in the figure, the as-implanted sample (note that, actually, the sample has been annealed at ~ 250 °C for ~ 20 min during the deposition of the electrodes) has $\sim 1.5 \times 10^{14}$ ions/cm^2 trapped in the SiO_2. This means that only $\sim 0.2\%$ of the implanted ions (note that the implant dose is 8×10^{16} ions/cm^2) remains in the SiO_2 thin film of the as-implanted sample. As the annealing temperature is increased, the number of the trapped ions decreases. For the annealing time of 20 min, the number of the trapped ions is reduced to $\sim 1 \times 10^{12}$ ions/cm^2 at the annealing temperature of 900 °C, and there is no further reduction in the number of the trapped ions at higher annealing temperatures. On the other hand, at the annealing temperature of 1000 °C, the number of trapped ions is also $\sim 1 \times 10^{12}$ ions/cm^2 for any annealing time longer than 20 min. It seems that $\sim 1 \times 10^{12}$ ions/cm^2 is the lowest limit corresponding to the smallest flatband voltage shift ($\delta v_{\mathrm{fb}} \sim -0.1$ V). This amount of ions can cause only a very small flatband voltage shift ($\delta v_{\mathrm{fb}} \sim -0.1$ V) because they are located far away ($> \sim 20$ nm) from the SiO_2/Si interface. In contrast, they can cause a flatband voltage shift of as much as ~ -1 V if they are located close to the SiO_2/Si interface. However, it should be pointed out that the lowest amount ($\sim 1 \times 10^{12}$ ions/cm^2) of ions is obtained under the assumption that the smallest flatband voltage shift ($\delta v_{\mathrm{fb}} \sim -0.1$ V) is caused by the trapped Si ions. If the smallest flatband voltage shift is due to other factors, such as nanocrystal-induced work function change, the above discussion on the lowest amount of ions is invalid.

On the other hand, the flatband voltage shift can be reduced by electron injection from the gate under a negative gate voltage, indicating that the trapped Si ions can be neutralized by the injected electrons. Fig. 4 shows the flatband voltage shift as a function of the electron injection time at the gate voltage of -5 V for the samples annealed at different temperatures or for different annealing time. For the as-implanted sample, the electron injection of the first 60 s causes a dramatic reduction from -37.8 to -4.8 V in the flatband voltage shift; however, further electron injection does not change the flatband voltage shift, showing that some trapped ions ($\sim 1.9 \times 10^{13}$ ions/cm^2) cannot be neutralized by the injected electrons. For the sample
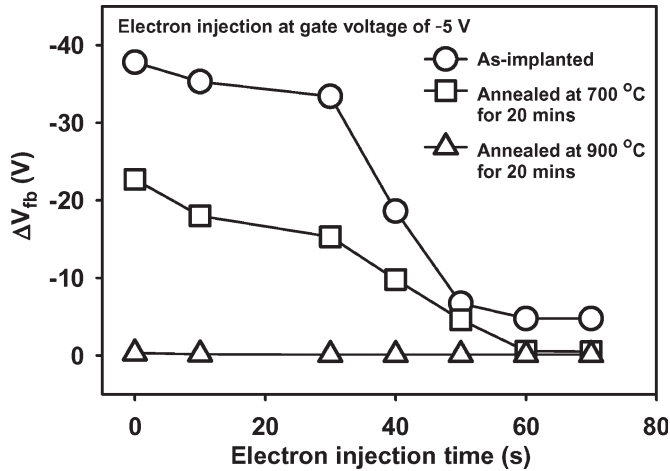
Fig. 4.   Reduction of flatband voltage shift by electron injection from the gate.

annealed at 700 °C for 20 min, there are also a small amount of trapped ions of 2×10^{12} ions/cm^2 that cannot be neutralized by the electron injection. For the sample annealed at 900 °C for 20 min, as discussed earlier, the thermal annealing has reduced the number of the trapped ions to the lowest limit (i.e., 1×10^{12} ions/cm^2) and, therefore, the electron injection does not lead to a significant change in the flatband voltage shift.

IV. CONCLUSION

The effect of Si ions trapped in the gate oxide on the $C-V$ characteristics and the flatband voltage has been examined through the thermal-annealing experiments. The flatband voltage shift due to the trapped Si ions can be reduced drastically by thermal annealing. For the sample annealed at 250 °C for $\sim$ 20 min, although only $\sim$ 0.2% of the implanted Si ions is remaining, it can cause a flatband voltage shift of as much as ~ -38 V. However, annealing at 900 °C for 20 min has reduced the number of the trapped ions to the lowest limit ($\sim 1 \times 10^{12}$ ions/cm^2), which corresponds to a flatband voltage shift of ~ -0.1 V. Higher annealing temperature or a longer annealing time does not show any obvious improvement. On the other hand, the flatband voltage shift is reduced by electron injection from the gate, indicating that the trapped ions can be neutralized by the electron injection.

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Effect of Source Extension Junction Depth and Substrate Doping Concentration on I-MOS Device Characteristics

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Abstract—Some device design issues of the impact-ionization MOS (I-MOS) device are discussed in terms of the junction depth of the source extension region and the substrate doping concentration. It is found that the source extension region is needed to be as shallow as possible in order to minimize the avalanche breakdown voltage. Furthermore, it is observed that the dependence of the threshold voltage of the I-MOS device on the substrate doping concentration is contrary to that of the MOSFET, which is an interesting phenomenon. It is related to the junction abruptness between the channel and the i-region, which is explained by using the concept of maximum lateral electric field.

Index Terms—Avalanche breakdown voltage, design, impact-ionization MOS (I-MOS) device, junction depth, maximum lateral electric field, substrate doping concentration.

I. INTRODUCTION

Recently, aggressive scaling down of the MOSFET has aggravated some important problems [1], [2]. The impact-ionization MOS (I-MOS) device was proposed in order to overcome one of them,

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