



Effects of NO Annealing and GaO_xN_y Interlayer on GaN Metal-Insulator-Semiconductor Capacitor with SiO₂ Gate Dielectric

L. M. Lin and P. T. Lai[†]

Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong

SiO₂ was deposited on GaN by radio-frequency sputtering to fabricate metal-insulator-semiconductor (MIS) capacitors. Before the deposition, an ultrathin GaO_xN_y interlayer was thermally grown on the GaN wafer to improve the quality of the insulator/GaN interface. The interface-trap density at 0.4 eV below the conduction bandedge was reduced by one order compared with that of a sample without the GaO_xN_y interlayer. Annealing in NO gas at 800°C was conducted on both samples, and turned out to greatly suppress their oxide charges. The NO-annealed sample with the GaO_xN_y interlayer achieved the lowest oxide-charge density of $1.7 \times 10^{11} \text{ cm}^{-2}$, as compared to $9.5 \times 10^{11} \text{ cm}^{-2}$ for its counterpart without the GaO_xN_y interlayer and about $8.0 \times 10^{12} \text{ cm}^{-2}$ for the two nonannealed samples. Moreover, the NO annealing was found to effectively reduce border traps. Secondary-ion mass spectrometry analysis was performed to explain how the GaO_xN_y interlayer and NO annealing affect the performance of the GaN MIS capacitors.

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As wide-bandgap III-V material, GaN has brought great interest to optical applications: high-efficiency light-emitting diodes, ultraviolet photodetectors, and laser diodes.¹ Based on the advantages of high critical electric field (up to 3 MV/cm) and low thermal generation rate, GaN is also suitable for fabricating high-power and high-temperature devices, such as metal-semiconductor field-effect transistor,² metal-insulator-semiconductor field-effect transistor (MISFET),³ and high-electron-mobility transistor.^{4,5} Although AlGaIn/GaN heterostructure field-effect transistor has advantages over MISFET such as high two-dimensional electron-gas density and high carrier mobility, it suffers from large gate leakage and current collapse. As a result, GaN MISFET also received much attention due to its normally off nature and relatively lower gate-leakage current,⁶ and many dielectric films such as Ga₂O₃,⁷ Ga₂O₃(Gd₂O₃),⁸ Sc₂O₃,⁹ SiO₂,¹⁰ Si₃N₄,¹⁰ and MgO¹¹ have been applied as its gate dielectric. However, leakage current through the gate dielectric, interface quality, and charges in the dielectric are major obstacles. Native Ga₂O₃ achieved low interface-state density D_{it} , but its leakage current was high.² In order to improve the interface quality and breakdown field, SiO₂ stacked with thermally grown Ga₂O₃ was prepared by growing 15 nm Ga₂O₃ and 35 nm Ga oxynitride, and then sputtering 100 nm SiO₂.¹² In this paper, we show that a much thinner (~4 nm) thermally grown GaO_xN_y can effectively reduce interface traps, and the negative effects of GaO_xN_y on breakdown field and gate leakage current can be minimized by increasing the thickness ratio of SiO₂ to GaO_xN_y. Low-pressure chemical-vapor deposited SiO₂ annealed in NO or NH₃ at 1100°C for 5 min was found to increase the leakage current and degrade the performance of GaN capacitor.¹³ In this work, both stacked (SiO₂/GaO_xN_y/GaN) and nonstacked (SiO₂/GaN) structures were annealed in NO at a lower temperature of 800°C for 1 h, and as a result, showed less oxide charges and border traps. In addition, the effects of the NO annealing on interface states and breakdown field are discussed. Last, a microscopic analysis was done by secondary-ion mass spectrometry (SIMS) to explain how the GaO_xN_y interlayer can improve the interface quality, and how the NO annealing can reduce the oxide charges.

Fabrication of devices.—GaN wafers used in this study were prepared by metallorganic chemical-vapor deposition on c-plane sapphire. A 25 nm undoped GaN buffer layer was grown at 550°C and then 1 μm epitaxial n-type GaN was grown at 1170°C. The epitaxial GaN layer was intentionally doped with Si to $5 \times 10^{17} \text{ cm}^{-3}$. Four wafers were cleaned by the standard RCA

method and then dipped into 1:1 HF solution to remove the native oxide and contaminants.¹⁴ Two wafers were loaded into a furnace at 300°C, and the temperature was raised to 800°C in nitrogen ambient. Then, an oxidation was performed at 800°C in diluted oxygen (O₂:N₂ = 1:4) for 15 min. Because 200 nm GaO_xN_y could be formed in pure oxygen for 12 h at 800°C in our system, the GaO_xN_y interlayer was estimated to be less than 4 nm. Then, a layer of SiO₂ was deposited on all the samples, producing two with SiO₂/GaO_xN_y stacked gate dielectric. The thickness of SiO₂ was measured to be 40 nm with an error of 0.5 to 3% by a variable-angle spectroscopic ellipsometer from J. A. Wollam Co., Inc. After that, one stacked sample was annealed at 800°C in nitrogen, denoted as S-N₂; another was annealed in NO, denoted as S-NO. The two nonstacked samples without the GaO_xN_y interlayer were annealed also at 800°C in N₂ and NO, and denoted as NS-N₂ and NS-NO, respectively. Finally, Al was thermally evaporated as electrodes for all the samples and then annealed in argon at 410°C for 30 min for good ohmic contacts. The area of the resulting capacitors was $7.85 \times 10^3 \text{ cm}^2$. High-frequency (1 MHz) capacitance-voltage characteristics were measured by using an HP4284A LCR meter with a bias sweep rate of 0.1 V/s. The current-voltage (*I*-*V*) characteristics were measured by an HP4156B semiconductor parameter analyzer. All measurements were conducted in a dark ambient at room temperature.

Results and Discussion

SIMS.—The SIMS results of the four samples are shown in Fig. 1a-d. The top 5 nm signals are omitted due to the instability of SIMS signals at the sample surface. The curves have been adjusted along the *x*-axis due to the difference in dielectric thickness, thus providing clearer comparison. There are similar peak intensities of SiO₂, SiN, GaN, and GaO for the NS-N₂, S-N₂, and S-NO samples in the transition region, while the intensity variations vs depth for the NS-NO sample are gradual with no elements piling up at the interface. It has been reported that the diffusivity (*D*) of Ga in SiO₂ is about 2 to 6 orders of magnitude higher than those of B, P, Al, Sb in SiO₂.¹⁵ This high diffusivity makes it possible to implant Ga through a 5000 Å SiO₂ layer into the underlying Si, and then a 30 min annealing at 800°C in N₂ resulted in significant diffusion of the implanted Ga ($D = 2.9 \times 10^{-15} \text{ cm}^2/\text{s}$).¹⁶ At 800°C, Si can diffuse into GaN to a distance of about 30 Å ($D = 1.9 \times 10^{-17} \text{ cm}^2/\text{s}$, calculated based on the values in Ref. 17).¹⁷ In brief, Ga can diffuse in SiO₂ about 100 times faster than Si in GaN. Therefore, we can conclude that Ga out-diffusion into SiO₂ is the main reason for the formation of SiGaON glass at the interface or in the dielectric layer. The NS-NO sample has characteristics quite different from the

[†] E-mail: laip@eee.hku.hk

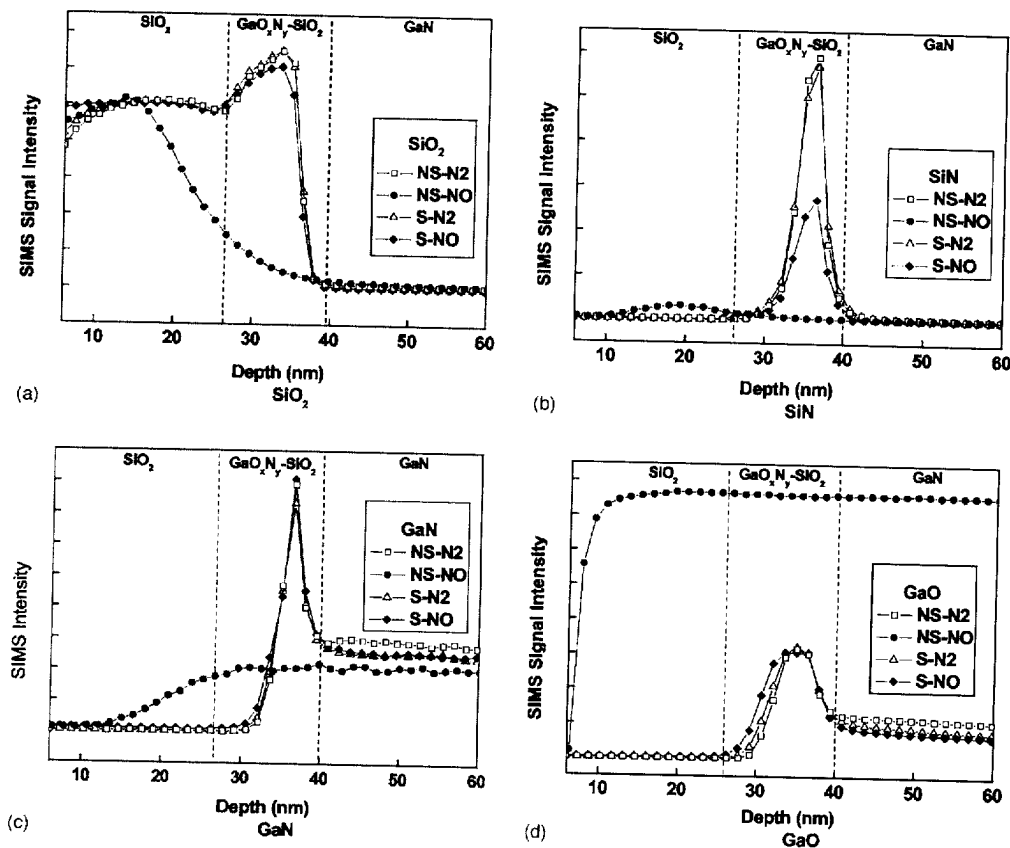


Figure 1. SIMS profiles of the GaN MIS capacitors. (a) SiO₂, (b) SiN, (c) GaN, (d) GaO.

other three: (i) the intensities of SiO₂ and SiN gradually decrease from the surface of the dielectric to the interface, (ii) the intensity of GaN gradually increases from the surface to the interface, (iii) the GaO intensity remains high from the surface to the GaN substrate. The above three characteristics clearly demonstrate that a large amount of Ga has outdiffused into the SiO₂ dielectric. The reason why the NS-NO sample has much more Ga diffusing into SiO₂ compared with the same structure annealed in N₂ (NS-N2) should be because the N and O decomposed from NO can have chemical reaction with Ga ions, and thus Ga ions have higher chance to diffuse into the dielectric under the oxidizing ambient. The diffused Ga could damage the lattice structure of SiO₂ and produce defects, which trigger large leakage current. However, according to the S-NO sample, many fewer Ga ions diffuse into the SiO₂ dielectric. This should be associated with the presence of the GaO_xN_y interlayer because Ga-O and O-N bonds are much more stable than Ga-N bonds under the oxidizing ambient. Moreover, the peak intensity of SiN in the transition layer is even lower than those of the two samples annealed in nitrogen. This is probably related to the fact that the N released from NO can react with the Si near the SiO₂/GaN interface to form Si oxynitride, which can block the nitrogen out-diffusion from the GaN substrate more effectively than SiO₂.

Positive oxide charges.—Although the SIMS profiles of the NS-NO and S-NO samples are quite different, a common feature is a significant reduction of positive oxide charges induced by the NO annealing. Figure 2a and b shows the high-frequency capacitance-

voltage (HF *C-V*) characteristics of the four samples, and Table I presents the device parameters extracted from the HF *C-V* curves (average values from six sample points).

The oxide thickness is calculated from the oxide capacitance C_{ox} , which is approximated by the maximum value in the accumulation region. After annealing, the films become denser and their thicknesses calculated from C_{ox} are a little bit smaller than the original 40 nm. For the samples NS-N2, S-N2, and NS-NO, the interdiffusion mainly happens near the interface (Fig. 1), and thus would not have significant effect on their dielectric constants. As for the sample S-NO, although there is more interdiffusion (Fig. 1), its dielectric constant hardly changes due to little changes in its oxide thickness and C_{ox} . The chemical compositions of the four oxide films have little changes after annealing, and therefore, the dielectric constant used for calculation is taken to be that of SiO₂ (3.9).

The capacitance at the flatband voltage is as follows

$$C_{fb} = \frac{C_s C_{ox}}{C_s + C_{ox}} \quad [1]$$

where

$$C_s = \epsilon_{GaN} \epsilon_0 / L_D \quad [2]$$

$$L_D = (kT \epsilon_{GaN} \epsilon_0 / q^2 N_d)^{1/2} \quad [3]$$

ϵ_{GaN} is the dielectric constant of GaN; ϵ_0 is the permittivity of free space; L_D is the Debye length; N_d is the actual carrier concentration ($1.1 \times 10^{17} \text{ cm}^{-3}$) calculated from the measured capacitance; k is the Boltzmann's constant, and T is the measurement temperature

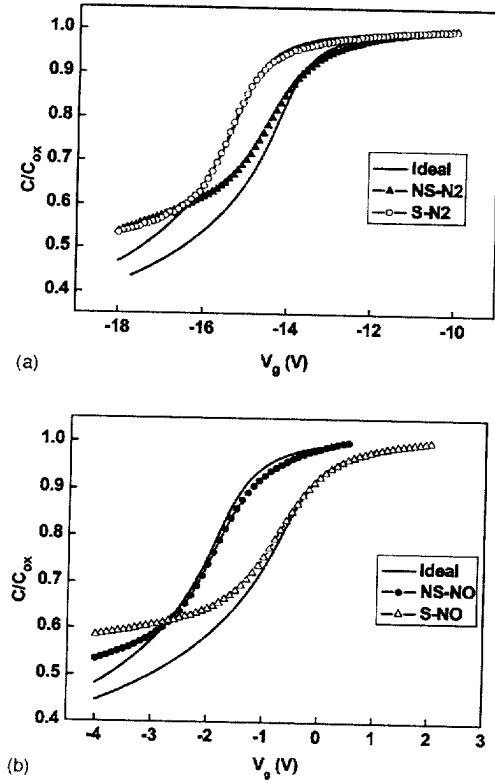


Figure 2. Measured and ideal C - V curves of the GaN MIS capacitors with SiO_2 or stacked dielectric. (a) Annealed in N_2 , (b) annealed in NO .

(298 K). Oxide-charge density Q_{ox} is determined from the shift of flatband voltage

$$V_{\text{fb}} = \phi_{\text{Al,GaN}} - \frac{Q_{\text{ox}}}{C_{\text{ox}}} \quad [4]$$

$$\phi_{\text{Al,GaN}} = \chi + E_g/2 - (kT/q) \ln(N_d/n_i) \quad [5]$$

where $\phi_{\text{Al,GaN}}$ is the work-function difference between Al and GaN; χ is the electron affinity of GaN (4.07 eV); n_i is the intrinsic carrier concentration of GaN at room temperature ($2.0 \times 10^{-10} \text{ cm}^{-3}$);¹⁸ E_g is the forbidden bandgap of GaN (3.4 eV). After the NO annealing, the HF C - V curve shifts right, resulting in the lowest oxide-charge density of $1.8 \times 10^{11} \text{ cm}^{-2}$ for the S-NO sample, followed by the NS-NO sample at $9.5 \times 10^{11} \text{ cm}^{-2}$, with Q_{ox} of the former more than one order lower than those of the two N_2 -annealed samples.

During the SiO_2 sputtering process, high-energy Ar^+ ions bombard the SiO_2 target and knock off its molecules. First, the SiO_2 molecules have many dangling bonds. Second, these high-energy molecules to be deposited on the GaN wafer can break the GaN bonds, thus creating more dangling bonds. These dangling bonds of the Si or Ga ions should be the reason for the large Q_{ox} of the two N_2 -annealed samples (NS-N2 and S-N2). However, through the NO annealing for the NS-NO and S-NO samples, sputtered SiO_2 can also achieve low oxide-charge density, which should be due to the N and O decomposed from NO forming bonds with the Si or Ga ions.

Border traps.—Oxide traps close to the interface which can communicate with the semiconductor are called border traps,¹⁹ whose density (Q_{bt}) can be calculated by the following formula

$$Q_{\text{bt}} = C_{\text{ox}} \Delta V_{\text{FB}} / (q \times d) \quad [6]$$

ΔV_{FB} is the hysteresis at flatband between opposite sweeping directions of gate voltage; d is the distance in the oxide above the GaN surface ($\sim 30 \text{ \AA}$).¹⁹ The hysteresis is due to the difference in gate biases at which electrons fill the traps and escape from the traps, or the difference between the capture and emission times of the border traps. In Table I, it can be seen that after the NO annealing, the border traps are reduced for both the NS-NO and S-NO samples. The NS-NO sample achieved the lowest border-trap density of $1.2 \times 10^{17} \text{ cm}^{-3}$, which should be related to the decrease of oxide charges after the NO annealing, as mentioned in the previous section.

Interface traps.—Interface-trap density is calculated based on the HF C - V curve by using the Terman method.²⁰ The interface traps follow the change in gate bias and cause a stretch-out of the HF C - V curve. The ideal capacitance is calculated by the following equation²¹

$$C_{\text{ideal}} = \frac{C_s C_{\text{ox}}}{C_s + C_{\text{ox}}} \quad [7]$$

where surface capacitance C_s is

$$C_s = \frac{C_{\text{FBS}}}{\sqrt{2}} \frac{\exp(v_s) - (n_i/N_d)^2 \exp(-v_s) - 1}{[-(v_s + 1) + \exp(v_s) + (n_i/N_d)^2 \exp(-v_s)]^{1/2}} \quad [8]$$

with carrier concentration N_d given by

$$N_d = \frac{2}{q \epsilon_{\text{GaN}} \epsilon_0 A^2 d (1/C^2) / dV} \quad [9]$$

As Fig. 3 shows, N_d is fitted for the gate voltage ranging from -15.2 to -16.3 V based on the measured HF C - V curve of the S-N2 sample. Any fitting error is probably due to the nonuniformity of doping concentration or the interface traps. In order to compare the interface quality of different samples, the same N_d ($1.1 \times 10^{17} \text{ cm}^{-3}$) is used in all calculations. Figure 2a and b shows the difference between the ideal and measured C - V curves. The ideal curves are shifted along the x -axis because the interface-state density is not related to the shift of flatband voltage but only the shape

Table I. Electrical and physical parameters of the GaN MIS capacitors extracted from the high-frequency C - V curves.

Sample	NS-N2	NS-NO	S-N2	S-NO
T_{ox} (\AA)	379	381	380	390
V_{FB} (V)	-13.4	-1.6	-14.4	-0.21
Q_{ox} ($\times 10^{11} \text{ cm}^{-2}$)	77.2	9.5	85.0	1.8
D_{it} @ $E_c - E_v = 0.4 \text{ eV}$ ($\times 10^{16} \text{ cm}^{-2} \text{ eV}^{-1}$)	120	63	5.9	160
$Q_{\text{bt}} \times 10^{17} (\text{cm}^{-3})$	2.6	1.2	2.7	2.0
J_{leakage} @ E_{BD}	65 mA/cm^2 @ 4.9 MV/cm	1.2 mA/cm^2 @ 0.23 MV/cm	1.2 mA/cm^2 @ 0.93 MV/cm	1 mA/cm^2 @ 1.79 MV/cm

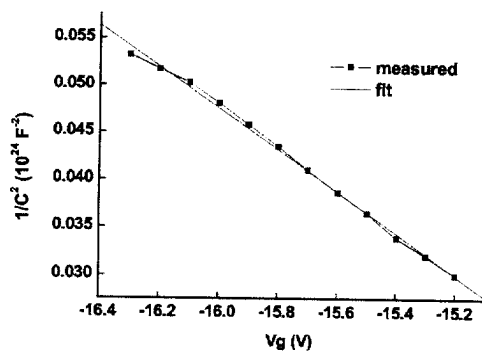


Figure 3. Typical capacitance characteristic of the GaN MIS capacitors vs gate voltage. Carrier concentration obtained by the fitting is $1.1 \times 10^{17} \text{ cm}^{-3}$.

of the curve. The S-N2 sample has the smallest stretch-out from the ideal curve, indicating least interface traps among all the samples. The interface-trap distribution from 0.1 to 0.8 eV below the conduction band is shown in Fig. 4. Obviously, although the deep-level traps close to the midgap are hardly affected by thermally growing a Ga oxynitride interlayer or annealing in NO, the shallow traps close to the conduction band can be greatly suppressed. However, for the stacked sample annealed in NO, the shallow traps increase, probably due to excessive accumulation of nitrogen at the interface. Specifically, Table I shows that at 0.4 eV below the conduction bandedge, the S-N2 sample achieves a low interface-trap density of $5.9 \times 10^{10} \text{ cm}^{-2}$, followed by the NS-NO sample with $6.3 \times 10^{11} \text{ cm}^{-2}$, $1.2 \times 10^{12} \text{ cm}^{-2}$ for the NS-N2 sample, and $1.6 \times 10^{12} \text{ cm}^{-2}$ for the S-NO sample. The relatively high interface-trap density of the NS-N2 sample should be related to sputtering-induced damage of crystalline structure and large amount of dangling bonds formed at the interface. The S-N2 sample has fewer interface traps, possibly due to the formation of a GaO_xN_y interlayer through oxidation before the sputtering deposition. This interlayer can work as a buffer layer to reduce the damage of the GaN surface caused by the ensuing sputtering. Moreover, because GaO has higher binding energy than GaN,²² the GaO_xN_y interlayer is more resistant to high-energy bombardment, thus forming a more passivated interface. The NO annealing has different effects on the stacked and nonstacked samples. For the nonstacked sample (NS-NO), it presents improved interface quality, which should be due to the N or O decomposed

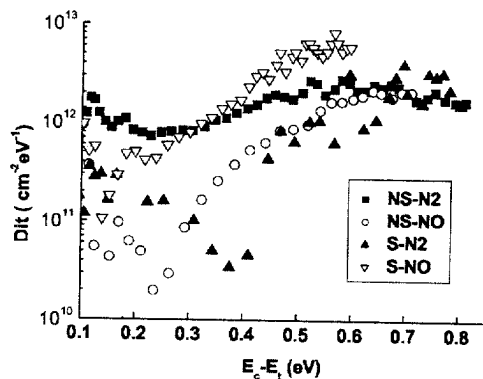


Figure 4. Interface-trap density of the GaN MIS capacitors vs energy (from 0.1 to 0.8 eV below the conduction band) extracted from the high-frequency C-V curves.

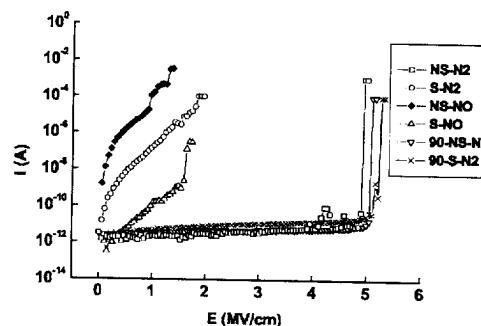


Figure 5. Typical leakage current of the GaN MIS capacitors vs electric field E . (Samples 90-SiN2 and 90-GaN2 have a thicker SiO_2 of 90 nm.)

from NO forming bonds with the dangling bonds of the Ga or Si ions at the interface, and thus results in a much smoother interface. However, after the stacked sample is annealed in NO (S-NO), the interface traps increase significantly, implying that too many nitrogen and oxygen atoms (decomposed from NO) piling up at the interface could also introduce traps and deteriorate the performance of devices. It is believed that by reducing the NO concentration in annealing, shortening annealing time, or lowering annealing temperature, the $\text{SiO}_2/\text{Ga}_2\text{O}_3/\text{GaN}$ system annealed in NO could achieve fewer oxide charges as well as fewer interface traps.

Breakdown field (E_{BD}) and leakage current.—Figure 5 shows the current vs electric-field (I - E) characteristic. The electric field is estimated by using the total equivalent thickness calculated from C_{ox} , with an error of about 5% due to the interlayer in the samples. The NS-N2 sample has the best I - E characteristic and lowest leakage current through the gate dielectric. The E_{BD} of the NS-N2 sample is as high as 4.9 MV/cm ($J_{leakage} = 65 \mu\text{A}/\text{cm}^2$), followed by 1.79 MV/cm ($J_{leakage} = 1 \text{ mA}/\text{cm}^2$) for the S-NO sample, 0.93 MV/cm ($J_{leakage} = 1.2 \text{ mA}/\text{cm}^2$) for the S-N2 sample, and 0.23 MV/cm ($J_{leakage} = 1.2 \text{ mA}/\text{cm}^2$) for the NS-NO sample. After annealing in NO, the leakage current of the NS-NO sample increased significantly due to a large amount of Ga outdiffused into the dielectric. However, for the sample with GaO_xN_y interlayer, improved I - E characteristic was achieved by annealing in NO (the S-NO sample vs the S-N2 sample), which should be related to reduced oxide charges and defects in the dielectric. Compared with the nonstacked sample NS-N2, the stacked sample S-N2 presents degraded I - E characteristic, which should be due to the negative effects of the thermally grown GaO_xN_y interlayer. Stacked and nonstacked samples with thicker SiO_2 were also fabricated by sputtering. In Fig. 4, the 90-NS-N2 sample means 90 nm SiO_2 was deposited on GaN, while the 90-S-N2 sample had 90 nm SiO_2 deposited on the same $\text{GaO}_x\text{N}_y/\text{GaN}$ structure used earlier. Both samples were annealed in nitrogen at 800°C for 1 h after the SiO_2 deposition. When the thickness of the SiO_2 dielectric was increased to 90 nm, the negative effects brought by the GaO_xN_y interlayer could be suppressed, resulting in little difference in the breakdown and leakage characteristics between the samples with or without the interlayer.

Figure 6 depicts the energy-band diagram for a GaN MIS capacitor with a positive gate bias, and the interlayer is simplified as Ga_2O_3 with a smaller conduction-band offset ($\Delta E_c = 0.9 \text{ eV}$) than SiO_2 ($\Delta E_c = 2.3 \text{ eV}$).⁶ For very thin interlayer, electrons can directly tunnel through it to the $\text{Ga}_2\text{O}_3/\text{SiO}_2$ interface. For thicker interlayer, the Fowler-Nordheim (FN) tunneling and thermionic emission dominate, and make the electrons jump to the conduction band of the Ga_2O_3 interlayer. Under the same electric field in the SiO_2 layer, the electrons at the GaN/ SiO_2 interface have the highest barrier of 2.3 eV to overcome (Fig. 6a): the electrons after direct

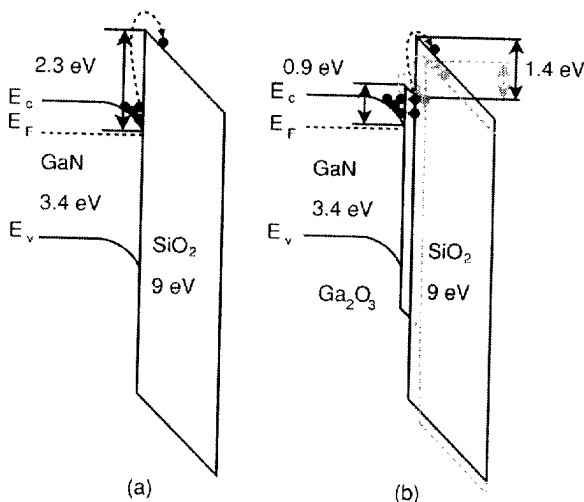


Figure 6. (Color online) Energy-band diagram of gate dielectric on GaN. (a) SiO_2/GaN . (b) $\text{SiO}_2/\text{Ga}_2\text{O}_3/\text{GaN}$. Black balls represent the electrons when Ga_2O_3 is thin to have direct tunneling dominant; gray balls represent the electrons when Ga_2O_3 is thicker to have FN tunneling and thermionic emission dominant.

tunneling through the Ga_2O_3 interlayer see a lower barrier of 1.4 eV (solid arrow in Fig. 6b); and the electrons after FN tunneling through the Ga_2O_3 interlayer face the lowest barrier of less than 1.4 eV (dotted arrow in Fig. 6b). Thus, we can deduce that the thinner the interlayer, the lower the leakage current because the existence of the interlayer lowers the barrier. For the NS-N2 sample, it should have the thinnest interlayer, which makes the dielectric conduction mechanism mainly decided by the SiO_2 layer. The NS-NO sample has Ga ions outdiffused into the SiO_2 layer to produce a thicker interlayer (see Fig. 1), and the resulting lower barrier leads to an increase of leakage current. If the SiO_2 thickness increases, the SiO_2 layer dominates the conduction mechanism, and thus the electrons will find it harder to go through the SiO_2 layer by the thermionic emission or FN tunneling. Therefore, we can conclude that by decreasing the interlayer thickness or increasing the SiO_2 thickness, the leakage current can be effectively reduced, which can be well supported by our experimental results.

Therefore, it is expected that through optimizing the thicknesses of SiO_2 and GaO_xN_y , low oxide-charge density, good interface quality, and high breakdown field could be simultaneously achieved.

Conclusions

NO annealing was applied on both SiO_2/GaN and $\text{SiO}_2/\text{GaO}_x\text{N}_y/\text{GaN}$ MIS structures and turned out to effectively reduce fixed oxide charges by about one order. Nitrogen and oxygen atoms (decomposed from NO) forming bonds with the dangling Si or Ga in the gate dielectric was the main reason for the reduction of positive oxide charges. The NO annealing was also shown to suppress the border traps for the same reason. A very thin GaO_xN_y interlayer formed by thermal oxidation can improve the interface quality and achieve a low interface-trap density D_{it} of 5.9

$\times 10^{10} \text{ cm}^{-2}$. After the NO annealing, D_{it} of the SiO_2/GaN capacitor was reduced by about half due to the formation of a GaO_xN_y interlayer by the chemical reaction between GaN and NO. The D_{it} of the $\text{SiO}_2/\text{GaO}_x\text{N}_y/\text{GaN}$ structure increased after the NO annealing, implying that too many nitrogen and oxygen atoms (decomposed from NO) piling up at the interface could also have deteriorated the interface quality. According to the breakdown field E_{BD} and leakage current characteristics, SiO_2/GaN capacitor annealed in nitrogen achieved the highest E_{BD} and lowest leakage current. After the NO annealing, E_{BD} was degraded for the sample without the GaO_xN_y interlayer, but improved for the sample with the interlayer. SIMS results reveal that the opposite phenomenon should be due to the formation of SiGaON glass throughout the SiO_2 dielectric in the former, and the blocking of Ga out-diffusion by the interlayer in the latter. After increasing the SiO_2 thickness to 90 nm, the differences in E_{BD} and leakage characteristics between the stacked and non-stacked samples were negligible. Therefore, it should be possible that interface quality, oxide charges, and E_{BD} could be all improved through optimizing the SiO_2 thickness and NO-annealing conditions.

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