

## Interfacial Microstructures in Ramp Type Multilayer Josephson Junctions Studied by TEM

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**Abstract**—The microstructures of high  $T_c$  ramp type Josephson junctions were studied by using transmission electron microscopy. The work was emphasized at the interfacial defects and the influence of the ramp slope. The results show that for the ramp slope angles of  $15^\circ\sim 40^\circ$ , the epitaxy was still remained through all layers at the ramp region without the formation of big grain boundaries. No amorphous layers and secondary phases were observed at the barrier interfaces. For a gentle ramp junction, small misoriented grains appeared in some portions of the barrier. The substrate ramp formed during the ion etching process had little influence on the growth of the upper layers. In junctions with a steep ramp, defects increased near the interface, although the epitaxy of the barrier was of good quality. The results demonstrate that the slope angle of the junction ramp is an important factor that influences the performance of the Josephson junctions.

### I. INTRODUCTION

Ramp type Josephson junctions are formed on the ramp surface of epitaxial multilayer and allow the Josephson coupling taking place along the  $a,b$ -plane [1]–[5]. In comparison with other kinds of HTS Josephson junctions, ramp type multilayer junctions allow for the adjustment of junction performance by changing the barrier thickness or the barrier material [6], [7]. Since they can be fabricated at desired locations and the device parameters can be varied according to the application requirements they have attracted lots of research interests in the past several years.

A major problem associated with ramp junctions is that their reproducibility is relatively poor. It is mainly influenced by the defects formed near the interfaces. Investigation using transmission electron microscopy (TEM) is useful to identify the nature and formation of the interfacial defects. The TEM studies in ramp junctions were reported by several groups [8], [9]. However, all the results were obtained on samples with a small ramp slope. Little attention has been given to the influence of the ramp slope on the formation of interfacial defects although Jia *et al* reported the such study on step-edge junctions [10]. For ramp type multilayer junction, the situation is somewhat different from that in step-edge junctions. The ramp surface is created on multilayer structure whereas the step-edge is formed on single crystal substrate. The quality of the multilayer would affect the ramp surface

and the growth of the barrier. Thus the ramp slope of the junction turns out to be important for the occurrence of the defects in the junction region.

In this paper, microstructures in ramp types Josephson junctions with a  $\text{PrBa}_2\text{Cu}_3\text{O}_y$  (PBCO) barrier were investigated by means of TEM. The goal of our study is to reveal the possible origins which cause the difficulty in reproducing the ramp type Josephson junctions. In particular, the influences of the ramp slope angles on the microstructure of the junctions are discussed.

### II. EXPERIMENT

The details about preparation of our junctions and TEM samples were described in our early publications [7], [11]. In brief, the samples were made by using off-axis sputtering. A mixture of Ar and  $\text{O}_2$  with a ratio of  $\text{Ar}/\text{O}_2\sim 3/1$  was used as sputter gas. The total sputter pressure was 0.1-0.2 mbar and the rf-power was  $\sim 80$  W. The substrate temperature was kept in the range of  $720\text{--}750^\circ\text{C}$ . The junction ramp was created by lithography and ion beam etching. The beam voltage and current were typically 500 V and 10 mA, respectively. To create ramp with various slopes the incident angle of the Ar-ion beam was controlled between  $40^\circ$  to  $65^\circ$ , resulting in ramp angles of  $10^\circ\text{--}40^\circ$ .

The challenge for preparing XTEM sample of junctions lies in that the thin area should be located exactly at the junction region, which is about a few microns, and the thin area should be large enough, which enables us to investigate the whole range of the junction. We have made lots of efforts to achieve useful and good cross sectional TEM samples. The specimens were cut into slices with the cutting direction perpendicular to the junction 'trips'. Two of the slices were glued together face to face. After mechanical grinding and polishing, the samples were thinned by ion milling process. When a very tiny hole appeared near the center of the sample, an ion-polishing procedure was applied to finally thin the sample to electron transparency. To obtain a reliable and systematical results, in this work junctions with six different ramp slopes were fabricated and more than twenty TEM samples were prepared, among which some were fail. The TEM study was carried out on a JEOL 2000FX and a JEOL 2010 electron microscope operating at 200 kV.

### III. RESULT AND DISCUSSION

In this research our efforts have been emphasized at the interfacial microstructural characteristics and the influence of the ramp slope on the formation of interfacial defects. Fig. 1 presents the low magnification bright field XTEM views of

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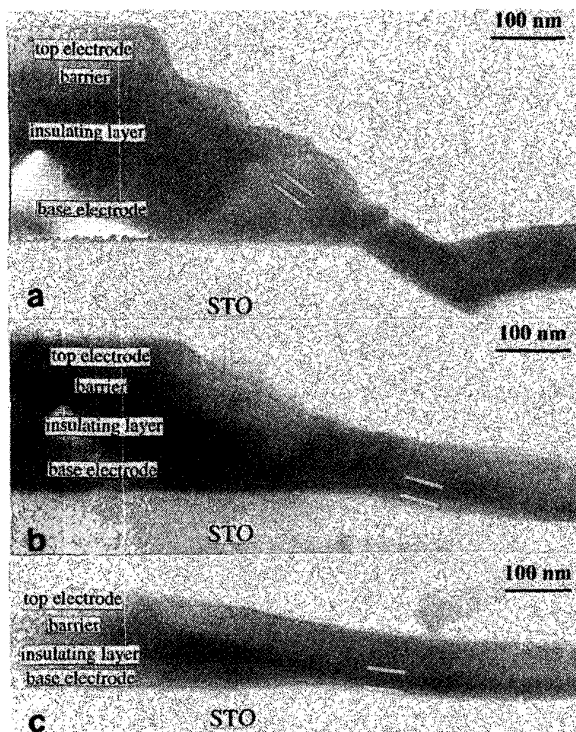


Fig. 1 Low magnification cross sectional views of the junctions with different ramp slopes. The ramp angles are  $40^\circ$ ,  $27^\circ$ , and  $15^\circ$ , respectively. For all samples, the thickness of barrier is about 20 nm.

the junctions with ramp slopes of  $40^\circ$ ,  $27^\circ$ , and  $15^\circ$ , respectively. The contrast change indicates the locations of  $\text{YBa}_2\text{Cu}_3\text{O}_y$  (YBCO) layers and PBCO barrier. The thickness of PBCO barrier is about 20 nm and quite homogeneous for all samples used in this study. As shown in Fig. 1a, the thickness of the removed substrate is about 80 nm. A dimple was formed in the substrate near the junction region. Actually such a dimple is typical for the junctions made with a steep

ramp. In contrast, we did not observe similar dimple in the junctions with a gentle ramp. Cautions should be exercised with such a dimple because it often leads to the formation of grain boundaries or big dislocations. Such defects were found at the dimple location even perovskite substrates were used. It differs from that reported by Wen *et al*, they mentioned that the discontinuity of epitaxy occurred only on non-perovskite the base, insulating, and top-layer, respectively [9]. With a small slope (as shown in Fig. 1c) the thickness of all layers in the junction region is quite uniform, being about 50 nm, 120 nm, and 100 nm for grain boundary. In contrast, the YBCO top-layers for the junction with a steep slope is somewhat non-uniform. It is unclear whether such inhomogeneity was caused by the film growth on a steep ramp or by the high angle ion milling.

Fig. 2 shows a typical TEM image of our ramp junction fabricated on (100)  $\text{SrTiO}_3$  (STO) substrate. The contrast difference between YBCO and PBCO is not obvious due to their similar structures. In order to enhance the contrast it is necessary to take the image in a direction that is not parallel to a low index zone. Thus the *ab*-plane of the film is not parallel to the electron beam. By tilting the *ab*-plane of the film about  $5^\circ$  away from the electron beam, the barrier can be distinguished from the adjacent YBCO layers. According to the deposition time and TEM observation, the thickness of the base, insulating, barrier and top layer are about 65 nm, 70 nm, 30 nm, and 60 nm, respectively. As can be seen in Fig. 2, the ramp with a gentle slope is formed with all layers grown epitaxially to each other. These layers are oriented with their *c*-axes parallel to the [001] direction of the substrate. The interfaces between the PBCO barrier and the YBCO layers are visible, as indicated by the black broken lines. The slope angle of this junction ramp is about  $15^\circ$ . Actually, the slope angle strongly depends on the etching process, such as the incident angle of ion beam, the thickness of photoresist, the energy of Ar ions, and so on. In this TEM study, the slope angle of our junctions are varied in the range from  $10^\circ$  to  $40^\circ$ . Usually we make the etching time a little bit

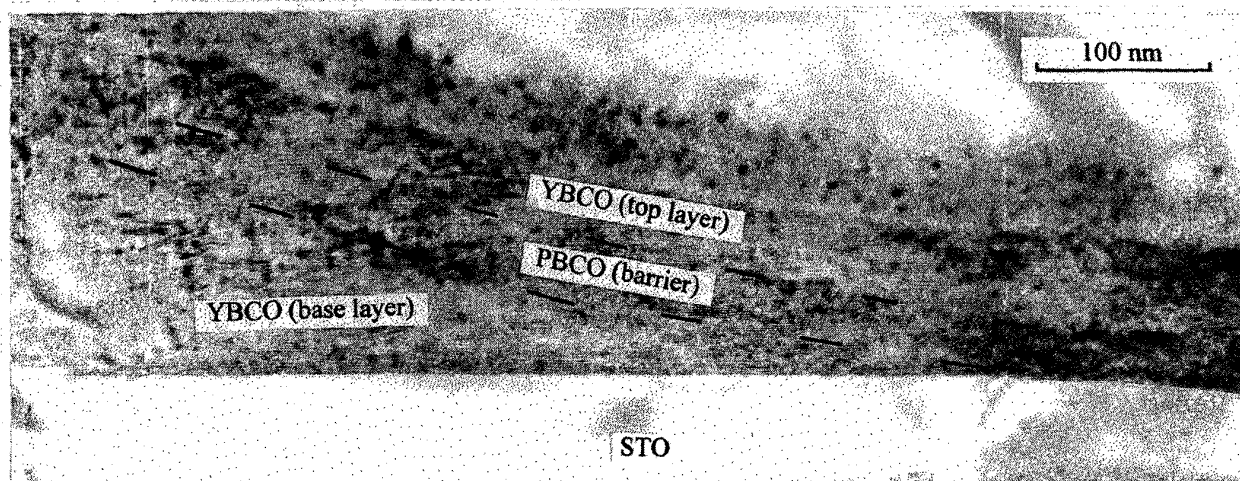


Fig. 2. A low magnification TEM review of a YBCO/PBCO/YBCO ramp junction, taken by tilting  $5^\circ$  away from the [100] axis. The slope angle of this junction is about  $15^\circ$ .

longer to ensure that the base electrode is completely removed, thus some of the substrate material is removed also. This results in an extension of the ramp into the substrate, as can be seen at the right bottom side of Fig. 2.

The interface microstructure plays an important role in determination of the junction properties. Fig 3 is a micrograph of the interface region taken along the *ab*-plane of the film. The major defects in the ramp region are stacking faults and antiphase boundaries (APBs). Small *a*-axis grains with sizes of about 10 nm are present in a local area along the barrier interface, as marked rectangle A in Fig. 3. Their images are overlapped with the image of the *c*-axis film, so that some moiré type fringes can be observed. The origination of these *a*-axis grains is most likely on the etched ramp surface of the insulating layer. The further growth of such grains is effectively depressed by the growth of the *c*-axis film, so that they only appeared near the interface between the barrier and insulating layer. Compared with area A, the interface between the barrier and YBCO base electrode (marked as area B) is better defined without the presence of misoriented structures. The defects which appear near the barrier/base layer interface are mainly lattice shifts with *c*/3 unit between PBCO and YBCO, forming antiphase boundaries. They are probably caused by the ex-situ deposition process. Before the deposition of the barrier, Ar-ion beam etching and photolithography processes are performed in order to fabricate the junction ramp. The contact with atmosphere, photoresist, acetone *etc.* may all bring damages to the ramp surface, which result in defects on the barrier interface.

For relatively small ramp slopes, the substrate ramp created by the ion etching procedure is quite gentle and broad. A TEM image of the etched substrate part is presented in Fig. 4, the slope angle of the STO substrate ramp is  $\sim 6^\circ$ . It was found that the PBCO barrier was grown epitaxially on a gentle substrate ramp with its *c*-axis parallel to the [001] direction of STO. We did not observe any amorphous layer

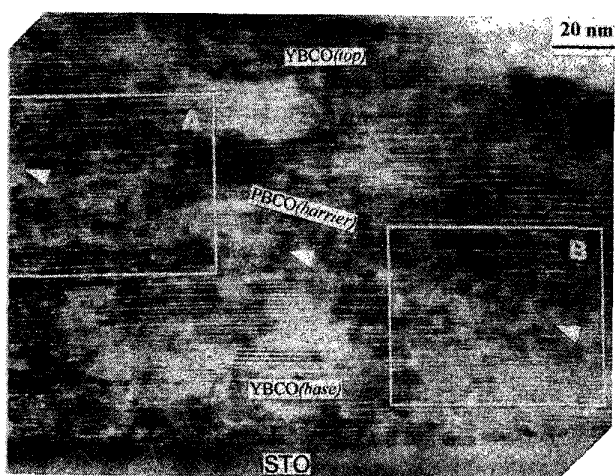


Fig. 3 High resolution TEM micrograph showing the multilayer structure at the junction ramp with a gentle slope.

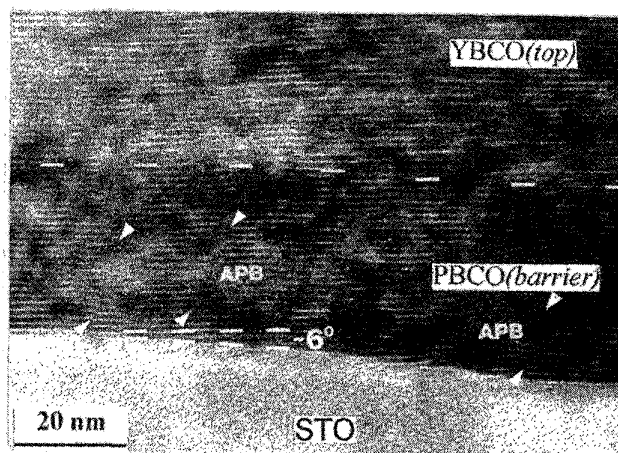


Fig. 4. A quite gentle ramp was formed in the substrate and the epitaxy of the grown layers has not been significantly influenced.

or intermediate layer. To accommodate the slope change of the substrate surface, antiphase boundaries were formed near the interface between the film and substrate. The concentration of APBs in such area is slightly higher than that in the upper layers. The formation of the interface between the PBCO barrier and YBCO top layer (marked by the broken line) was not influenced by the quite gentle slope angle.

The junction revealed in Fig. 5 was fabricated by using a high angle ion beam etching. Measured from the TEM picture, the slope angle of the junction is about  $40^\circ$ . As can be seen, some portions of the top YBCO layer have become amorphous, which seems due to the excess of ion milling adopted in the process of high resolution TEM specimen preparation. But the multilayer at the ramp area is still grown epitaxially with the same orientation. In this junction sample, the thickness of the removed substrate is about 60 nm except for the area close to the junction region where a deep dimple was formed in the substrate (as indicated by an arrow in Fig. 5). The slope angle of the substrate ramp (the white arrow) is

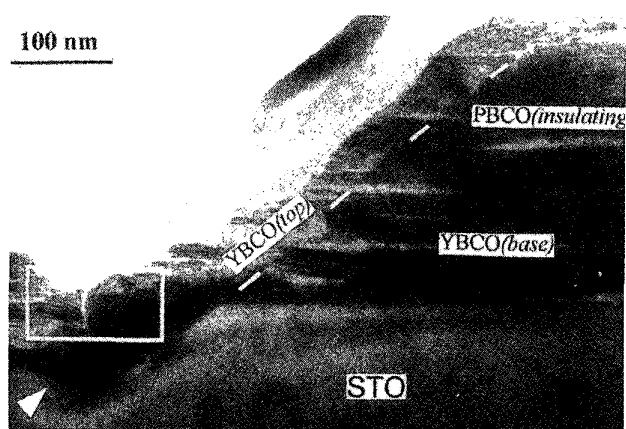


Fig. 5. A low magnification bright field view of a junction with a large ramp slope. The slope angle is about  $40^\circ$ . The white arrow indicates the small difference between the ramp slopes of layers and STO substrate.

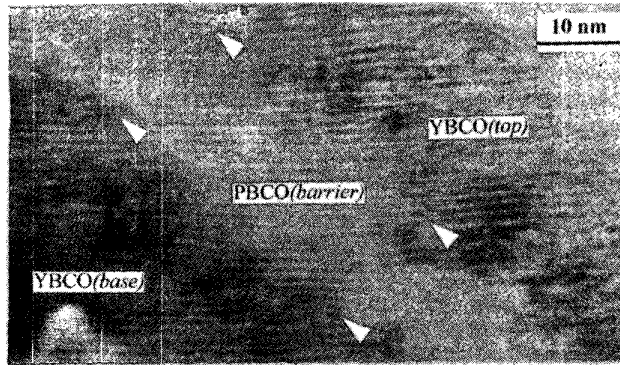


Fig. 6. Microstructure of the multilayer at the ramp region with a relatively steep slope. The white arrows indicate the barrier interfaces.

a little bit smaller than that of the film ramp. The epitaxial growth of the layers was ruptured at the dimple and a big misoriented grain was formed, as marked by the rectangle. The grown layers on such a dimple are usually distorted. Actually, the occurrence of the deep dimple is often accompanied with misoriented grains. From our experience, to prevent the formation of such defects the incident angle of the Ar-ion etching beam should not exceed  $40^\circ$ .

Fig. 6 is a high resolution TEM picture of the junction region with a steep ramp. The barrier layer may be identified by the contrast change in the image, or by the defect appearance near the interface between the barrier and base layer. Given by TEM image the thickness of PBCO barrier is about 15 nm, which is consistent with that estimated from the sputtering time. It can be seen that the three layers at the junction region are still grown epitaxially to each other. The barrier has a relatively homogenous contrast. Few defects like secondary phases, domains and grain boundaries can be observed within the barrier. Compared with the base layer, the top YBCO is much more defective. The (001) planes of some parts of the YBCO layer near the film surface are slightly inclined. The origin to cause such inclination is unclear. It seems caused by the TEM sample preparation process. As the top layer was in-situ deposited on the barrier, one might expect an interface with fewer defects between the barrier and the top layer. However, the defect concentration near the interface between the barrier and top layer does not change significantly.

#### IV. CONCLUSION

The microstructures of the ramp-type Josephson junctions have been investigated by using HRTEM. Our results show that disregarding the ramp slope angles up to  $40^\circ$ , all layers at the ramp regions are grown epitaxially with  $c$ -axis orientation. Amorphous layers and secondary phases are not observed at the barrier interfaces. In the junction with a small

slope angle, some  $a$ -axis grains with sizes of about 10 nm are present in local areas of the barrier. They are most likely nucleated on the etched surface of the insulating layer. The further growth of such grains is effectively depressed by the film growth along the  $c$ -axis. A gentle and broad ramp formed in substrate by the ion beam etching does not influence the orientation of the film grown on it. In contrast, a deep dimple created in substrate causes the bending in the film and the nucleation of misoriented grains. In the junction with a slope angle of about  $40^\circ$ , the PBCO barrier exhibits a homogenous contrast. The top YBCO is much more defective than the base YBCO layer. Our TEM investigation demonstrates that the slope angle and the surface morphology of the ramp should be controlled attentively, since they give rise to different microstructural features of the ramp junctions.

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