# Post-Stress Interface Trap Generation Induced by Oxide-Field Stress with FN Injection

T. P. Chen, Stella Li, S. Fung, C. D. Beling, and K. F. Lo

***Abstract*—Interface trap generation in nMOS transistors during both stressing and post-stress periods under the conditions of oxide field (dynamic and dc) stress with FN injection is investigated with charge pumping technique. In contrast to the post-stress interface trap generation induced by hot carrier stress which is a logarithmical function of post-stress time, the post-stress interface trap generation induced by oxide-field stress with FN injection first increases with post-stress time but then becomes saturated. The mechanisms for the interface trap generation in both stressing and post-stress periods are described.**

***Index Terms*— Integrated circuit reliability, MOS devices, MOSFET's, semiconductor device reliability, silicon materials/devices.**

## I. Introduction

IT IS well known that the injection of hot carriers (electrons and/or holes) from the drain of n-channel MOSFET's results in the generation of fast interface traps and in the trapping of charges in the gate oxide, and both effects can result in the degradation of device performance. Recently, a post-stress increase of the interface trap generation induced by hot-carrier stress was reported [1], [2], and the post-stress effect is attributed to the release of hydrogen by the thermal detrapping of the injected holes. On the other hand, high voltage stress of thin gate oxide will also lead to trap generation in the oxide and at the interfaces [3], causing reliability problems in devices. There have been many studies on oxide field stress (for example, [3]–[5]), but most of them were carried out under the conditions of dc voltage. There has been relatively little information concerning trap generation at the interface under dynamic oxide field stress. Interface trap generation under dynamic stress conditions has been investigated in previous studies [6]–[9], but some controversies still exist. As the oxide field stress with FN injection may lead to the trapping of holes in the oxide, it is interesting to ask whether there is a post-stress interface trap generation induced by the oxide field stress, similarly to the situation of hot-carrier stress. In this work, we will show that dynamic (bipolar, and positive and negative unipolar) and dc (positive and negative) oxide field stresses with FN injection also lead to post-stress interface trap generation. In contrast to the post-stress interface trap generation induced by hot-carrier stress which proceeds logarithmically with post-stress time [1], the post-stress interface trap generation induced by oxide field stress with FN injection first increases with post-stress time but then becomes saturated. A model based on the release of hydrogen by detrapping of the trapped holes in the oxide is used to explain the post-stress interface trap generation.

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## II. Experiments

The devices used in this study are packaged n-channel MOSFET's with a gate length of 0.5 $\mu$m, a gate width of 50 $\mu$m, an oxide thickness of 110 Å, and a source/drain junction depth of 0.2 $\mu$m. The devices are of polysilicon gate fabricated on $p$-substrate with a 0.5 $\mu$m process.

Dynamic voltage or dc voltage is applied to the gate electrode to stress the devices at room temperature. During the stressing process, the source, drain, and substrate are grounded. For dynamic stress, bipolar and unipolar square waveforms are used. A symmetric bipolar pulse train with equal pulse width is used in bipolar stress. The unipolar stress consists of two types, i.e., the positive unipolar stress and the negative unipolar stress. For dc stress, both positive and negative voltage are used. In all the stress experiments, the magnitude of stress voltage is set to be 10 V.

Interface trap density $N_{it}$ is determined by charge pumping technique. Charge pumping measurement is carried out with a HP 4155A semiconductor parameter analyzer and a Toellner 7704 function generator at room temperature. The device under test (DUT) is mounted in a HP 16442A test fixture. For the charge pumping measurement, the frequency and amplitude of the voltage pulse applied to the gate electrode is 300 kHz and 4 V, respectively, and the source and drain are grounded. The interface trap density is monitored before and immediately after stress, and after a certain post-stress time. Note that during the post-stress period (the period after the termination of stress), the gate, source, drain, and substrate are all grounded. The interface trap density for fresh devices, i.e., the prestress interface trap density is in the order of $10^{10}$ cm$^{-2}$.

## III. Results and Discussions

For the same magnitude of applied voltage, the electric field strength in the oxide film is different for positive and negative voltages. The electric field in the oxide film $E_{\text{ox}}$ is evaluated as follows. For inversion, $E_{\text{ox}}$ is obtained by taking into account the flat-band voltage $V_{FB}$ and the substrate potential $2\phi_F$ ($q\phi_F$ is the energy difference between the midgap

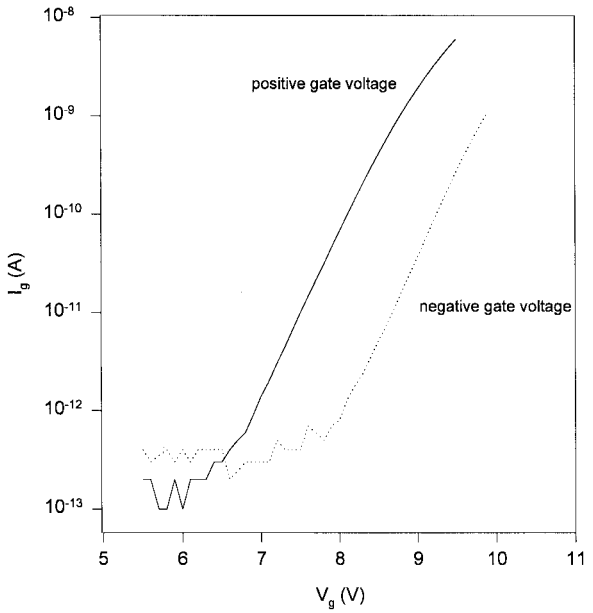


Fig. 1. Gate current $I_g$ as a function of gate voltage $V_g$. The measurement is carried out on fresh devices. Gate current is measured when the gate voltage is swept from 0 V to positive or negative voltage at a low sweep rate.

position and the Fermi level in the bulk of the substrate) as [4]

$$E_{\rm ox} = (V_g - V_{FB} - 2\phi_F)/t_{\rm ox} \tag{1}$$

where $V_g$ is the voltage applied to the gate and $t_{\rm ox}$ is the thickness of the oxide film. For accumulation, $E_{\rm ox}$ is defined as [4]

$$E_{\rm ox} = (V_g - V_{FB} - 0.55 + \phi_F)/t_{\rm ox}. \tag{2}$$

As the substrate is p-type, positive voltage corresponds to the inversion while the negative voltage corresponds to the accumulation. The values of $V_{FB}$ and $\phi_F$ are $-1.36$ V and 0.48 V, respectively, for the 110-Å oxide film grown on the $p$-type substrate. If we take the electric field of 6 MV/cm across the oxide film as the criterion of the start of the FN tunneling [4], it is estimated from (1) and (2) that the FN tunneling current starts to build up at around 6 V for positive voltage and at around $-8$ V for negative voltage for the devices used in this study. This has been confirmed by Fig. 1. As mentioned above, the amplitude of stress voltage used in this study is 10 V. Based on (1) and (2), this gives an oxide field of 9.45 and 7.92 MV/cm for positive voltage and negative voltage, respectively. Obviously, the amplitude of stress voltage leads to FN tunneling across the gate oxide.

As shown in Fig. 2(a) for negative voltage, electrons are injected from the gate to the oxide conduction band by FN tunneling and are accelerated toward the substrate. Some of the electrons reach the $SiO_2$/substrate interface and lose their energy as they drop to the conduction band of the silicon. Part of the energy is converted to interface trap generation as the chemical bonds at the interface are broken by the energetic electrons. In addition, electron-hole pairs in the substrate are also generated by the energetic electrons, and the generated

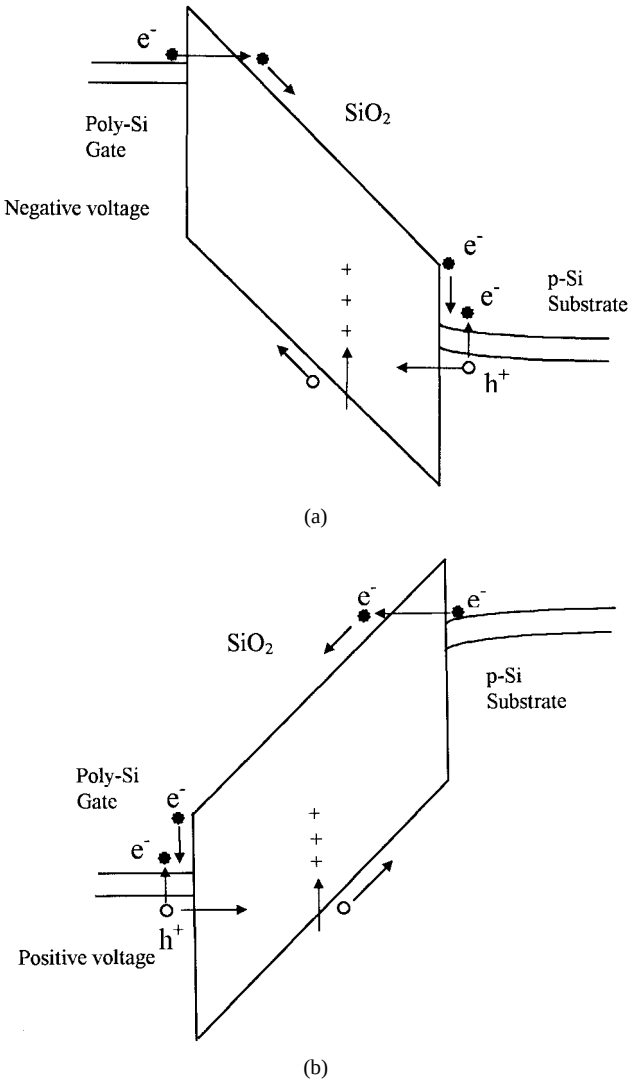


Fig. 2. Schematic energy band diagram for FN injection under (a) negative voltage and (b) positive voltage.

holes are injected into the oxide. Then, some of the trapped holes may recombine with electrons, leading to interface trap generation [6]. The release of hydrogen due to the reaction of the holes with the Si-H bonds in the oxide may create interface traps also (see discussions below). On the other hand, as shown in Fig. 2(b) for positive voltage, electrons are injected from the substrate toward the gate by FN tunneling, and some of the electrons release their energy at the poly-Si/$SiO_2$ interface, generating electron-hole pairs in the poly-Si. The generated holes will then be injected into the oxide. Holes may also be generated inside the oxide via impact ionization [6]. Some of the holes drift to the $SiO_2$/substrate interface (the cathode) under the influence of the applied electric field, and the recombination of the holes with electrons leads to trap generation at the interface. For both negative and positive voltage stresses, holes are generated and injected into the oxide. The holes may react with the Si-H bonds in the $SiO_2$ layer, leading to the release of hydrogen (H or $H^+$). The released hydrogen may also create some interface traps. This mechanism may play a role during both the stressing and

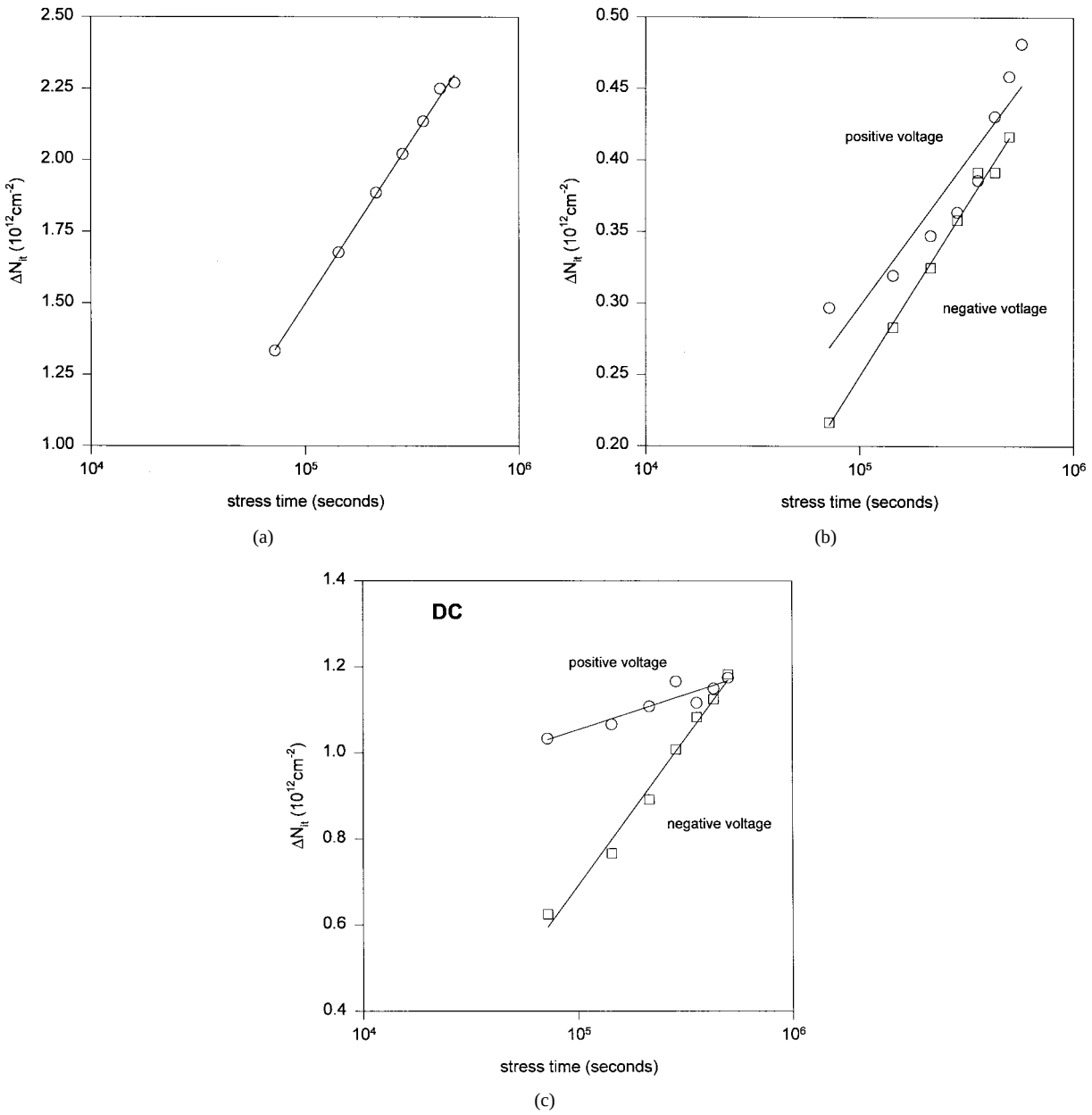


Fig. 3. Interface trap generation by oxide field stress (the amplitude of stress voltage is 10 V) as a function of stress time. (a) Bipolar voltage with a frequency of 3 MHz, (b) unipolar (positive and negative) voltage with a frequency of 3 MHz, and (c) dc (positive and negative) voltage. $\Delta N_{it} = N_{it}$ (at the time immediately after stress)—$N_{it}$ (before stress).

post-stress periods. The details for this mechanism will be described below. In summary, for positive voltage, the two mechanisms including the recombination of trapped holes with electrons and the release of hydrogen may be involved in the interface trap generation. For negative voltage, in addition to the two mechanisms, the mechanism of bond breaking at the interface by the energetic electrons may also be responsible for the interface trap generation. It should be pointed out that the two mechanisms for positive voltage described above are somewhat similar to those proposed by DiMaria *et al.* [15]–[17]. According to their model [15]–[17], the interface trap generation for positive voltage are caused by the following two mechanisms: a) trap creation near the cathode (i.e., the substrate) caused by mobile hydrogen release from near the anode (i.e., the gate)/oxide interface by hot electrons and b) trap generation near the cathode caused by electron/trapped-hole recombination where holes are generated in the oxide bulk by impact ionization.

The interface trap generation under the stresses of bipolar, unipolar (positive and negative) and dc (positive and negative) voltage as a function of stress time is shown in Fig. 3. It is evident from Fig. 3 that, for all the stress experiments, interface trap generation is a logarithmical function of stress time, in the form of $\Delta N_{it} = A\log(t)+B$, where $t$ is the stress time, and $A$ and $B$ are two constants which are different for different stress conditions. This is different from the stress-time dependence of hot-carrier stress which can be described by a power law [10]–[12]. As can be seen in Fig. 3, for both unipolar and dc stresses, the positive voltage generates more interface traps than the negative voltage. The reason for this

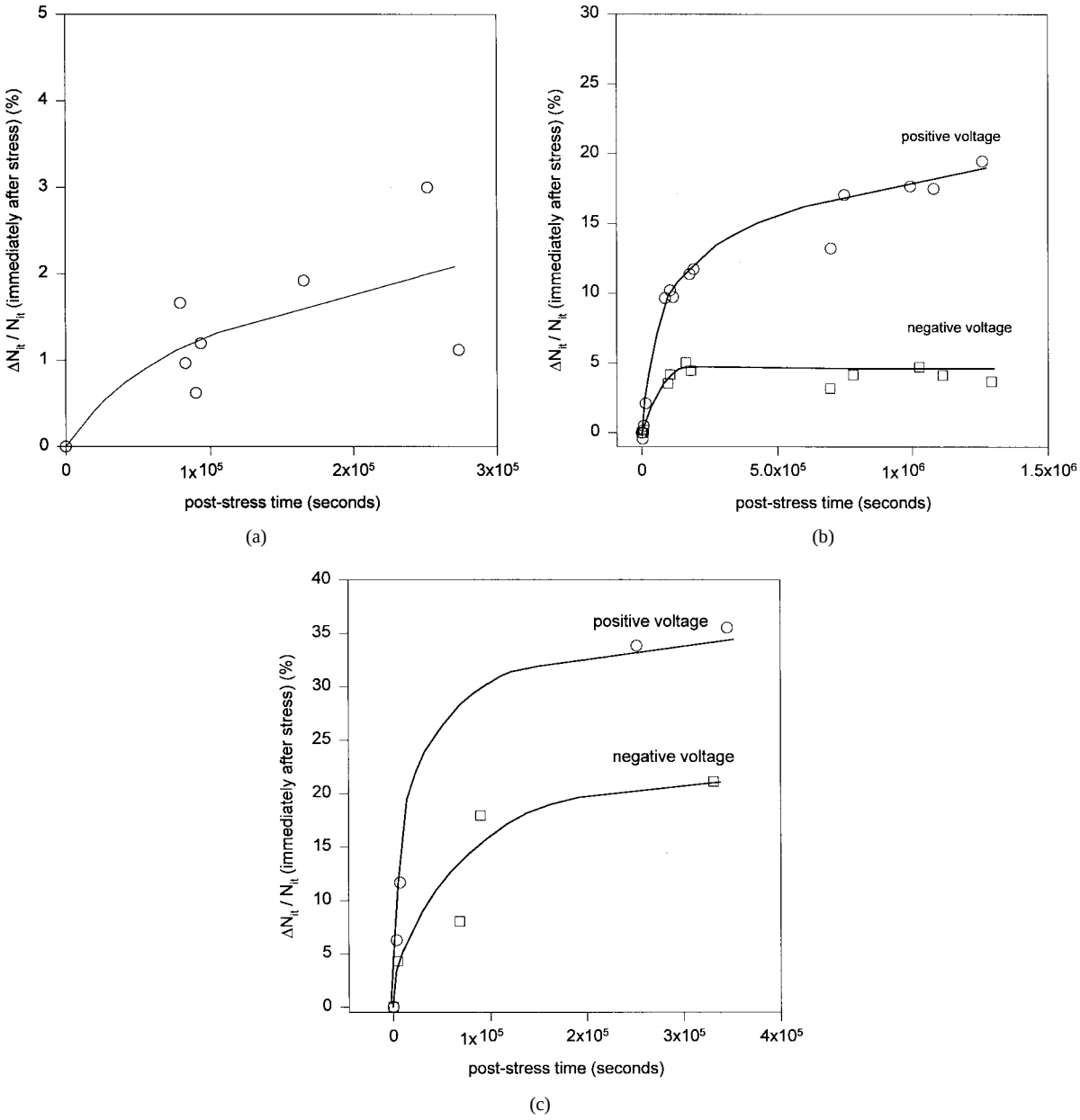


Fig. 4. Post-stress interface trap generation as a function of post-stress time. The devices are subjected to the following stresses (the amplitude of stress voltage is 10 V) for 20 min. (a) Bipolar (300 kHz) voltage, (b) unipolar (positive and negative, 300 kHz) voltage, and (c) dc (positive and negative) voltage. $\Delta N_{it} = N_{it}$ (post-stress time)—$N_{it}$ (at the time immediately after stress).

situation is that in the present study, the oxide field for the positive voltage (9.45 MV/cm) is significantly higher than that for the negative voltage (7.92 MV/cm), and thus the positive voltage leads to much more charges passing through and injected into the oxide. However, the negative voltage has a higher rate of interface trap generation, as shown in Fig. 3(c). The mechanism of the bond breaking at the interface by energetic electrons under negative voltage stress is possibly responsible for this phenomenon (see the above discussions on the mechanisms for interface trap generation). Comparing Fig. 3(b) with Fig. 3(c), one can also find that the positive unipolar stress has about the same interface trap generation rate as the positive dc stress. On the other hand, Fig. 3 shows that bipolar stress gives the highest level of interface trap generation. This is consistent with the observation of Rosenbaum *et al.* [6], [7]. They reported that interface trap generation is enhanced under bipolar stress conditions. They pointed out that this is not surprising in light of the evidence which interface traps can be generated by the recombination of trapped holes with electrons, and the scenario of hole generation and detrapping when the field reverses can explain large interface trap generation under bipolar stress [6], [7].

For hot-carrier stress, a post-stress increase of the interface trap generation was reported [1]. Similarly, for both dynamic and dc oxide field stresses with FN injection, a post-stress interface trap generation is also observed in this study. In the following post-stress experiments, the DUT's are first stressed by bipolar, unipolar (positive and negative), or dc (positive and negative) voltage with the amplitude of 10 V for 20 min, and then, the interface trap density is monitored as a function of

post-stress time. The results are shown in Fig. 4. In contrast to the stress time dependence of interface trap generation shown in Fig. 3, the post-stress interface trap generation first increases with post-stress time but then becomes saturated. Note that for different stress conditions including bipolar, unipolar (positive and negative), and dc (positive and negative) voltage, the post-stress time dependence of interface trap generation is similar. This post-stress time dependence is different from that of the hot-carrier-induced post-stress interface trap generation. For hot-carrier stress, the post-stress interface trap generation proceeds logarithmically with time [1]. However, the present post-stress time dependence is similar to that of interface trap generation induced by pulsed ionizing radiation [13]. In [13], the post-stress time dependence of interface trap generation induced by radiation was explained successfully by a two-stage model. In the first stage, radiation creates holes in the oxide which react in the oxide bulk to produce positively charged ions, probably $H^+$. In the second stage, the $H^+$ ions move by dispersive transport to the $Si/SiO_2$ interface, where they can break a Si-H bond and create an interface trap.

In the following discussions, we will explain the post-stress interface trap generation induced by oxide-field stress with FN injection using a model similar to the two-stage model mentioned above. As discussed above, for both positive and negative voltage stresses, holes are generated and are injected into the oxide, and some of them are trapped in the oxide. The trapped holes may be detrapped thermally or under the influence of applied electric field. Thermal detrapping can take place during both the stressing and post-stress periods. After detrapping, the holes may react with the Si-H bonds in the $SiO_2$ layer and the reaction may occur according to one of the following processes [14]:

$$\text{Si-H} + h^+ \rightarrow \text{Si} + \text{H}^+ \tag{3}$$

or

$$\text{Si-H} + h^+ \rightarrow \text{Si}^+ + \text{H}. \tag{4}$$

The first process will lead to the release of positive hydrogen ions while the second one will lead to the release of neutral hydrogen atoms. During the post-stress period, the released hydrogen atoms may move by dispersive transport to the $SiO_2$/substrate interface where they can break a Si-H bond and create an interface trap Si• according to one of the following processes [1]:

$$\text{Si-H} + \text{H}^+ + \text{e}^- \rightarrow \text{Si} \bullet + \text{H}_2 \tag{5}$$

or

$$\text{Si-H} + \text{H} \rightarrow \text{Si} \bullet + \text{H}_2. \tag{6}$$

This model shows that the trapped holes play a key role in the post-stress interface trap generation. Obviously, the post-stress interface trap generation will be limited by the amount of the trapped holes which are available in the post-stress period. This has been confirmed by experiment. As shown in Fig. 4, different stress conditions lead to different values of the saturated post-stress interface trap density. As described above, the bipolar stress creates the largest number of interface traps during the stressing period (see Fig. 3). However, the bipolar stress gives the smallest percentage of post-stress interface trap generation (see Fig. 4). Under bipolar-stress conditions, the reversal of electric field will enhance the detrapping of the trapped holes during stressing, giving rise to a large interface trap generation in terms of the recombination of the holes with the injected electrons. On the other hand, the enhancement of detrapping leads to less trapped holes available in the post-stress period. This explains why the bipolar stress gives the smallest percentage of post-stress interface trap generation. Comparing Fig. 3 with Fig. 4, one can also find that, for both dc and unipolar stresses, the positive voltage leads to larger interface trap generation during both the stressing and post-stress periods compared to the negative voltage. We have already pointed out above that the positive voltage leads to much more charges passing through and injected into the oxide as its oxide field is significantly higher. In other words, there are more holes trapped in the oxide under the positive voltage conditions. This will lead to a larger post-stress interface trap generation, based on the above model of the release of hydrogen.

## IV. Conclusions

The post-stress interface trap generation induced by dynamic (bipolar and unipolar) and dc oxide field stresses with FN injection is observed in this work. In contrast to the post-stress interface trap generation induced by hot-carrier stress which is a logarithmical function of post-stress time, the post-stress interface trap generation induced by oxide-field stress with FN injection first increases with post-stress time but then becomes saturated. A model based on the release of hydrogen by detrapping of the trapped holes in the oxide is used to explain the post-stress interface trap generation. The hydrogen atoms are released by the reaction of the trapped holes with the Si-H bonds in the oxide and they move by dispersive transport to the interface where they break a Si-H bond and create an interface trap.

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**T. P. Chen**, for a photograph and biography, see this issue, p. 1926.

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**K. F. Lo**, for a photograph and biography, see this issue, p. 1926.