

Letters to the Editor

Reduction of Crosstalk on Printed Circuit Board Using Genetic Algorithm in Switching Power Supply

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Abstract—Crosstalk between printed circuit board (PCB) traces in switching power supplies may cause high electromagnetic interference emission. PCB layout plays an important part and a genetic algorithm (GA) is used to produce a layout with reduced crosstalk. A coupling index and a new way of representing a trace for the GA process is presented.

Index Terms—Crosstalk, electromagnetic interference, genetic algorithm, near field, switching power converter.

I. INTRODUCTION

Electromagnetic interference (EMI) is a major concern of a switching power supply engineer. The subject is not as well understood as other aspects of switching power supply. Reduction of EMI often takes up a good portion of the design time.

Many researchers have been attempting to tackle EMI issues but only a limited number focus on those concerning switching power supply. Of those interested in switching power supply EMI issues, some attempt to shape the switching waveform. Some use snubber circuits to reduce dv/dt and di/dt , some use resonant circuits with a quasi-sinusoidal waveform instead of a rectangular waveform. Some use random pulsewidth modulation (PWM) to average out the EMI spectrum so produced. Others use filters to filter out noise. Design guidelines are produced which advise minimization of switching loops. Despite these and many other attempts to reduce EMI, the issue remains largely unclear and more items will be added to the list.

In this letter, electric field coupling or crosstalk between printed circuit board (PCB) traces is raised as an important source of EMI in switching power supply. This is often overlooked because the noise is coupled through invisible coupling paths. PCB layout plays an important part in the process. In order to enable optimization of PCB trace placement, a trace is split into a number of turning points and a genetic algorithm (GA) is used to optimize the trace placement. This method allows maneuver of a trace in a two-dimensional PCB with respect to an electric field map produced by a noisy trace. An example illustrates the application of such method.

II. ELECTRIC FIELD COUPLING IN TERMS OF A COUPLING INDEX

Switching power supply has distinct EMI characteristics when compared with other noise-generating circuits, such as a digital circuit. Switching power supply has a few noise-generating nodes with high dv/dt , whereas a digital circuit may have many switching nodes spread all over the circuit. Very often, it is easy to identify such noisy nodes in a switch power supply. These nodes are often a terminal of a switching device. On the other hand, it is also easy to identify victims. They are

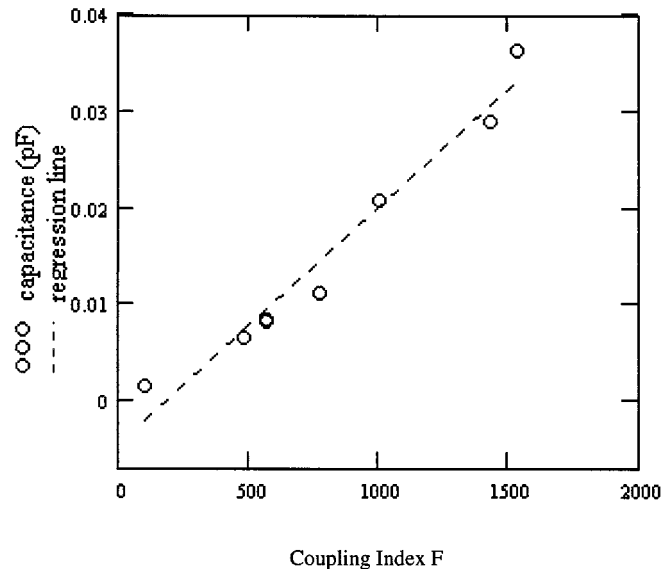


Fig. 1. Comparison of coupling index and capacitance.

those traces that can have adverse effects when they pick up noise emission from the noisy traces. A typical example of a victim trace is the connection to an input cable which is directly connected to the outside world. The placement of noisy traces and victim traces is very important in EMI reduction.

Capacitance between traces is often used to calculate crosstalk, but such method is not convenient despite its accuracy. Very often, finite-element analysis (FEA) [13] is used to calculate parasitic capacitance between traces but the process is computation intensive and it is not easy to produce a real-time response to enable layout adjustment. On the other hand, this often involves a stand-alone software package which cannot incorporate a GA for optimization in the later process.

Here, in the present work, a coupling index F is proposed which provides a reasonable but quick estimate of capacitance. This coupling index is represented by

$$F = \sum_{n=1}^N |\zeta(n)| \cdot \Delta A(n). \quad (1)$$

Here, a victim trace is placed in an electric field produced by a noisy trace. This victim trace is divided into N meshes and $|\zeta(n)|$ is the magnitude of displacement current density at the center of the n th mesh, and $\Delta A(n)$ is the area of the n th mesh. The coupling index F sums up all displacement current over the victim trace.

There is a conceptual difference between capacitance and the coupling index. Calculation of the coupling index assumes a fixed field which is not affected by the position of the victim trace, whereas capacitance calculation by finite-element method takes into account the effect of the victim trace on the field at the expense of computation complexity. This is an assumption. In order to verify that the simpler coupling index has sufficient correlation to capacitance, a comparison of results obtained by FEA capacitance calculation and the corresponding coupling indexes is carried out. Nine pairs of victim and noisy traces are generated at random which are compatible with a realistic power supply trace layout. Fig. 1 shows the correlation between the coupling

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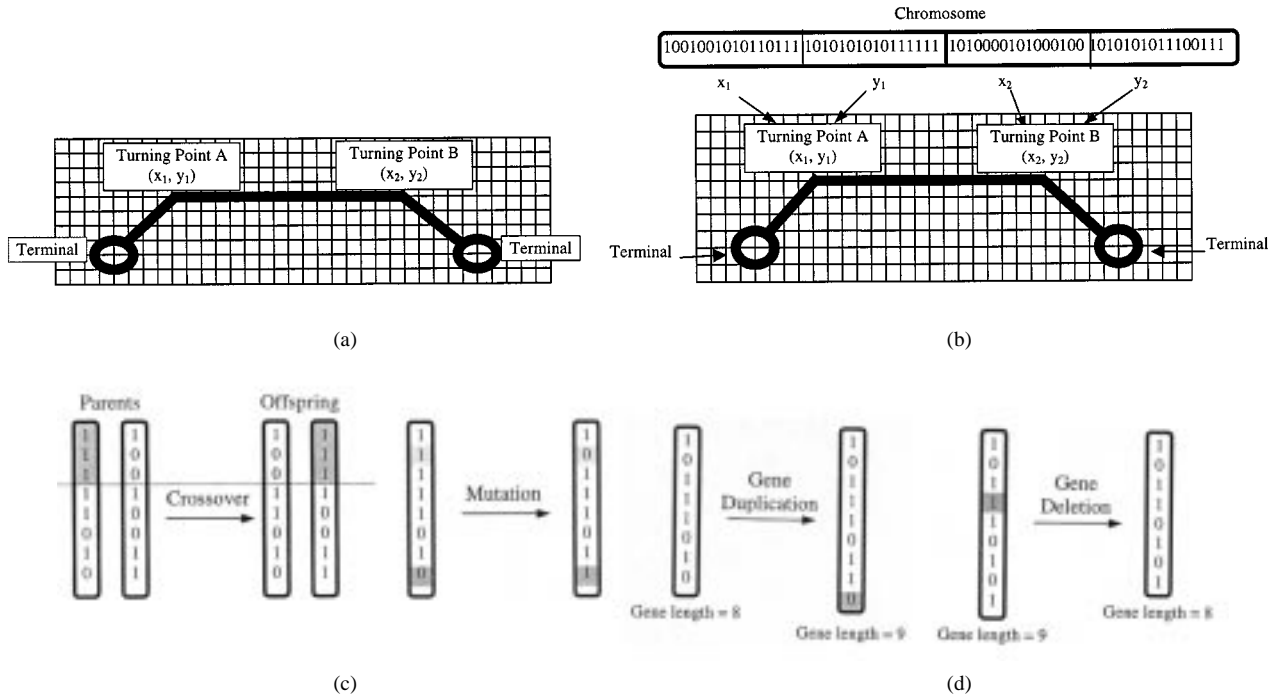


Fig. 2. (a) Representation of PCB trace by turning points between defined terminals. (b) Chromosome representation of a PCB trace between defined terminals. (c) Crossover and mutation. (d) Gene duplication and deletion.

index and capacitance calculation by FEA. The correlation coefficient obtained is 0.98, and this shows the coupling index is sufficient for switching power supply layout purposes.

III. OPTIMIZING TRACE LAYOUT USING GA

The GA is used to optimize layout of a victim trace with respect to the emission map from a noisy trace. The GA has been proven to be useful in solving many engineering problems, but it has not been applied to a PCB layout of power electronics circuits. Here, the GA is incorporated with the coupling index so established and a trace layout is proposed in a two-dimensional plane. The discussion in this letter concentrates on the layout of a victim trace in a field produced by a noisy node.

A method is developed to represent a trace on a PCB. A trace is divided into segments joined up by turning points. The more the turning points, the more flexible the layout of the trace is. It is assumed that the terminal points of the trace are fixed for predefined interconnections, while the turning points are placed using GA. Fig. 2(a) illustrates a simple example of a trace with two turning points. Each turning point (x, y) is called a *gene*, which is represented by two binary numbers. Here, each binary number has 16 bits. A PCB trace is made up of a collection of genes called a *chromosome*, which represents a trace layout. In this illustrative example, each chromosome has two genes. The contents of the genes may vary, so the turning points are free to be located within the boundary of the PCB. The width of the trace concerned is assumed fixed for simplicity.

A fitness function is needed to carry out the GA process. The objective of this application is to reduce the noise coupling level at a victim trace. Therefore, the coupling index of a victim trace in a field should be as low as possible. Here, a fitness function is defined as the inverse of the coupling index in

This fitness function can be calculated very quickly and provides quick online iteration with different chromosomes. The best solution can be obtained with maximum fitness and lowest coupling index.

New chromosomes can be spawned by many reproduction methods [14]. The tournament method of selection provides a good start. The method suggests selection of two chromosomes randomly from the gene pool regardless of their length, or the number of genes. The fitter of the two chromosomes becomes the first parent which dictates the length of the second parent to be selected. Two chromosomes are then randomly chosen from the gene pool to produce a second parent. They should have the same length as the first parent. Similarly, the fitter of the two becomes the second parent. Fig. 2(c) illustrates crossover and mutation. Crossover is the operation by which a certain number of bits is exchanged between parent chromosomes. Mutation is another operation whereby a bit within a chromosome may toggle to the opposite binary. Fig. 2(d) illustrates gene duplication and deletions. They are mechanisms employed to adjust the resolution of a gene. If the chromosome length is too short, it may not have enough resolution to converge to an optimal value, whereas an excessively long chromosome takes up computing resources unnecessarily. Gene duplication and deletion are considered as genetic disorders resulting in the formation of a slightly longer or shorter chromosome. The same concept is used in this optimization technique to reproduce chromosomes that are of a different length compared to their parents. In addition to these methods, genes are reordered from time to time to ensure that the resultant trace will not form loops within itself. This reordering process arranges the phenotype of the genes in ascending order in order to ensure convergence efficiency of the algorithm.

IV. IMPLEMENTATION TO A LAYOUT

An example illustrates the application of the process so described. Fig. 3(a) shows a switching power transistor with a rectangular TO220 package. It makes a noisy node and produces a field extended to its vicinity. Here, a victim trace has to be laid to join fixed terminals A_1 and A_2 . The victim trace is confined to a rectangular area. The objective of

$$K = \frac{1}{\text{Coupling Index } F}. \quad (2)$$

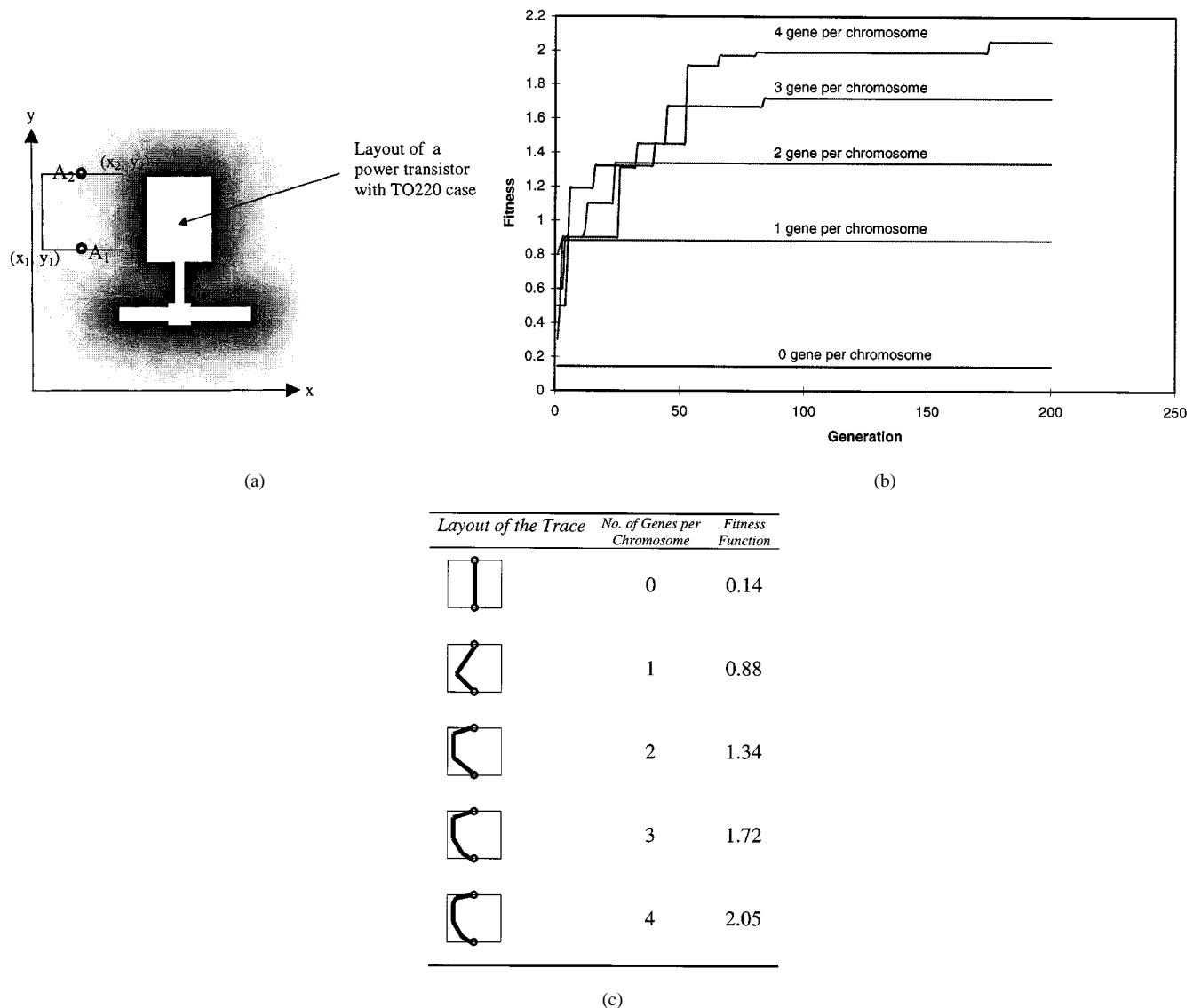


Fig. 3. (a) Field plot of the power transistor with TO220 package. (b) Result of GA. (c) Final result of trace layout with different number of turning points.

the exercise is to produce a layout of the victim trace with low influence from the noisy node.

The GA process is carried out. The process starts with 200 randomly produce chromosomes. The best half is taken for the process. Mutations and various methods are carried out to produce offspring. The evolution process shown in Fig. 3(b) shows that the chromosome fitness increases with the number of genes at the expense of computing resources. The final result and trace layout of the victim trace is given in Fig. 3(c). More genes or turning points provide more flexibility and better fitness function.

V. CONCLUSIONS

This letter has pointed out that electrical field coupling in a switching power supply makes a considerable contribution to total EMI emission. Proper PCB layout is the key to reduce interference between traces. A coupling index is introduced to indicate the coupling level between traces. A GA is applied and the coupling index produces a fitness function. A method to define a trace is presented which uses a number of turning points along the length of a trace. The locations of these turning points are refined by the GA. A design example was presented by which

the layout of a victim trace is optimized in the vicinity of a switching power transistor with standard TO220 package.

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An Improved Energy-Saving Scheme for Capacitor-Run Induction Motor

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Abstract—Conventionally, the speed of a capacitor-run single-phase induction motor is controlled by using an ac voltage controller (generally a triac) between the supply voltage and the motor. This letter proposes a new scheme, in which the triac is inserted in series with the main winding, while the motor auxiliary winding remains directly connected across the supply voltage. The experimental results indicate the superiority of the new method suggested in this letter.

Index Terms—Energy conservation, induction motors, phase control.

I. INTRODUCTION

Stator voltage control of induction motor drives is a cheaper and more reliable scheme of speed control and is widely employed [1]. Capacitor-run single-phase motors combined with stator voltage control are quite commonly used for domestic fans and low-power industrial applications. Generally, a triac is used for varying the stator voltage and to get variable speed. The triac-based controller is superior to a resistance-type controller due to increased energy saving and compactness. However, phase control results in reduced input power factor and increased line current harmonics. Improved performance can be obtained with ac chopper circuits, in which controlled freewheeling is adopted [2], [3]. The freewheeling action improves the input power factor significantly and further eliminates line current harmonic components. However, the complexity of the firing circuit and the cost of the devices used in ac chopper circuits prohibit their use as speed controllers for single-phase fan-type motors. This letter explains a new scheme for speed control of a single-phase fan motor using a triac, in which the triac is connected in series with the main winding and the auxiliary winding is directly connected across the supply voltage. The speed control is attained by changing the voltage applied to the main winding only. Thus, the auxiliary winding current is sinusoidal, resulting in reduced input current harmonics and improved motor efficiency. Experimental results are presented to validate the proposed method.

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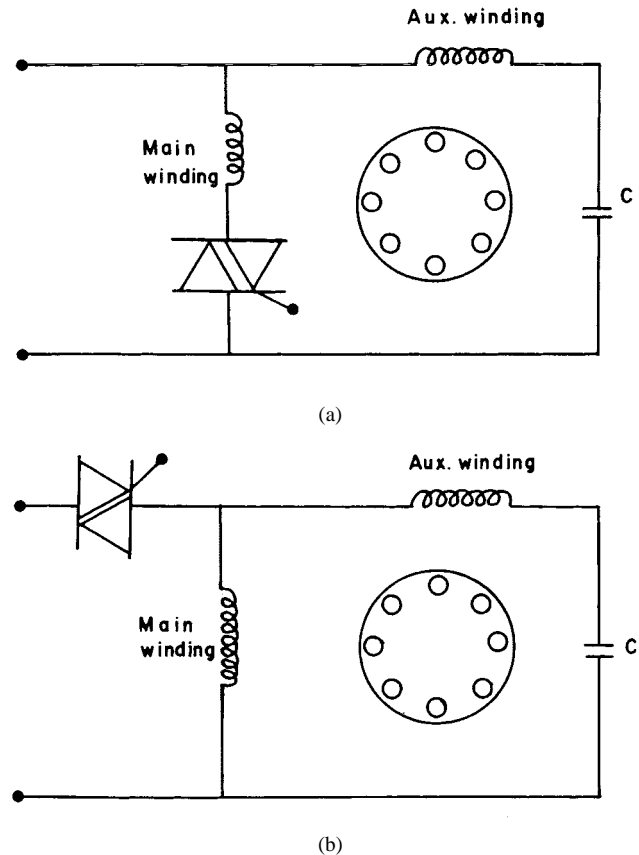


Fig. 1. (a) Proposed scheme for speed control. (b) Conventional scheme.

II. PROPOSED SCHEME

The proposed scheme for speed control of a capacitor-run motor is shown in Fig. 1(a). Fig. 1(b) shows the traditional way of using the triac for the speed control of the fan motor. From Fig. 1(a), it is evident that, in the proposed scheme, only the main winding current is interrupted. By varying the firing angle of the triac, the current through the main winding is controlled and, hence, different speeds are achieved. It may be noted that, in the proposed scheme, also, the triac turns off by natural commutation and, hence, there will not be any problem of large induced voltages due to current interruption.

A simple analytical approach for the proposed scheme is given below. Let I_i , I_m , and I_a be the input current, main winding current, and auxiliary winding current, respectively. Thus, using phasor addition,

$$I_i = I_m + I_a. \quad (1)$$

Further,

$$I_i = (I_l^2 + I_h^2)^{1/2} \quad (2)$$

where I_l is the rms value of the fundamental component and I_h is the rms value of the harmonic components.

For a given fan speed, let P_1 be the required fundamental power input. The total input power P_T is given by

$$P_T = P_1 + P_r + P_i + P_h + P_m \quad (3)$$

where

P_r copper loss due to fundamental;