

# Spreading-Resistance Temperature Sensor on Silicon-On-Insulator

P. T. Lai, Bin Li, C. L. Chan, and Johnny K. O. Sin, *Senior Member, IEEE*

**Abstract**—A spreading-resistance temperature (SRT) sensor is fabricated on silicon-on-insulator (SOI) substrate and achieves promising characteristics as compared with similar SRT sensor on bulk silicon wafer. Moreover, experimental results show that the maximum operating temperature of thin-film (1.2  $\mu\text{m}$ ) SOI SRT sensor can reach 450  $^{\circ}\text{C}$ , much higher than 350  $^{\circ}\text{C}$  of thick-film (10  $\mu\text{m}$ ) SOI SRT sensor under the same current level. With complete oxide isolation, this sensor structure can be potentially used in low-power integrated sensors operating at temperatures as high as 450  $^{\circ}\text{C}$ .

## I. INTRODUCTION

SILICON temperature sensors have been well studied in recent years because of their potential applications in various areas. Conventional silicon temperature sensors based on the positive temperature coefficient of resistance can only be used for temperatures below 200  $^{\circ}\text{C}$ , due to excessive thermal generation of charge carriers at intrinsic temperatures. Therefore, getting higher operating temperatures and integration of sensing elements is always the target of investigations. To achieve these goals, the spreading-resistance temperature (SRT) sensor shown in Fig. 1(a) has been proposed for over ten years [1], [2], and its maximum operating temperature can go up to 350  $^{\circ}\text{C}$ . Moreover, with the bottom electrode moved to the wafer surface, as in Fig. 1(b), the SRT sensor can be integrated with other devices and/or circuits on a small piece of silicon chip to form more complicated sensors [3].

The operating principle of the SRT sensor lies in the fact that the minority-carrier exclusion effect occurs at  $n^+$ - $n$  high-low junction under high current densities [4]. This effect suppresses the thermal generation of carriers and maintains extrinsic-carrier concentrations even at high temperatures, thereby increasing the maximum operating temperature of the device. One potential application of this novel SRT sensor in integrated flow sensor has been reported [3], [5]. However, with pn junctions as isolation between the SRT sensors, the chip cannot operate under ambient temperatures above 150  $^{\circ}\text{C}$ , due to high leakage current of the pn junctions. In this letter, silicon-on-insulator (SOI) with mesa isolation is adopted to eliminate the pn junctions and SRT sensors are fabricated on the silicon islands of the SOI wafer [6]. This new structure can also provide an extra dimension (silicon-film thickness) for optimizing the characteristics of the sensor. Experimental

Manuscript received May 10, 1999; revised July 19, 1999. This work was supported by the University of Hong Kong under Grants RGC and CRCG.

The authors are with the Department of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology, Hong Kong (e-mail: laip@hkueee.hku.hk).

Publisher Item Identifier S 0741-3106(99)08996-X.

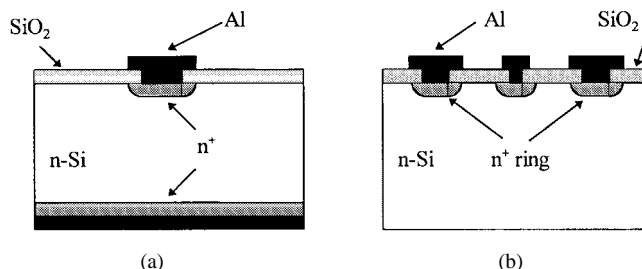


Fig. 1. (a) Cross section of traditional SRT sensor. (b) Cross section of novel SRT sensor.

results show that the maximum operating temperature of SOI SRT sensor can go up to 450  $^{\circ}\text{C}$  even when the device operates at low current levels.

## II. DEVICE FABRICATION

SRT sensors were fabricated on commercially available SOI wafers formed by the separation by implantation of oxygen (SIMOX) technique with an  $n$ -type  $\langle 100 \rangle$  silicon-film thickness of 10  $\mu\text{m}$  or 1.2  $\mu\text{m}$ , and a buried-oxide thickness of 0.4  $\mu\text{m}$ . Conventional bulk wafers were also processed by the same technology for the sake of comparison. The silicon film and the bulk wafer both had a resistivity of 10–20  $\Omega \cdot \text{cm}$ . A  $\text{SiO}_2$  layer with a thickness of 0.4  $\mu\text{m}$  was obtained by means of thermal oxidation at 1050  $^{\circ}\text{C}$  (15-min dry + 60-min wet + 15-min dry). The  $n^+$  regions in Fig. 1(b) with a junction depth of 0.8  $\mu\text{m}$  for the SRT sensors were formed by thermal diffusion of phosphorus at 1000  $^{\circ}\text{C}$  for 15 min. Then, 1  $\mu\text{m}$  of aluminum was evaporated as electrodes. Finally, post-metallization annealing was done at 450  $^{\circ}\text{C}$  for 30 min to make better contacts to the sensors. The sensor had a circular  $n^+$  region at the center, with a ring  $n^+$  region (inner and outer diameters were 200 and 300  $\mu\text{m}$ , respectively) surrounding it. The circular  $n^+$  region of the SRT sensor had a diameter of 20  $\mu\text{m}$ .

## III. RESULTS AND DISCUSSIONS

The sensor resistance versus temperature for different samples under constant-current condition is measured using a conventional temperature-controlled oven, with a bias current through the sensors ranging from  $-1$  mA to 4 mA. Figs. 2 and 3 depict the device resistance versus temperature at different current levels for thick-film SOI and bulk SRT sensors, respectively. In Fig. 2, the maximum operating temperature of the thick-film SOI SRT sensor is over 300  $^{\circ}\text{C}$  and increasing the bias current in the forward direction (the circular  $n^+$  region is

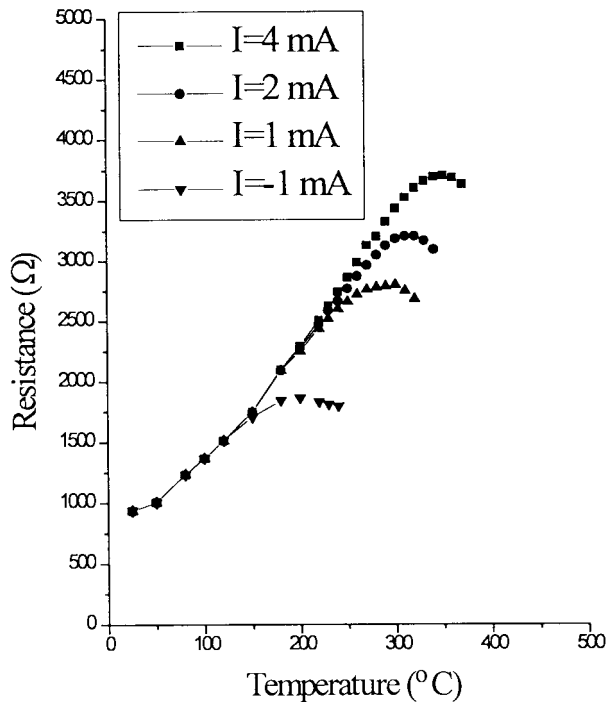


Fig. 2. Temperature dependence of the resistance of thick-film ( $10\ \mu\text{m}$ ) SOI SRT sensor biased at different current levels  $I$ .

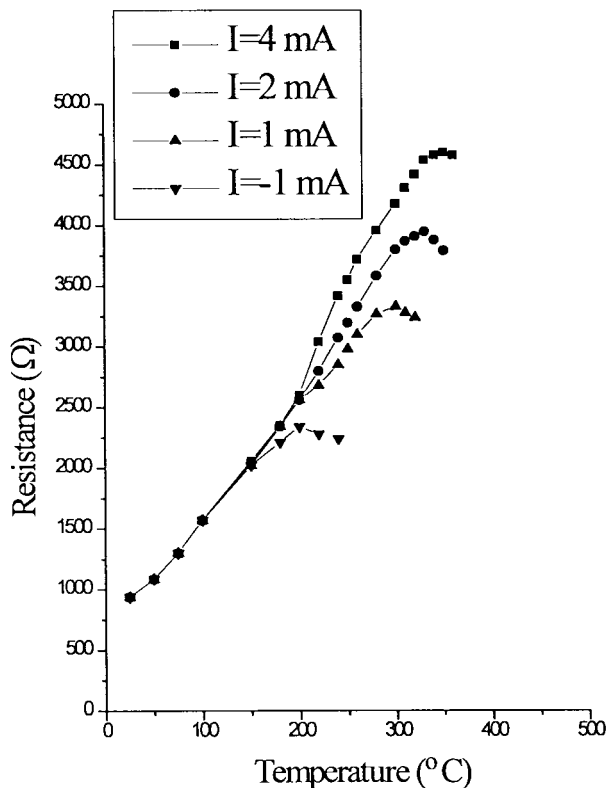


Fig. 3. Temperature dependence of the resistance of bulk SRT sensor biased at different current levels  $I$ .

at a higher potential than the ring  $n^+$  region) can increase the maximum operating temperature. On the other hand, with the bias current reversed, the maximum operating temperature is

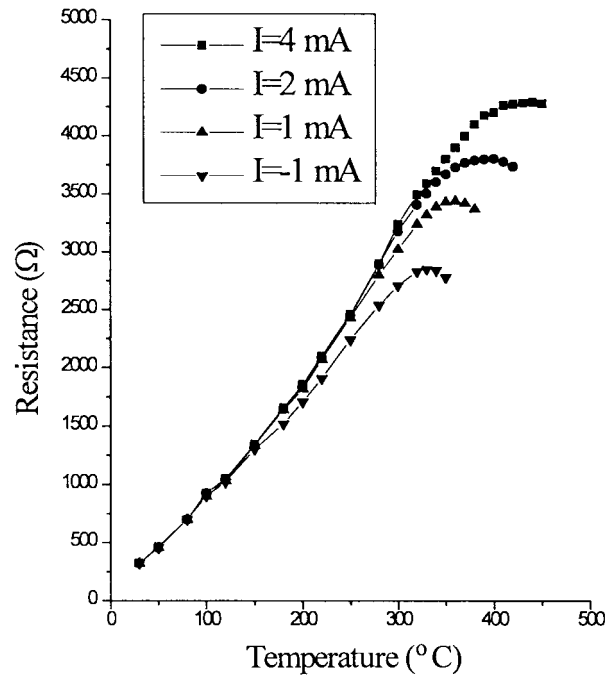


Fig. 4. Temperature dependence of the resistance of thin-film ( $1.2\ \mu\text{m}$ ) SOI SRT sensor at different current levels  $I$ .

only  $200\ ^\circ\text{C}$ , just like conventional resistor structure. When majority carriers flow from the lowly doped region to the highly doped region and minority carriers move in the opposite direction, the highly doped region cannot provide sufficient minority carriers to sustain an equilibrium minority-carrier flow in the lowly doped region. In other words, the electric field in the lowly doped region extracts minority carriers from the junction region faster than the highly doped region can supply. Consequently, the minority-carrier concentration near the junction decreases, resulting in the so-called *exclusion effect* [4]. When the current is reversed, the lowly doped region can supply enough minority carriers and hence, the device behaves like an ordinary diffused resistor. Moreover, a larger current can extract more minority carriers and remove more thermally generated minority carriers, thus raising the temperature at which thermal generation begins to take control on the sensor resistance. Similar results can also be obtained for the bulk SRT sensor in Fig. 3, indicating that the silicon film of the SOI SRT sensor has comparable quality and sufficient thickness to approximate the current flow in the bulk sensor.

Due to the special structure of the SOI SRT sensor, the thickness of the silicon film should significantly affect the resistance-temperature characteristics of the sensor. In Fig. 4, experiments on SOI wafers with a thinner silicon film indeed show a higher maximum operating temperature. For forward bias, the R-T characteristics of the thin-film SOI SRT sensor are similar to those of the thick-film SOI SRT sensor, but displays a maximum operating temperature as high as  $450\ ^\circ\text{C}$  under the same bias current of  $4\ \text{mA}$ . The resulting higher maximum operating temperature of the sensor is due to the fact that the thinner silicon film increases the current density, and thus enhances the exclusion effect. On the other

hand, for reverse bias, the maximum operating temperature is about 300 °C, higher than that of a conventional diffused resistor. This phenomenon indicates that the exclusion effect can happen in both current directions when the silicon film is sufficiently thin. One possible reason is that for very thin films, owing to the limited freedom in the vertical direction, the exclusion region (normally  $>10 \mu\text{m}$  [3]) has to extend more in the lateral direction, thus greatly enhancing the exclusion effect even for reverse bias.

#### IV. CONCLUSION

Preliminary results support the feasibility of making SRT sensors on SOI materials which can function at temperatures as high as 450 °C. The characteristics of the SOI SRT sensor compare favorably with those of SRT sensor fabricated on bulk wafer, and its complete oxide isolation makes it an

excellent temperature sensor, especially suitable for integration into more complex forms of sensors or devices.

#### REFERENCES

- [1] G. Raabe, "Silizium-temperature-sensoren von  $-50 \text{ }^\circ\text{C}$  bis  $+350 \text{ }^\circ\text{C}$ ," *NTG Fachberichte*, vol. 79, pp. 248–253, 1982.
- [2] S. R. in't Hout and S. Middelhoek, "400 °C silicon Hall sensor," *Sens. Actuators A*, vol. 60, pp. 14–22, 1997.
- [3] P. T. Lai and B. Liu, "Monolithic integrated spreading-resistance silicon flow sensor," *Sens. Actuators A*, vol. 58, pp. 85–88, 1997.
- [4] G. G. E. Low, "Carrier concentration disturbances in semiconductors," in *Proc. Phys. Soc. B*, 1955, vol. 68, pp. 310–314.
- [5] P. T. Lai and B. Liu, "A two-dimensional flow sensor using integrated silicon spreading-resistance temperature detectors," *Rev. Sci. Instrum.*, vol. 68, pp. 3785–3789, 1997.
- [6] P. T. Lai, B. Li, and C. L. Chan, "Spreading-resistance temperature sensor on SOI," in *Proc. IEEE Hong Kong Electron Device Meeting*, Hong Kong, Aug. 1998, pp. 148–151.
- [7] N. Arora, *MOSFET Models for VLSI Circuit Simulation*. New York: Springer-Verlag, 1993, p. 138.