A Novel Chip-Interleaving DS SS System

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Abstract—This paper proposes a chip-interleaving direct-sequence (DS) spread-spectrum (SS) system. Its performance is analyzed under ON–OFF wide-band jamming, and closed-form bit error rate (BER) performances of two special cases of the system are obtained. The behavior of the system under tone interference is also studied. The average signal-to-noise ratio of the system is given as a function of tone interference frequency, and the system BER performance under harmonic tone jamming is then investigated. The system is compared with a conventional system using numerical examples.

Index Terms—Chip-interleaving, direct-sequence spread-spectrum, jamming.

I. INTRODUCTION

A GREAT deal of natural noise as well as manmade electromagnetic interference are basically impulsive in nature. ON–OFF wide-band noise is a typical model for impulsive interference [2]–[8]. Since the wide-band noise is spectrally flat over the entire signal bandwidth, the direct-sequence (DS) spread-spectrum (SS) system cannot rely on its processing gain to suppress the jamming. Although burst error correcting coding together with coded bit interleaving can improve the system performance [8], coding, however, will certainly introduce redundancy to the system. Nonlinear noise suppression techniques such as amplitude limiters have been employed to suppress the impulsive noise [3], [6], [9]. Nevertheless, performance improvement by the amplitude limiters depends highly on the model of impulsive noise and appears insignificant under ON–OFF wide-band noise model [3], [6]. The concept of chip interleaving was first introduced by Tachikawa and Marubayashi [2]–[6] to the DS SS system used in power line communications to combat burst noise which was modeled by *periodic* ON–OFF wide band. In their system, the time intervals between the spreading chips are randomized by using multielements m-sequences or Tausworthe–Lewis–Payne (TLP) sequences and amplitude limiters are used [3], [5], [6]. Nevertheless, the system seems difficult to be analyzed. In this paper, a simpler chip-interleaving system is proposed and studied. Its closed-form bit error rate (BER) results of two special cases under burst noise are obtained. The results also provide performance bounds for general cases of the chip-interleaving system. Furthermore, analysis shows that the proposed chip-interleaving system is also resistant to

harmonic tone jamming if full period of m-sequence is used to spread each data bit.

The paper is organized as follows. Section II describes the chip-interleaving DS SS system. Performance analysis of the system under ON–OFF wide-band jamming is presented in Section III and the performance of the system under multiple tone jamming is investigated in Section IV. The effect of synchronization error on the performance of the system is analyzed in Section V. Numerical results are presented and compared with conventional DS SS system in Section VI. Finally, conclusions are drawn in Section VII.

II. SYSTEM MODEL

The major difference of the chip-interleaving DS SS system from the conventional DS SS system is the order in which chips are transmitted. Let $\mathbf{B}^{(h)} = [b_1^{(h)} \ b_2^{(h)} \ \ldots \ b_M^{(h)}]$, $\mathbf{A}^{(i)} = [a_1^{(i)} \ a_2^{(i)} \ \ldots \ a_L^{(i)}]$, where $b_1^{(h)} b_2^{(h)} \ldots b_M^{(h)}$ is the sequence of data bits of the hth data block and $a_1^{(i)} a_2^{(i)} \ldots a_L^{(i)}$ is the spreading sequence of the ith data bit of a data block, M is the number of data bits per data block and L is the number of spreading chips per data bit, i.e., processing gain (PG). If the bit duration and chip duration are denoted by T_b and T_c respectively, then $L = T_b/T_c$. Define

$$\mathbf{D} = \begin{bmatrix} b_1^{(h)}\mathbf{A}^{(1)} \\ b_2^{(h)}\mathbf{A}^{(2)} \\ \vdots \\ b_M^{(h)}\mathbf{A}^{(M)} \end{bmatrix} = \begin{bmatrix} d_{11} & d_{12} & \cdots & d_{1L} \\ d_{21} & \ddots & & d_{2L} \\ \vdots & & \ddots & \vdots \\ d_{M1} & d_{M2} & \cdots & d_{ML} \end{bmatrix} \quad (1)$$

where d_{ij} is actually the sequence being sent out. The emphasis here is the order of sending $\mathbf{D}$. Conventional system transmits the contents of $\mathbf{D}$ row by row, left to right, while the proposed system transmits them column by column, top to bottom. To be specific, the sequence it sends out can be written as $d_{11}d_{21}\ldots d_{M1}d_{12}\ldots d_{M2}\ldots d_{1L}\ldots d_{ML}$. Thus, the adjacent chips of the same data bit is separated by $M-1$ chips from $M-1$ different information bits. A block diagram of the transceiver of the proposed system is shown in Fig. 1. On the transmission side in the first MT_c interval, the switch rotates from contact to contact every T_c s, the resulting sequence of M data chips is multiplied by the first chip of their spreading sequence, respectively, and transmitted. The transmitter then repeats the same procedure in the second, third, etc., until the Lth MT_c interval. On the receiving side, the switch rotates synchronously with the transmitter, deinterleaves and despreads the received sequel of chips to recover the M data bits at the end of $LMT_c = MT_b$ interval. Finally, the data stream is obtained through parallel to serial device. Thus, the system transmits M information bits in MT_b duration, with processing
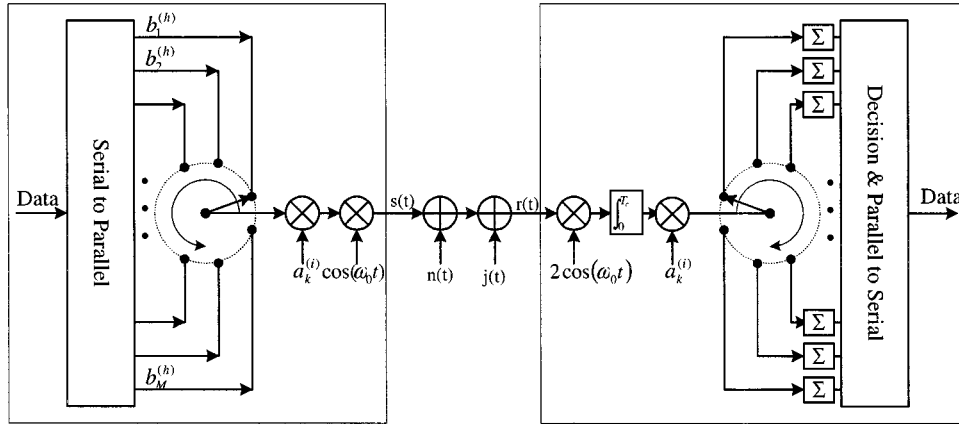
Fig. 1.   The proposed chip-interleaving DS SS system.

gain L which is the same as that of conventional system. It is easy to see that when M is equal to one, the system reduces to the conventional system.

Note that in the chip-interleaving system described above, the time intervals between neighboring chips of the same data bit are identical and the order of chips is not changed, hence the system can be called periodic chip-interleaving system (PCIS). In comparison, the chip-interleaving system proposed by Tachikawa and Marubayashi [3], [5] tries to randomize the time intervals between chips of the same data bit by using delay sequences such as multielements m-sequences or TLP sequences. The order of chips is also changed, i.e., for example, the third chip could be sent out before the second chip. Hence, it is appropriate to refer their system as random chip-interleaving system (RCIS) in order to distinguish it from the proposed system. It is worth to point out that in RCIS, the interleaving pattern is actually fixed once the delay sequence is selected. Though the PCIS appears similar to the special case of the RCIS given in [2], there are several differences between these two systems: 1) the order of chips is changed in the RCIS; 2) the special case of the RCIS exists only when the processing gain is a prime number; and 3) the interleaving pattern can be easily changed during transmission in the PCIS by changing the parameter M while that of RCIS will be difficult to change.

The SS signal transmitted by the proposed system using BPSK modulation can be mathematically represented by

$$s(t) = \sqrt{2P} \sum_{h=-\infty}^{\infty} \sum_{i=1}^{M} b_i^{(h)}$$
$$\cdot \sum_{k=1}^{L} a_k^{(i)} u_{T_c}(t - (hML + kM + i - 1)T_c) \cos(\omega_0 t) \tag{2}$$

where

$$u_{T_c}(t) = \begin{cases} 1, & -MT_c \leq t \leq (-M+1)T_c \\ 0, & \text{elsewhere.} \end{cases}$$

P and ω_0 are the power and carrier frequency of the DS SS signal, respectively. The acquisition and tracking of the chip-interleaving DS SS system have been discussed in [4] and [5] and

the synchronization technique for conventional DS SS system is applicable to the proposed system as well, where the principle employed is the same. Hence, in the following analyses to be presented in Sections III and IV, we will neglect the effect of synchronization error and assume perfect synchronized reception for simplicity of presentation. The effect of synchronization error on the performance of the proposed system will be addressed in Section V.

III. ON–OFF WIDE-BAND JAMMING

We now proceed to examine the system performance under ON–OFF wide-band jamming. The jammer model was described in [7] which is the same as that used in [6]. It is assumed that the noise produced by the jammer is also white Gaussian with increased power spectral density. The jammer operates *periodically* with ON duration xT_b and OFF duration yT_b. In other words, x and y are jammer's ON duration and OFF duration normalized to T_b, respectively. When the jammer is ON, the spectral power density of the noise is σ_j^2, when it is OFF, the noise reduces to background noise with variance σ_0^2, and $\sigma_j^2 \gg \sigma_0^2$. Obviously, the assumption of jamming being *periodic* may not be valid in real situations. However, the assumption allows the analysis of two special cases whose closed-form BER results can be obtained and helps to provide insight on the proposed system performance under ON–OFF wide-band jamming. Generalization to more realistic model of ON–OFF wide-band jamming will be discussed at the end of this section.

For brevity we consider the case that T_c is less than or equal to xT_b and yT_b, i.e., $x \geq 1/L$ and $y \geq 1/L$. For cases that T_c is larger than xT_b and/or yT_b, interested readers are referred to [7] for analysis of various combinations of T_c, xT_b and yT_b (with T_b in [7] replaced by T_c, analogous results can be easily obtained following the discussion in [7]). Results in [7] indicate that the analyses of different combinations of T_b, xT_b and yT_b on conventional DS SS system are similar and our current study on the proposed system also comes to similar conclusion. We define function $m_k(s)$ as the fraction in the kth chip duration of a data bit that the jammer is ON, where s is the distance of the starting edge of the first chip of a data bit from the starting edge of the jamming noise as shown in Fig. 2. From the figure,
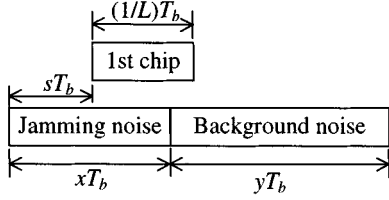
Fig. 2. Distance s between starting edges of jamming noise and first chip of a data bit.

we see that $m_k(s)$ is a periodic function with minimum period $x + y$. Note that $m_k(s)$ and s are all normalized to T_b. For the first chip of a data bit, $m_1(s)$ can be obtained analogously as in *case 1a* of [7] and can be written as

$$m_1(s) = \begin{cases} 1/L, & 0 \le s \le x - 1/L \\ x - s, & x - 1/L \le s \le x \\ 0, & x \le s \le x + y - 1/L \\ s - (x + y - 1/L), & x + y - 1/L \le s \le x + y. \end{cases} \tag{3}$$

Note in [7] that $m(s)$ is defined as the fraction in a bit duration that the jammer is ON and s is the starting edge of a data bit from the starting edge of the jamming noise. In the proposed system, adjacent chips of the same information bit are separated with distance $(M/L)T_b$. Therefore, the portion of an information bit being affected by the jammer is found to be

$$\tilde{m}(s) = \sum_{k=1}^{L} m_k(s) = \sum_{k=1}^{L} m_1\left(s + (k-1) \cdot \frac{M}{L}\right). \tag{4}$$

For a partially jammed BPSK signal, its probability of error is

$$P_e = 0.5 \operatorname{erfc}\left(\sqrt{\overline{\gamma_b}}\right) \tag{5}$$

where

$$\overline{\gamma_b} = PT_b / \left((1 - \tilde{m}(s))\sigma_0^2 + \tilde{m}(s)\sigma_j^2\right). \tag{6}$$

Assuming the starting time of the jammer is random, s has a uniform distribution over the interval $[0, x + y]$. The proposed system performance can be calculated by averaging the P_e of (5) over s, i.e.,

$$P_b = \frac{1}{x + y} \int_0^{x+y} 0.5 \operatorname{erfc}\left(\sqrt{\frac{PT_b}{(1 - \tilde{m}(s))\sigma_0^2 + \tilde{m}(s)\sigma_j^2}}\right) ds. \tag{7}$$

In general, the explicit expression of $\tilde{m}(s)$ is unknown and we cannot obtain closed-form expression for (7). Obviously, on average $\rho = x/(x+y) \times 100\%$ of the chips will be jammed under the periodic ON–OFF jamming, where ρ is jammer's duty cycle. For low duty cycle jamming, i.e., the jammer's OFF duration yT_b is much longer than its ON duration xT_b, it is easy to see that the system performance depends on the distribution of the jammed chips in data bits. Contrary to the conventional system, we can change this distribution by adjusting the interleaving parameter M in the proposed system. A special case is to have an uniform distribution of the jammed chips in all data bits. In other words, the system distributes the chips of a data bit evenly over the jamming period $x+y$ by proper selection of M. We refer to this case as *Case A*. Under this situation, each information bit is jammed

with approximately $T_b x/(x + y)$ s, which is proportional to the jammer's duty cycle, and (4) can be approximated by

$$\tilde{m}(s) = x/(x + y). \tag{8}$$

Substituting (8) into (7), we obtain

$$P_b = 0.5 \operatorname{erfc}\left(\sqrt{\frac{PT_b}{(y\sigma_0^2 + x\sigma_j^2)/(x + y)}}\right). \tag{9}$$

If we define $\sigma^2 = (y\sigma_0^2 + x\sigma_j^2)/(x + y)$ to be the average noise power density, (9) can be rewritten as

$$P_b = 0.5 \operatorname{erfc}\left(\sqrt{PT_b/\sigma^2}\right). \tag{10}$$

Another special case, *Case B*, occurs when M/L is an integer multiple of $x + y$, i.e., all the chips of the same data bit are virtually located at the same position of the jamming period which results in extreme uneven distribution of jammed chips in data bits. If $(M/L)T_b$ is an integer multiple of jammer period $(x + y)T_b$, we obtain from (3) and (4)

$$\tilde{m}(s) = \sum_{k=1}^{L} m_1\left(s + (k-1) \cdot \frac{M}{L}\right) = L \cdot m_1(s)$$

$$= \begin{cases} 1, & 0 \le s \le x - 1/L \\ L(x - s), & x - 1/L \le s \le x \\ 0, & x \le s \le x + y - 1/L \\ Ls - L(x + y - 1/L), & x + y - 1/L \le s \le x + y. \end{cases} \tag{11}$$

Substituting (11) into (7), we finally obtain

$$P_b = (\bar{w}_0 P_0 + \bar{w}_j P_j + \bar{w}_0' P_0' + \bar{w}_j' P_j')/(x + y) \tag{12}$$

where

$$P_0 = 0.5 \operatorname{erfc}\left(\sqrt{PT_b/\sigma_0^2}\right)$$
$$P_j = 0.5 \operatorname{erfc}\left(\sqrt{PT_b/\sigma_j^2}\right)$$
$$P_0' = 0.5 \exp\left(-PT_b/\sigma_0^2\right)$$
$$P_j' = 0.5 \exp\left(-PT_b/\sigma_j^2\right)$$
$$\bar{w}_0 = y - \frac{1}{L} - \frac{1}{L} 2 \cdot \frac{\sigma_0^2 + 2PT_b}{\sigma_j^2 - \sigma_0^2}$$
$$\bar{w}_j = x - \frac{1}{L} + \frac{1}{L} 2 \cdot \frac{\sigma_j^2 + 2PT_b}{\sigma_j^2 - \sigma_0^2}$$
$$\bar{w}_0' = \frac{1}{L} \frac{4}{\sqrt{\pi}} \cdot \frac{PT_b}{\sigma_j^2 - \sigma_0^2} \sqrt{\frac{\sigma_0^2}{PT_b}}$$
$$\bar{w}_j' = -\frac{1}{L} \frac{4}{\sqrt{\pi}} \cdot \frac{PT_b}{\sigma_j^2 - \sigma_0^2} \sqrt{\frac{\sigma_j^2}{PT_b}}. \tag{13}$$

As mentioned before, for a more realistic jamming model the ON–OFF duration should be random variable. Hence, *Case A* and *Case B* are two extreme cases and never happen under random ON–OFF jamming. However, these two extreme cases provide useful indications on the proposed system BER performance under impulsive wideband jamming. Furthermore, when the interleaving parameter M is large, the chips of a data bit

can be considered being uniformly distributed over jammer's ON–OFF duration and *Case A* is approximated.

IV. HARMONIC TONE JAMMING

In this section, we assume m-sequence is used in the system and each data bit is spreaded by full period of the m-sequence. Consider an AWGN channel and a multitone jammer, the received signal $r(t)$ can be written as

$$r(t) = s(t) + j(t) + n(t) \tag{14}$$

where $s(t)$ is the transmitted signal defined in (2), $n(t)$ is AWGN with unilateral power spectral density σ_0^2, and $j(t)$ is the multitone jammer given by

$$j(t) = \sum_{l=1}^{K-1} \sqrt{2J_l} \cos((\omega_0 + \delta\omega_l)t + \theta_l) \tag{15}$$

where $K - 1$ is the number of tones, $J_l, \delta\omega_l, \theta_l$ are the power, frequency offset and phase of the lth tone jammer, respectively, and θ_l's are mutually independent random variables uniformly distributed on $[0, 2\pi]$. If we set

$$\delta\omega_l = \frac{l}{K} \cdot \frac{B_s}{2} \tag{16}$$

the tones are evenly spaced over the region $(0, B_s/2)$, where $B_s = 2T_c^{-1} \cdot 2\pi$ is the SS bandwidth measured in radians. We call this type of multitone jammer harmonic jammer. When $K = 2$, (15) reduces to a single tone.

Assuming perfectly synchronized reception, the decision variable for a particular data bit, say $b_1^{(0)}$, can be written as

$$U = \sum_{k=1}^{L} a_k^{(1)} \int_{(k-1)MT_c}^{((k-1)M+1)T_c} r(t) \cdot 2\cos(\omega_0 t) \, dt. \tag{17}$$

For simplicity of notations, we will drop the superscript of $a_k^{(1)}$ in what follows. If assume a "one" is transmitted, using (2), (14), and (15), (17) can be simplified to

$$U = \sqrt{2P}T_b + I + N \tag{18}$$

where N is due to the channel thermal noise $n(t)$ and is a zero mean Gaussian random variable with variance $\sigma_0^2 T_b$. The term I of the right-hand side (RHS) of (18) is given by

$$I = \sum_{l=1}^{K-1} H_l \sum_{k=1}^{L} a_k \cos\left((k-1)M\delta\omega_l T_c + \frac{\delta\omega_l T_c}{2} + \theta_l\right) \tag{19}$$

where H_l is a factor caused by the integrate-and-dump circuit

$$H_l = \frac{T_c\sqrt{2J_l}\sin(\delta\omega_l T_c/2)}{\delta\omega_l T_c/2}. \tag{20}$$

Since it is generally impossible to obtain the probability distribution of I, the BER performance of the system can only be evaluated numerically. For analysis purposes, we use average signal-to-noise ratio (SNR) to obtain an indication of system performance versus $\delta\omega_l$, based on the fact that average SNR is a good performance index. The average SNR is defined by

$$\text{SNR} = \frac{1}{2} \cdot \frac{[E(U)]^2}{\text{Var}(U)}. \tag{21}$$

The problem then reduces to finding the mean and variance of I. Since θ_l's are mutually independent random variables uniformly distributed over $[0, 2\pi]$, the mean of I is zero, and the variance of I can be expressed as

$$\text{Var}(I)$$
$$= E(I^2) = \sum_{l=1}^{K-1} \frac{H_l^2}{2} E\left(\sum_{k=1}^{L}\sum_{h=1}^{L} a_k a_h \cos((k-h)\delta\omega_l MT_c)\right). \tag{22}$$

Note the RHS of (22) is the result already averaged over $\{\theta_l, l = 1, 2, \ldots, K-1\}$. We have to average the RHS of (22) over the ensemble of length L m-sequences in order to obtain the variance of I. By using the autocorrelation property of m-sequence, we obtain (details are omitted due to space limit) a simple expression for $\text{Var}(I)$ as follows:

$$\text{Var}(I) = \sum_{l=1}^{K-1} \frac{H_l^2}{2}\left(L + 1 - \frac{1}{L}\left(\frac{\sin(LM\delta\omega_l T_c/2)}{\sin(M\delta\omega_l T_c/2)}\right)^2\right). \tag{23}$$

It follows that the average SNR is given by (24) at the bottom of the page. As the jammer is harmonic and by using (16), (24) can be simplified to (25), given at the bottom of the page. We can maximize the SNR by setting M to be integer multiples of K in (25), and the maximum SNR is

$$\text{SNR}_{\max} = \frac{PT_b}{\sigma_0^2 + \frac{T_c}{L}\sum_{l=1}^{K-1} J_l\left(\frac{\sin(l\pi/K)}{l\pi/K}\right)^2}. \tag{26}$$

In this case, the average BER of the system can also be derived similarly to [1] as given in the following.

$$\text{SNR} = \frac{PT_b}{\sigma_0^2 + \sum_{l=1}^{K-1} J_l T_c\left(\frac{\sin(\delta\omega_l T_c/2)}{\delta\omega_l T_c/2}\right)^2\left(1 + \frac{1}{L} - \frac{1}{L^2}\left(\frac{\sin(LM\delta\omega_l T_c/2)}{\sin(M\delta\omega_l T_c/2)}\right)^2\right)} \tag{24}$$

$$\text{SNR} = \frac{PT_b}{\sigma_0^2 + \sum_{l=1}^{K-1} J_l T_c\left(\frac{\sin(l\pi/K)}{l\pi/K}\right)^2\left(1 + \frac{1}{L} - \frac{1}{L^2}\left(\frac{\sin(LMl\pi/K)}{\sin(Ml\pi/K)}\right)^2\right)} \tag{25}$$

Using the definitions of $\delta\omega_l$ and B_s under harmonic jamming conditions, (19) and (20) can be rewritten as

$$I = \sum_{l=1}^{K-1} H_l \sum_{k=1}^{L} a_k \cos\left((k-1)\frac{M}{K} \cdot 2l\pi + \frac{l\pi}{K} + \theta_l\right) \quad (27)$$

$$H_l = \frac{T_c\sqrt{2J_l}\sin(l\pi/K)}{l\pi/K}. \quad (28)$$

Since M is an integer multiple of K, (27) can be simplified to

$$I = -\sum_{l=1}^{K-1} H_l \cos\left(\frac{l\pi}{K} + \theta_l\right) \quad (29)$$

by using the autocorrelation property of m-sequence. Therefore, the decision variable U is a Gaussian random variable conditioned on $\{\theta_l, l = 1, 2, \ldots, K-1\}$ with conditional mean

$$E(U \mid \{\theta_l, l = 1, 2, \ldots, K-1\})$$
$$= \sqrt{2P}T_b - \frac{T_b}{L}\sum_{l=1}^{K-1}\frac{\sqrt{2J_l}\sin(l\pi/K)}{l\pi/K}\cos\left(\frac{l\pi}{K} + \theta_l\right) \quad (30)$$

and variance

$$\mathrm{Var}(U) = \sigma_0^2 T_b. \quad (31)$$

Hence, the system average BER is found to be

$$\text{BER}$$
$$= \frac{1}{(2\pi)^{K-1}}\int_0^{2\pi}\int_0^{2\pi}\cdots\int_0^{2\pi}$$
$$\cdot \frac{1}{2}\mathrm{erfc}\left(\frac{\sqrt{PT_b} - \frac{\sqrt{T_b}}{L}\sum_{l=1}^{K-1}\sqrt{J_l}\frac{\sin(l\pi/L)}{l\pi/K}\cos\left(\frac{l\pi}{K}+\theta_l\right)}{\sigma_0}\right)$$
$$\cdot d\theta_l\, d\theta_2 \ldots d\theta_{K-1}. \quad (32)$$

Equation (32) can be evaluated numerically.

V. IMPERFECT SYNCHRONIZATION

As mentioned before, the above results obtained are based on the assumption of perfect synchronized reception. However, precise synchronism is difficult to achieve in applications such as wireless communications. We investigate the effect of synchronization error on the performance of the proposed system in this section. Denoting the synchronization error as εT_c, where $\varepsilon \in [0, 1]$, and assuming an additive white Gaussian noise (AWGN) channel with unilateral noise power spectral density σ_0^2, the decision variable for the reference data bit, say $b_1^{(0)}$, can be written as

$$Z = \sqrt{2P}T_b(1-\varepsilon)b_1^{(0)} + \eta + N \quad (33)$$

where N is due to the AWGN and it is easy to show that N is a zero mean Gaussian random variable with variance $\sigma_0^2 T_b$. The

imperfect synchronization introduces an interfering term η from the neighboring data bit $b_2^{(0)}$ and η is given by

$$\eta = \sqrt{2P}T_c\varepsilon b_2^{(0)}\sum_{k=1}^{L}a_k^{(1)}a_k^{(2)}. \quad (34)$$

If random spreading sequence is employed, $\{a_k^{(2)}, k = 1, 2, \ldots, L\}$ in (34) are independent random variables taking values of either $+1$ or -1 with equal probability. From (33) it is obvious that the BER of the proposed system is 0.5 when $\varepsilon = 1$. For $\varepsilon < 1$, the BER of the proposed system is given by

$$\text{BER} = 0.5\,\mathrm{Prob}\{Z \le 0 \mid b_1^{(0)} = +1\}$$
$$+ 0.5\,\mathrm{Prob}\{Z > 0 \mid b_1^{(0)} = -1\}$$
$$= 0.5 - 0.5\,\mathrm{Prob}\left\{-1 < \frac{\eta + N}{\sqrt{2P}T_b(1-\varepsilon)} \le 1\right\} \quad (35)$$

where $\mathrm{Prob}\{\}$ stands for *the probability of*. Using characteristic-function (CF) method, (35) can be rewritten as

$$\text{BER} = 0.5 - \frac{1}{\pi}\int_0^\infty \frac{1}{v}\sin(v)\cos^L\left(\frac{\varepsilon}{L(1-\varepsilon)}v\right)$$
$$\cdot \exp\left(-\frac{\sigma_0^2}{4PT_b(1-\varepsilon)^2}v^2\right)dv. \quad (36)$$

Equation (36) can be evaluated numerically. When the PG L is large, the random variable η given by (34) is approximately Gaussian according to the central limit theorem. The mean of η is zero and the variance is

$$\mathrm{Var}(\eta) = 2P\varepsilon^2 T_c^2 L = 2PT_b^2\varepsilon^2/L. \quad (37)$$

Therefore, the system BER can be approximated by

$$\text{BER} \approx 0.5\,\mathrm{erfc}\left(\sqrt{\frac{PT_b(1-\varepsilon)^2}{\sigma_0^2 + 2PT_b\varepsilon^2/L}}\right) \quad (38)$$

where $\mathrm{erfc}()$ is the complementary error function. Compare (38) with the BER of the system with perfect synchronization given by $\varepsilon = 0$, we can conclude that for large PG the imperfect synchronization merely reduces the useful signal energy and increases the white noise power. This is particularly the case when ε is small and the second order term of ε in the denominator can be ignored.

VI. NUMERICAL RESULTS

We first compare the proposed system performance to that of conventional system under ON–OFF wide-band jamming. System parameters are chosen as follows: the jammer power $\sigma_j^2 = 100$, background noise power $\sigma_0^2 = 1$, processing gain $L = 7$, jammer ON duration $x = 4.5$ and jammer OFF duration $y = 10.5$, the corresponding duty cycle $\rho = 30\%$. In Fig. 3, we plot the system BER performance versus signal-to-jamming-noise ratio (SJR) PT_b/σ_j^2. Using the results obtained in Section III, we calculate the *Case A* and *Case B* performance of the proposed system under *periodic* ON–OFF wide-band jamming. The performance of conventional system under such situation is also evaluated using the analytical result of [7]. As
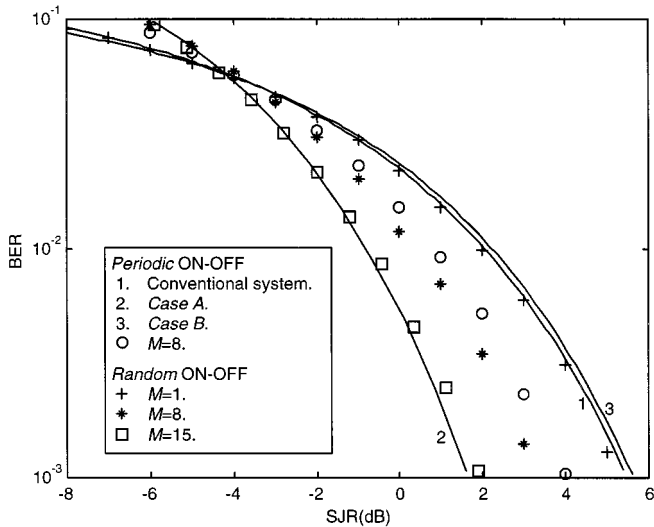
Fig. 3.   BER performance of the proposed system and conventional system under ON–OFF wide-band jamming.
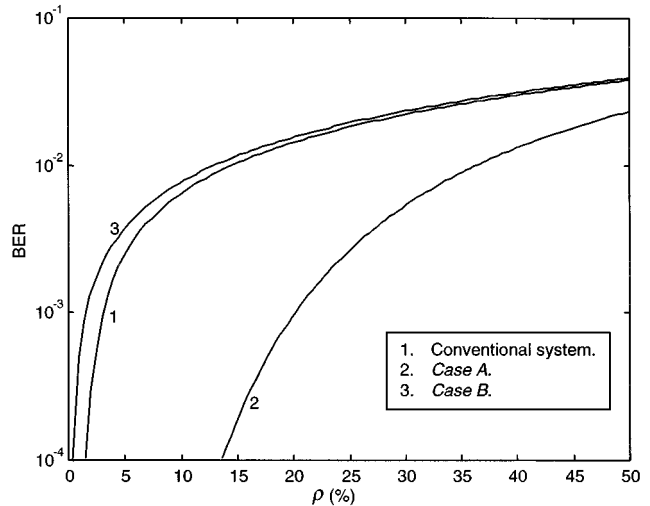

Fig. 4.   BER performance of the proposed system and conventional system versus jamming duty cycle.
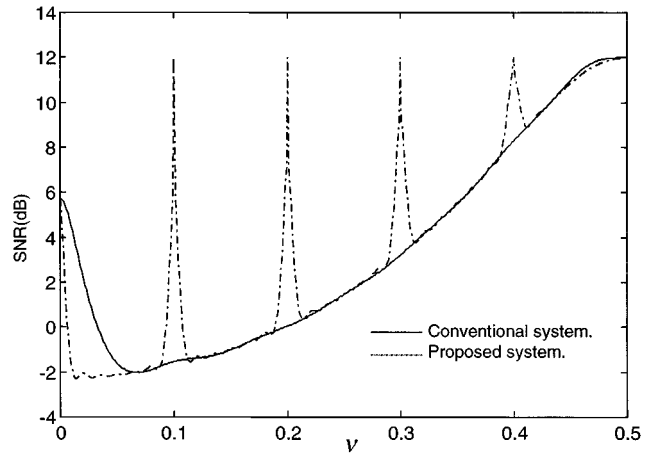

Fig. 5.   SNR versus ratio of tone frequency offset to the bandwidth of SS signal (v).
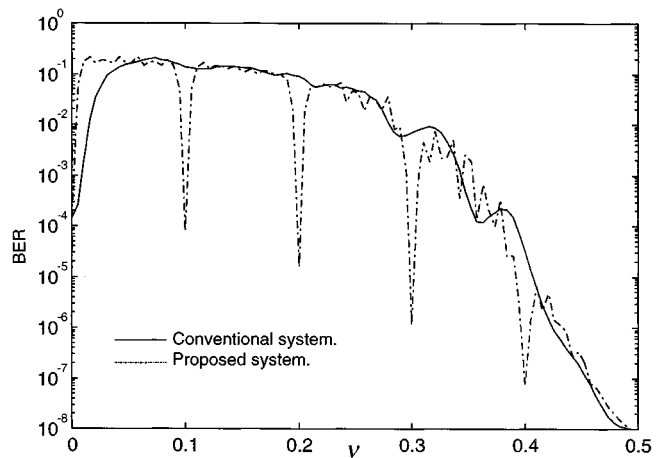

Fig. 6.   System BER performance versus ratio of tone frequency offset to the bandwidth of SS signal (v).

shown in Fig. 3, the BER of *Case B* is similar to that of conventional system while the *Case A* performance is much better. Monte Carlo simulations are also carried out for the proposed system with $M = 8$ under periodic ON–OFF jamming, and with $M = 1, 8, 15$ under *random* ON–OFF jamming, respectively. For the *random* ON–OFF jamming, the ON duration and OFF duration are simulated as random variables uniformly distributed over the $\pm 20\%$ region of $x = 4.5$ and $y = 10.5$, respectively. A number of 1×10^5 data bits are generated in each simulation. Note for $M = 1$, the proposed system reduces to the conventional system. We can see from the figure that the conventional system performs similarly under either random or *periodic* ON–OFF jamming, and the performance of the proposed system under *random* ON–OFF jamming gets closer to that of *Case A* as M increases. Another conclusion can be drawn from the figure is that the two special cases, namely *Case A* and *B*, actually provide lower and upper bounds for the performance of the proposed system with the SJR above a certain threshold (≈ -3 dB in this example). In Fig. 4, the BER's of conventional system as well as *Case A* and *B* of the proposed system are plotted against the jamming duty cycle ρ, where the parameters are held the same as the previous example with fixed ON–OFF period $x + y = 15$ and SJR $= 0$ dB. It is clear from the figure that much better performance can be achieved by the proposed system at low jamming duty cycle.

Next, we investigate the system performance under tone jammers. In the rest of this section, the following parameters are used in the computation: the total interference to signal power ratio J/P is fixed at 10 dB, signal to background noise ratio PT_b/σ_0^2 is set at 12 dB, processing gain is chosen as $L = 7$. In Fig. 5, we compare the average SNR versus the ratio of tone frequency offset to the bandwidth of SS signal (v) by using (24) of the proposed system to that of the conventional system. Since we are interested in the sensitivity of the system to the tone frequency, only single tone is considered. This is achieved by setting $K = 2$ in (24). The curves for the conventional system and the proposed system are obtained by setting $M = 1$ and $M = 5$ in (24), respectively. As shown in the figure, the proposed system has $M - 1 = 4$

peaks in the half bandwidth of the SS signal indicating that the system will outperform conventional system when tone jammers are located at these particular frequencies. It is also seen from the
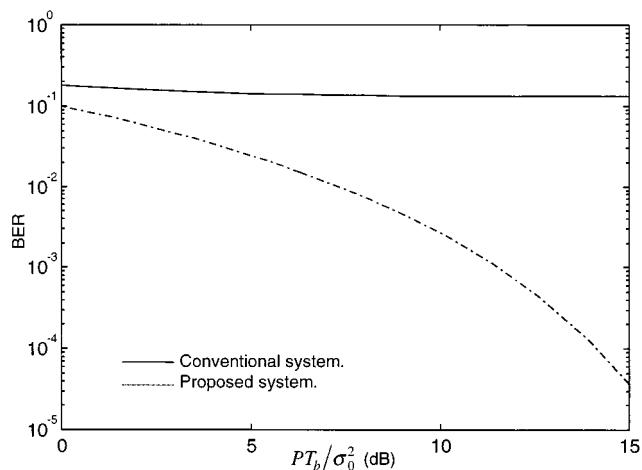
Fig. 7. System BER performance under two-tone interferers located at $v = 1/6$ and $v = 1/3$, respectively.

wide-band jamming and can be robust under harmonic tone jamming when properly designed.

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figure that when the single tone is located at the carrier frequency of the signal, system has a higher SNR. This observation coincides with the discussion in [1, part III]. The results of Fig. 5 are confirmed in Fig. 6, where we plotted the BER performances of both conventional system and the proposed system versus a single tone frequency offset. The BER's of both the conventional and the proposed systems are obtained by first calculating the conditional BER conditioned on the m-sequence and the tone phase, then averaging the conditional BER over the ensemble of m-sequence and tone phase. We chose a small processing gain $L = 7$ in the evaluation due to the large calculation burden required for larger values of L. As a second example, We evaluate the performance of the proposed system under two-tone equal-power harmonic interferer located at $v = 1/6$ and $v = 1/3$. Here, M is chosen equal to three and the total interference power to signal power ratio is still fixed at 10 dB. In Fig. 7, BER for the proposed system using (32) and that for conventional system are plotted against signal to background noise ratio. It is clear that the proposed system outperform the conventional system by a big margin. Note in this example, the value of M can be set to any integer multiples of three and the same performance characteristics will be obtained. Given the locations of the harmonic tone jammers and that M can be changed flexibly in the system design, the proposed system can always be made to perform better than conventional system under harmonic tone interference.

VII. CONCLUSION

We have described a chip-interleaving DS SS system which can be considered as a generalization of conventional DS SS system. Its performances under ON–OFF wide-band jamming and multiple tone jamming conditions have been analyzed. It is found that under low duty cycle ON–OFF wide-band jamming, the proposed system can perform much better than the conventional system as the SJR PT_b/σ_j^2 increases. It is also shown that when full period m-sequence is used to spread each data bit the proposed system can be made more robust than conventional system under tone jamming by proper selection of the interleaving parameter M. Numerical results show that the proposed system is very effective in combating low duty cycle ON–OFF

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