Improvement on $1/f$ Noise Properties of Nitrided n-MOSFET's by Backsurface Argon Bombardment

P. T. Lai, Jing-Ping Xu, and Y. C. Cheng

***Abstract*— The $1/f$ noise properties of nitrided n-MOSFET's bombarded by low-energy (550 eV) argon-ion beam are investigated. It is found that after bombardment, $1/f$ noise, and its degradation under hot-carrier stress are reduced, and both exhibit a turnaround behavior with bombardment time for a given ion energy and intensity. The physical mechanism involved is probably enhanced interface hardness resulting from bombardment-induced stress relief in the vicinity of the oxide/Si interface. Moreover, from the frequency dependence of the noise, it is revealed that the nitrided devices have a nonuniform trap distribution increasing toward the oxide/Si interface which can be modified by the backsurface bombardment.**

***Index Terms*— Backsurface bombardment, MOSFET's, nitridation, noise, oxide/Si interface.**

I. Introduction

OXYNITRIDES have been considered as a promising gate dielectric for metal–oxide–semiconductor (MOS) devices due to their excellent robustness against hot-carrier stresses and radiation exposure, good blocking against diffusion of dopants and impurities, etc. [1]–[4]. However, the process of nitridation also leads to increases of oxide/Si interface-state density and $1/f$ noise [5], especially for NH_3-nitrided and N_2O-grown oxynitrides, because the former suffers from hydrogen-related electron traps [6], [7], and the latter has an inferior structural transition layer with several defects near the oxide/Si interface, resulting from an initial accelerated growth phase [8]. Recently, the interface qualities of these oxynitrides have been improved by a backsurface Ar^+ bombardment technique [9], [10]. In this letter, it is further shown that $1/f$ noise properties of MOS devices with these two oxynitrides as gate dielectric are also largely improved after appropriate bombardment. This is very important because the capability of integrating low-noise analog circuits and high-speed digital circuits on the same chip is crucial to the production of a wide range of high-performance MOS integrated circuits.

II. Experimental

The n-channel MOSFET's used in this study were fabricated on p-type (100) silicon wafers with a resistivity of 6–8 Ω-cm by self-aligned n^+ polysilicon gate process. The NH_3-nitrded oxide (denoted as NO) was formed by thermally growing oxide at 1000 °C in Ar-diluted O_2 followed by a nitridation at 1000 °C for 60 min in pure NH_3, while N_2O-grown oxide (denoted as N2OG) was prepared at 1050 °C for 120 min in pure N_2O to give the same thickness of 250 Å as determined by capacitance–voltage measurements. Finally, the two kinds of samples were annealed at 950 °C for 25 min in N_2. After completing all conventional processing steps, the samples were put into a vacuum chamber and a low-energy (550 eV) Ar^+ beam with an intensity of 0.5 mA/cm^2 was applied to directly bombard the backsurface of the wafers at room temperature under a vacuum of 3.2 mPa. Four different bombardment durations (0, 10, 20, and 40 min) were chosen, with the corresponding samples denoted as NO0, NO10, NO20, NO40, N2OG0, N2OG10, N2OG20, and N2OG40, respectively. Subsequently, the wafers were annealed in N_2 at 450 °C for 20 min. After all these processing steps, initial noise and interface properties of n-MOSFET's were characterized and then a hot-carrier stress with maximum substrate current ($V_D = 2V_G = 8$ V) was performed to study their $1/f$ noise reliability. Using HP 35665A dynamic signal analyzer, BTA 9603 FET noise analyzer, and HP 4145B semiconductor parameter analyzer, $1/f$ noise was measured in the linear region of device operation ($V_D = 0.2$ V) for a gate overdrive voltage $V_G^* = V_G - V_T = 0.5$ V at 50 Hz (V_T is the threshold voltage). The channel length L and width W of the n-MOSFET's were 2 μm and 20 μm, respectively. All measurements were carried out under light-tight and electrically shielded conditions.

III. Results and Discussions

The $1/f$ noise of MOSFET's is characterized by the noise power of drain current (S_{id}) and can generally be approximated as [11]

$$S_{\mathrm{id}} = \alpha / f^{\gamma}$$

where γ is the noise exponent and α is a constant for a given device structure and bias conditions. Fig. 1 is the measured drain-current noise power spectrum for all bombarded and nonbombarded samples. A common phenomenon can be observed from Fig. 1(a) and (b): bombardment firstly leads to noise decrease and then increase for a sufficiently long bombardment time, corresponding to a turnaround of $1/f$ noise magnitude as bombardment continues. The turnaround time is 20 min for the NO sample and 10 min for the N2OG

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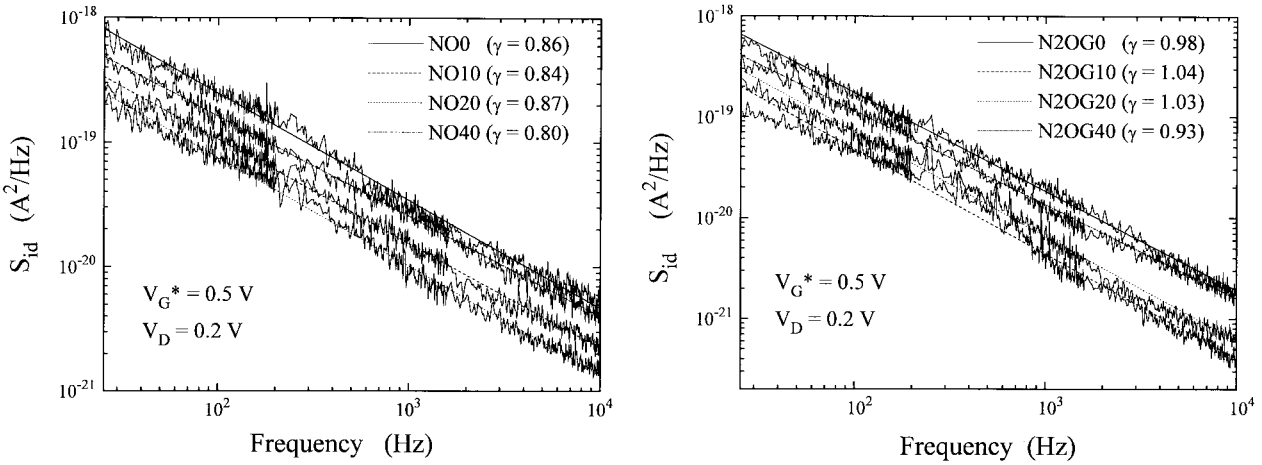

(a) (b)

Fig. 1. Drain-current noise power spectrum of (a) NO samples and (b) N2OG samples with different bombardment times. The error of extracted γ value is ± 0.003.

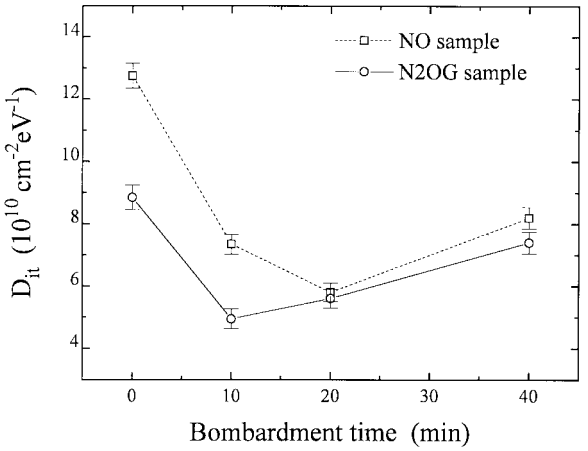

Fig. 2. Interface-state density before and after bombardment for different times (10, 20, and 40 min).

sample. From the number-fluctuation model [12], $1/f$ noise is attributed to fluctuation in the number of channel carriers arising from electronic tunneling transitions between interfacial traps and the inversion layer of MOSFET's. In other words, $S_{\rm id}$ should be proportional to the density of the dielectric traps close to the oxide/Si interface $(D_{\rm it})$ which can be evaluated by the charge-pumping method. As shown in Fig. 2, a similar turnaround phenomenon is also observed in $D_{\rm it}$ of the same transistors used in noise measurement. The physical mechanism involved should be the stress compensation effect, where the ion bombardment at the wafer back induces a stress which can reduce the residual mechanical stress at the oxide/Si interface by up to 37% [13]. The resulting lower interfacial stress means lower $D_{\rm it}$ and thus lower $S_{\rm id}$. Therefore, it can be believed that the residual stress at the interface is smaller in the N2OG sample than in the NO sample, and thus stress overcompensation causing the turnaround occurs earlier in the former than the latter. A possible explanation is that the higher the growth temperature (as for N2OG), the lower the residual stress in the oxide and at the oxide/Si interface [14]. In Fig. 1, the straight lines represent a least-squares fit to the measured data and their slopes give the noise exponent shown in the parenthesis. $\gamma \neq 1$ implies a nonuniform trap distribution along the direction normal to the oxide/Si interface [15], [16]. For a trap distribution that increases toward the interface, there are a large number of high-frequency traps (traps adjacent to the interface) giving rise to $\gamma < 1$. Otherwise, $\gamma > 1$ due to a large number of low-frequency traps (traps farther away from the interface). Therefore, the extracted γ values support that both NH_3 nitridation and N_2O growth produce a nonuniform trap distribution decreasing away from the interface due to hydrogen-related species for the former [6], [7], and an inferior structural transition layer with a lot of defects near the oxide/Si interface for the latter [8]. Also based on $\gamma(\mathrm{NO}) < \gamma(\mathrm{N2OG})$, the former introduces more high-frequency traps than the latter due to the significant effects of the hydrogen species in NH_3. As demonstrated by the N2OG sample, backsurface bombardment seems to preferentially affect high-frequency traps because they are closer to the interface: γ changes from <1 to >1 and then back to <1 as bombardment time increases. More specifically, 10- and 20-min bombardments greatly reduce high-frequency traps so that they become fewer than low-frequency traps and $\gamma > 1$. However, an excessive bombardment of 40 min generates many new high-frequency traps which, once again, outnumber low-frequency traps. For the NO sample, although the effect is not clearly seen, possibly due to a much higher interfacial oxide-trap density as shown in Fig. 2, a 40-min bombardment also gives rise to an obvious increase of high-frequency traps and thus a large reduction of γ.

The effect of electrical stress on the $1/f$ noise of the devices is also examined. Fig. 3 shows a suppressed degradation of $1/f$ noise properties for all bombarded samples after a maximum-substrate-current stress ($V_D = 2\,V_G = 8$ V). As bombardment continues, the increase of $1/f$ noise $(\Delta S_{\rm id})$ decreases to a minimum value for NO20 and N2OG10 samples, and then rebounds to a value comparable with those of nonbombarded samples, again exhibiting a turnaround behav-

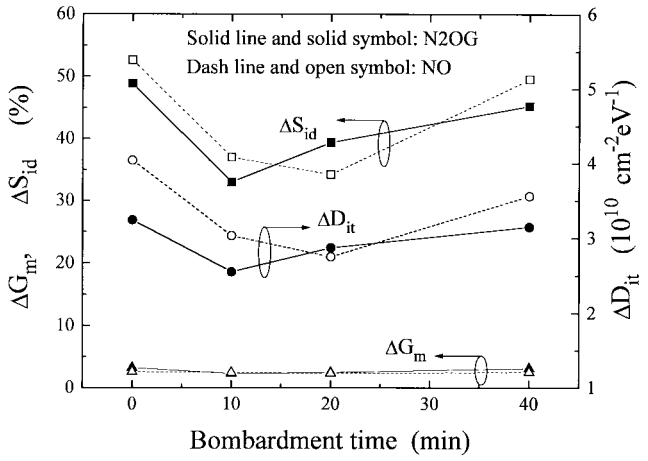

Fig. 3. Increases of $1/f$ noise and interface-state density after a hot-carrier stress at $V_D = 2$ $V_G = 8$ V for 3000 s for all samples.

ior similar to that in Fig. 1. In Fig. 3, interface-state creation $(\Delta D_{\rm it})$ caused by the electrical stress is also plotted, and presents exactly the same trend as $\Delta S_{\rm id}$, indicating that enhanced interface hardness induced by appropriate backsurface bombardment is responsible for the suppressed $\Delta D_{\rm it}$ and hence the improvement of $1/f$ noise properties. Therefore, an optimal bombardment time should be chosen for a given ion energy and intensity to obtain the best interface and thus $1/f$ noise properties. As for degradation of peak linear transconductance (ΔG_m) shown in Fig. 3, although it also exhibits a turnaround similar to those of $\Delta S_{\rm id}$ and $\Delta D_{\rm it}$, much smaller value is observed, indicating that static parameters of MOSFET's are not as sensitive as dynamic parameters, e.g., $1/f$ noise, in assessing the device damage due to electrical stresses.

IV. Summary

Backsurface Ar^+ bombardment can result in better $1/f$ noise properties of nitrided n-MOSFET's which exhibit a turnaround behavior with bombardment time. Moreover, increase of $1/f$ noise under hot-carrier stress is also greatly suppressed for properly-bombarded samples. The involved mechanism is attributed to improved oxide/Si interface quality resulting from stress relief near the interface induced by the bombardment. In addition, $1/f$ noise measurements show that NH_3 nitridation introduces much more interfacial traps than N_2O growth due to hydrogen-related species, and both give a nonuniform trap distribution near the oxide/Si interface which increases toward the interface. However, bombardment can greatly reduce interfacial oxide traps and thus change their distribution even to one decreasing toward the interface. Therefore, proper backsurface bombardment is effective to further increase interface hardness and decrease $1/f$ noise of nitrided MOSFET's. Moreover, since similar results have been obtained for much larger gate-oxide thickness of 5000 Å [13], under suitable bombardment conditions, this technique should be applicable to thicknesses below 100 Å.

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