Correlation Between Hot-Carrier-Induced Interface States and GIDL Current Increase in N-MOSFET's

P. T. Lai, J. P. Xu, W. M. Wong, H. B. Lo, and Y. C. Cheng, *Member, IEEE*

***Abstract*— Correlation between created interface states and GIDL current increase in n-MOSFET's during hot-carrier stress is quantitatively discussed. A trap-assisted two-step tunneling model is used to relate the increased interface-state density $(\Delta D_{\rm it})$ with the shift in GIDL current (ΔI_d). Results show that under appropriate drain-gate biases, the two-step tunneling is so dominant that ΔI_d is insensitive to temperatures up to about 50 °C. With the help of 2-D device simulation, the locations of the drain region with significant two-step tunneling and the energy levels of the traps involved can be found, with both depending on the drain voltage. From these insights on $\Delta D_{\rm it}, \Delta I_d$ and their relation, $\Delta D_{\rm it}$ near the midgap can be estimated, with an error less than 10% as compared to the results of charge-pumping measurement on the same transistors. Devices with nitrided gate oxide, different gate-oxide thicknesses and different channel dimensions are also tested to verify the above correlation.**

I. Introduction

INTERFACE-STATE creation due to hot-carrier stress constitutes a major device-reliability concern and attracts much research interest [1]–[3]. It is generally characterized by charge- pumping (CP) and C–V techniques. However, since its effects on the electrical characteristics of MOSFET's are obvious in terms of subthreshold slope and gate-induced-drain-leakage (GIDL) current, it should also be possible to determine the change in interface-trap density $\Delta D_{\rm it}$ by measuring the shift in these device parameters, which has been described in the literature [4]–[7]. It was suggested by Duvvury *et al.* [4] that the increase in GIDL current was a direct result of flat-band voltage shift due to $\Delta D_{\rm it}$. However, Chen *et al.* [5] reported that in an n^+ gated diode, $\Delta D_{\rm it}$ merely enhances GIDL current via an increase in surface generation velocity. More recently, Hori [6] discussed $\Delta D_{\rm it}$-related GIDL current based on band-to-band (B-B) tunneling process via interface state. The present work attempts to quantitatively study the correlation between $\Delta D_{\rm it}$ and GIDL current increase (ΔI_d) by means of an interface-trap-assisted two-step tunneling model [7], thus obtaining some insights on the physical mechanisms involved.

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II. Experiment

Conventional n-MOSFET's with thermal SiO_2 (OX) grown at 850 °C for 100 and 60 min, respectively, in O_2 and Ar (marked as OX1 and OX2, respectively), or nitrided oxide (N2ON) as gate dielectric were used. N2ON samples were fabricated by nitridizing OX2 samples at 950 °C for 70 min in pure N_2O ambient. The final gate-oxide thickness $T_{\rm ox}$ of the three kinds of samples (measured by C–V) was 210 Å for OX1 samples and N2ON samples, and 145 Å for OX2 samples. The devices were subject to hot-electron stress, $V_G = 0.5\ V_D = 3.5$ V, for 1000–4000 s to create interface traps. GIDL current was measured before and after the stress under three different conditions with the same drain-to-gate bias $V_{\rm DG} = 8$ V ($V_D = 5$ V, $V_G = -3$ V; $V_D = 4$ V, $V_G = -4$ V; and $V_D = 3$ V, $V_G = -5$ V), and source and substrate grounded. The stressings and measurements were performed on MOSFET's with channel length (L)/channel width $(W) = 1/24\ \mu$m and 1.8/10 μm in a nitrogen ambient under light-tight and electrically shielded condition using an HP 4156A precision semiconductor parameter analyzer.

III. Results and Discussion

Fig. 1 shows the measured pre-stress and post-stress GIDL currents for OX1 samples. Solid lines, dash lines and dot lines correspond to the three different conditions for GIDL measurement. Along the arrow direction, stress time increases from 0 s to 4000 s with an increment of 1000 s. X-axis is the time at which GIDL current is measured after the stress is finished. It can be seen that after stressing for 1000 s, GIDL current increases obviously, and for stress time above 1000 s, shift of GIDL current becomes gradually small and then reaches almost a saturation value after stressing for 4000 s. This saturation phenomenon seems to indicate that interface-trap creation is limited by the number of potential trap sites available. The observed increase in post-stress GIDL current is distinctly different from that induced by oxide traps because oxide traps only induce GIDL current transient on a time scale of seconds. So, it should be dependent on the amount of interface traps created during stress since the stress method of $V_G = 0.5\ V_D$ is mostly responsible for interface-state generation [1]. In other words, an additional conduction mechanism involving interface traps [7] should be possible after the hot-electron stress. Under low $V_{\rm DG}$, the energy band is not sufficiently bent with the Fermi level E_F still inside the bandgap, and therefore direct B-B tunneling is weak. However, the thermal excitation of electrons from the valence band into the interface traps, followed by tunneling into the conduction

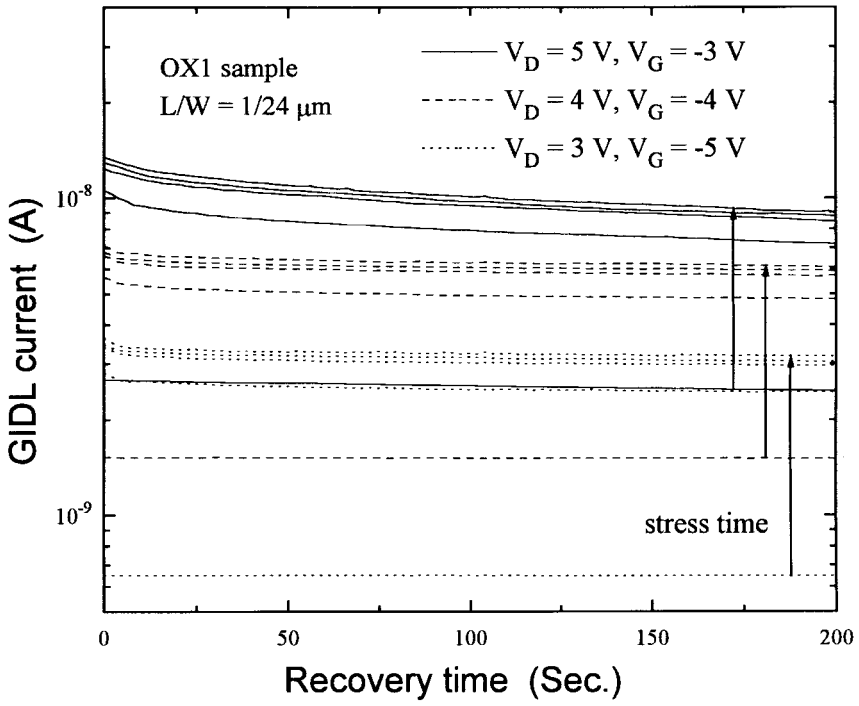


Fig. 1. Measured pre-stress and post-stress GIDL currents for OX1 sample. Stress time is 1000, 2000, 3000, and 4000 s, respectively.

band, i.e., a trap-assisted one-step tunneling [6], is highly probable. As $V_{\rm DG}$ is increased to such a large value that E_F is much below the interface-trap levels, a trap-assisted two-step tunneling is also appreciable due to enhanced tunneling rate, with hole tunneling from the interface traps to the valence band (step 1) and then electron tunneling from the interface traps to the conduction band (step 2) [7], as illustrated in Fig. 2. This deduction is further supported by the measured results for N2ON sample before and after a stressing for 3000 s, as presented in Fig. 3. It can be seen that shift in post-stress GIDL current is significantly smaller as compared to OX1 sample (only 167 pA for $V_D = 5$ V, 105 pA for $V_D = 4$ V and 40 pA for $V_D = 3$ V). This smaller shift is expected because creation of interface states during stress is effectively suppressed due to nitrogen incorporation at the Si/SiO_2 interface of nitrided devices [8]. Thus it can be concluded that the increase of GIDL current after stress indeed reflects a generation of interface states and $\Delta D_{\rm it}$ could be linked to the measured increase in post-stress GIDL current.

Under the two-step tunneling condition, the increased GIDL current ΔI_d can be derived as follows [7]:

$$\Delta I_d = A \exp(-B_{\rm it}/F) \tag{1}$$

$$B_{\rm it} = \frac{4}{\hbar}(2m_n)^{1/2}\frac{(E_c - E_t)^{3/2}}{3q} \tag{2}$$

$$E_t = \frac{E_V + (F_1/F)^{2/3}E_C}{1 + (F_1/F)^{2/3}} \tag{3}$$

where A is weakly dependent on electric field and proportional to the generated interface-state density near midgap $\Delta D_{\rm it}$, F_1 is the lateral field, F is the total field in deep-depletion region, and E_t is the energy level of the interface traps, which are most effective in the two-step tunneling process. Other variables

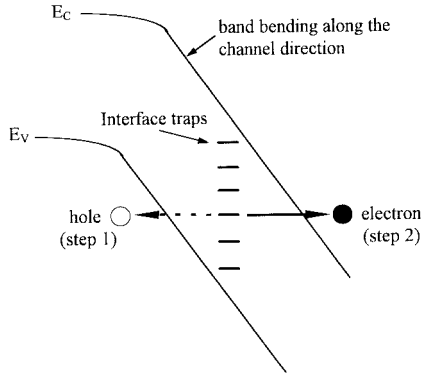


Fig. 2. Schematic diagram of the trap-assisted two-step tunneling, with hole tunneling occurred only in the direction parallel to the channel while electron tunneling occurred in both directions parallel and vertical (band bending is not plotted here) to the channel.

have their usual definitions. To check the validity of (1), the temperature dependence of ΔI_d was measured and the results are shown in Fig. 4. It can be seen that measured ΔI_d at $V_{\rm DG} = 8$ V hardly changes with temperature (T) below 50 °C, but increases at higher temperatures due to thermal generation which is ignored in (1) [7]. From (2) and (3), changes of $(E_t - E_V)$ and $B_{\rm it}$ with F_1/F can be obtained, as shown in Fig. 5. It can be seen that as lateral field F_1 gets stronger, E_t changes from E_V to E_i (intrinsic Fermi level) and the corresponding $B_{\rm it}$ decreases from 36 to 12.8 MV/cm. In fact, $B_{\rm it}$ in (1) reflects a potential barrier height in tunneling and has a minimum value for midgap-trap-assisted two-step tunneling. In [7], the parameter A was treated as a fitting parameter, and as a result, $\Delta D_{\rm it}$ was not explicitly involved in (1). In reality, A can be expressed as

$$A = \Delta D_{\rm it} q W L_e \Delta E_t / (2\tau_{0c}) \tag{4}$$

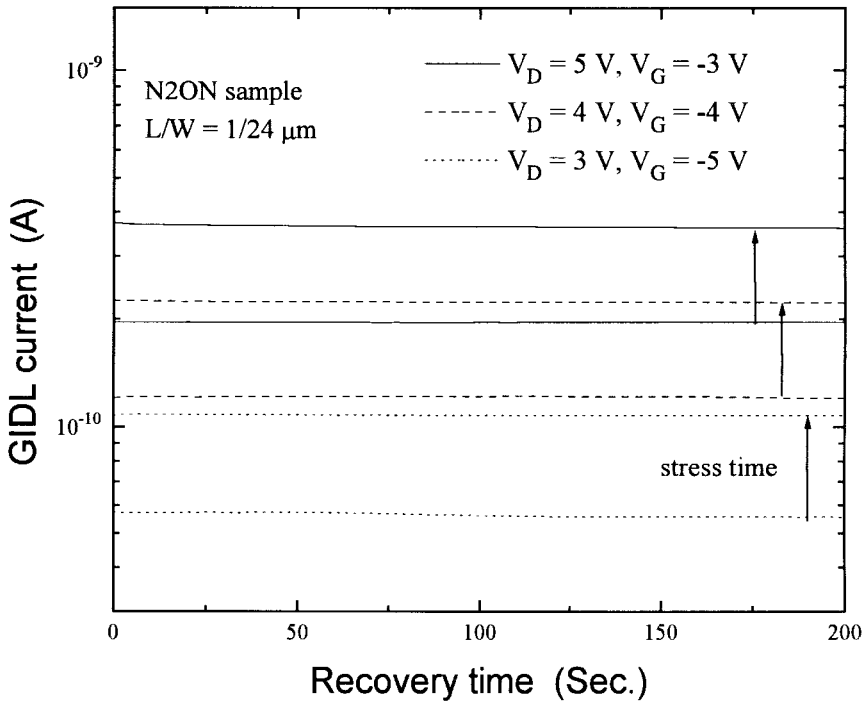


Fig. 3. Measured pre-stress and post-stress GIDL currents for N2ON sample. Stress condition is $V_G = 0.5V_D = 3.5$ V for 3000 s.

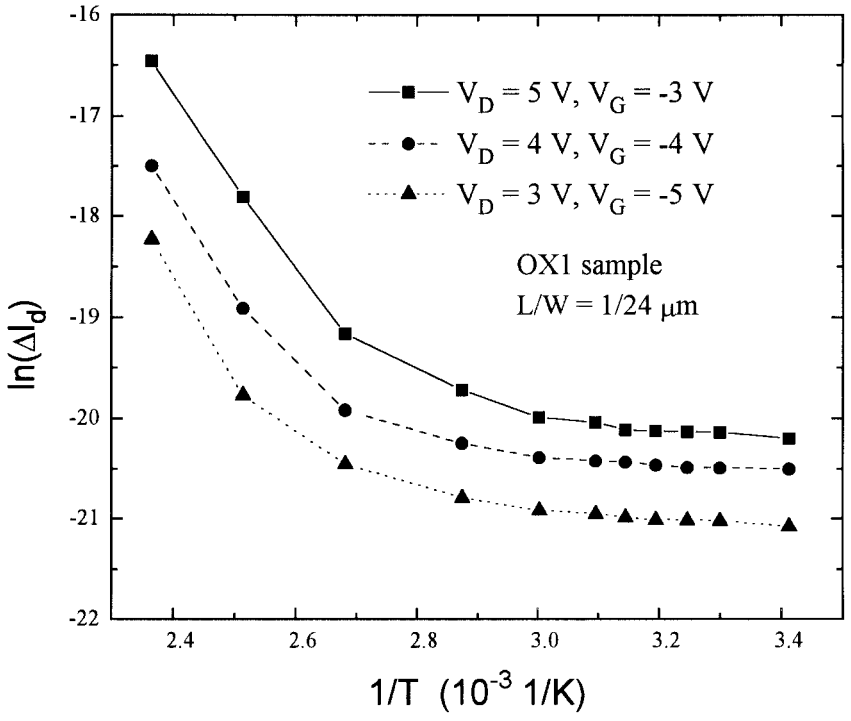


Fig. 4. Temperature dependence of post-stress GIDL increase for OX1 sample. Stress condition is $V_G = 0.5V_D = 3.5$ V for 1000 s.

where τ_{0c} is effective transit time in the conduction band, L_e is effective spatial width of $\Delta D_{\rm it}$ distribution which contributes to GIDL current through the two-step tunneling conduction mechanism, ΔE_t is effective energy range covered in GIDL current measurement. In order to deduce $\Delta D_{\rm it}$, it is necessary to obtain the field distribution near drain junction. Only after F and F_1 are determined by 2-D device simulation, the value of $B_{\rm it}$ in (1) can be calculated by (3) and (2), and then $\Delta D_{\rm it}$ can be found as below.

For clarity, the measured results in Fig. 1 are taken as an example to illustrate the detail of obtaining $\Delta D_{\rm it}$. For the three GIDL measurement conditions mentioned previously, the field distributions along the interface near the drain simulated by MINIMOS4 are depicted in Fig. 6. The gate and drain edges

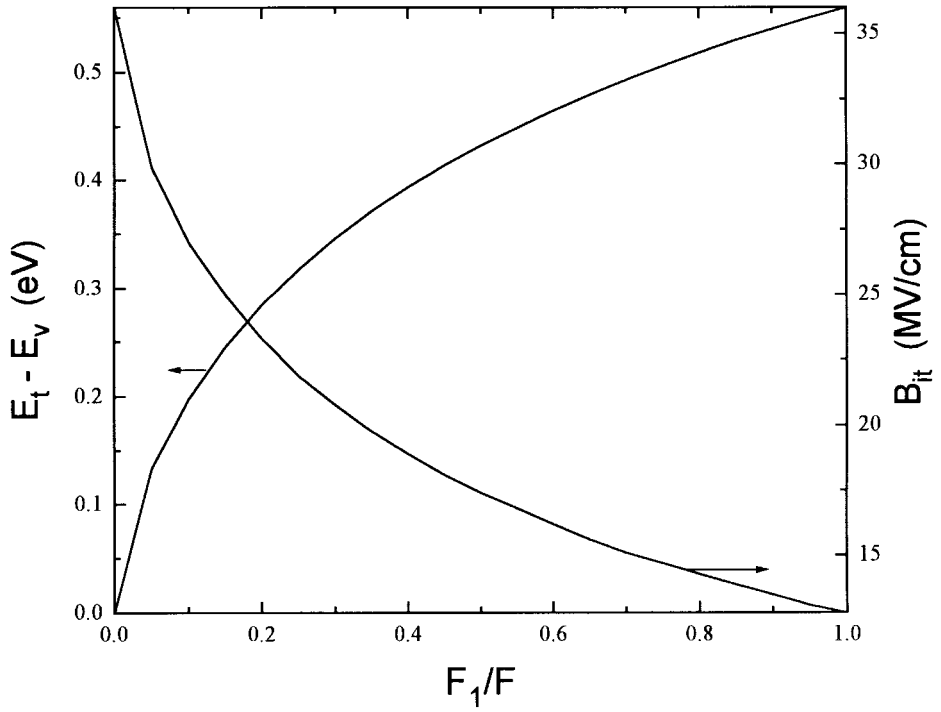


Fig. 5. Changes of trap energy E_t and $B_{\rm it}$ with the ratio of lateral and total fields F_1/F.

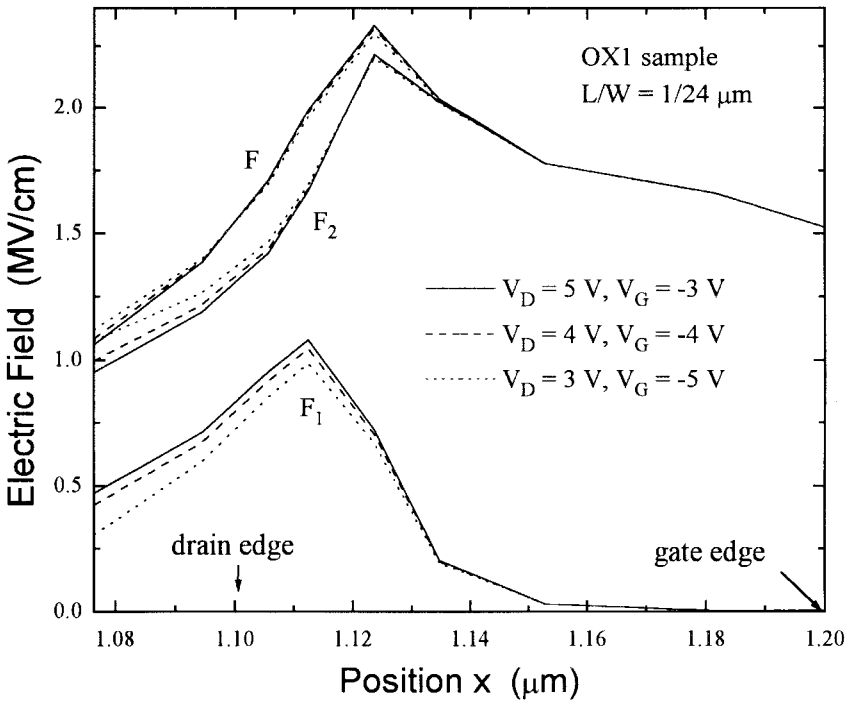
are located at position $x = 1.2$ and 1.1 μm for OX1 sample; $x = 2.0$ and 1.9 μm for OX2 sample, respectively, which define the two ends of the gate-drain overlap region. The width of this region was measured by the device-parameter extraction program BSIMPro® for Windows and was equal to 0.10 μm. From Fig. 6, two phenomena can be observed: the vertical field F_2 is higher than the lateral field F_1, and their peaks lie within the gate-drain overlap region. Since F_1 and F are functions of position, (1) should be rewriten as

$$\Delta I_d = A\frac{1}{\Delta X}\int \exp(-B_{\rm it}/F)\,dx \approx A\frac{1}{\Delta X}\sum_j \exp(-B_{it,j}/F_j)\,\Delta x_j. \quad (5)$$

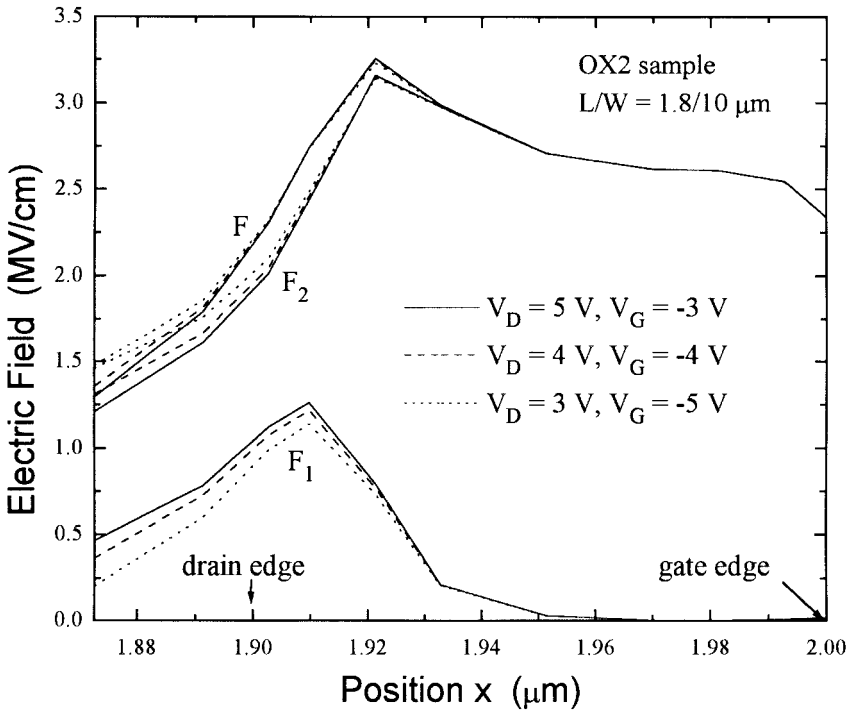
Substituting (4) and re-arranging gives

$$\Delta D_{\rm it} = \frac{2\tau_{0c}\Delta X}{qWL_e\Delta E_t\sum_j \exp(-B_{it,j}/F_j)\Delta x_j}\cdot \Delta I_d \quad (6)$$

where ΔX is effective action range of electric field which can result in significant two-step tunneling conduction, and can be approximated to be the same as L_e. Simulations showed that ΔX almost corresponds to depletion region width near drain junction which depends on drain voltage, in which depletion region edges in channel region and gate-drain overlap region can be determined by defining a value of 1×10^{14} cm^{-3} for majority concentration [9]. In addition, from the assumption that $\Delta D_{\rm it}$ is a uniform distribution only near midgap E_i [7], (5,) and (6) should not include the terms with large $B_{it,j}$ values which correspond to E_t levels far below Ei as shown in Fig. 5. Calculations showed that when $B_{\rm it}$ is above 29 MV/cm, electrons tunneling can be almost considered as B-B tunneling because E_t is very close to E_V in the cases. Combining considerations on ΔX and $B_{\rm it}$ above, after performing field simulation, $\Delta D_{\rm it}$ for different stress times can be calculated using (6) for different V_D under same $V_{\rm DG}$ from the measured ΔI_d, and the results are shown in Fig. 7(a) (in the calculation, $\tau_{0C} = 0.1$ ps [10]). For $V_D = 3$, 4, and 5 V measurement conditions, the values of ΔX and ΔE_t are 584 Å, 0.15 eV; 1347 Å, 0.21 eV; and 2111 Å, 0.25 eV, respectively, with ΔE_t below E_i. For comparison, the corresponding results measured by the commonly used CP method on the same transistor are also presented in Fig. 7(a). As can be seen, the results estimated by GIDL method under all measurement conditions are in good agreement with the results of CP measurement, and maximum error is less than 6%. The same procedures are also carried out for OX2 sample and results are shown in Fig. 7(b). Two different transistors are used for the two GIDL measurement conditions due to significant oxide-charge trapping effect during GIDL current measurement on the samples, which produces a larger error close to 10%. It is worth pointing out that in Fig. 7(b), the curves for $V_D = 3$ V are not included since both measured GIDL current ($<$20 pA) and ΔI_d are too small to be measured accurately, which results in a large error in the calculated $\Delta D_{\rm it}$ (about an order of magnitude lower than CP measurement). The fact is also supported by measured results of N2ON samples (CP measured value is 9.5×10^8 cm^{-2} eV^{-1} and estimated $\Delta D_{\rm it}$ is 1.0×10^9 cm^{-2} eV^{-1} for $V_D = 5$ V, 8.7×10^9 cm^{-2} eV^{-1} for $V_D = 4$ V, and 6.0×10^8 cm^{-2} eV^{-1} for $V_D = 3$ V (error: 37%). Therefore, to have a properly large measurement current, a suitable drain voltage should be chosen. It has been found in our measurements that GIDL current between hundreds of pA and tens of nA is appropriate, whose origin of course must still be examined, i.e., B-B tunneling dominant or



(a)



(b)

Fig. 6. Simulated electric field distributions along oxide/Si interface near drain junction for three measurement conditions using MINIMOS4. $V_S = V_B = 0$ V. (a) OX1 sample, and (b) OX2 sample.

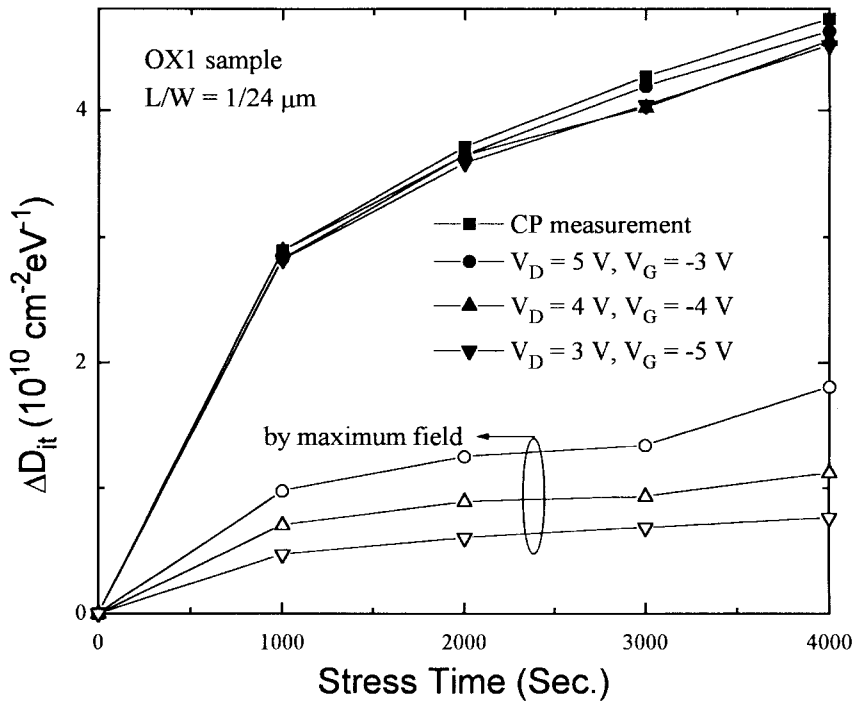
two-step tunneling dominant. This can be distinguished simply by plotting $\ln(I_d/F_s)$ versus $1/F_s$ for GIDL current resulted from band-to-band tunneling [11]

$$I_d = \frac{C}{B} F_{\text{tot}} \exp\left(-\frac{B}{F_{\text{tot}}}\right) \tag{7}$$

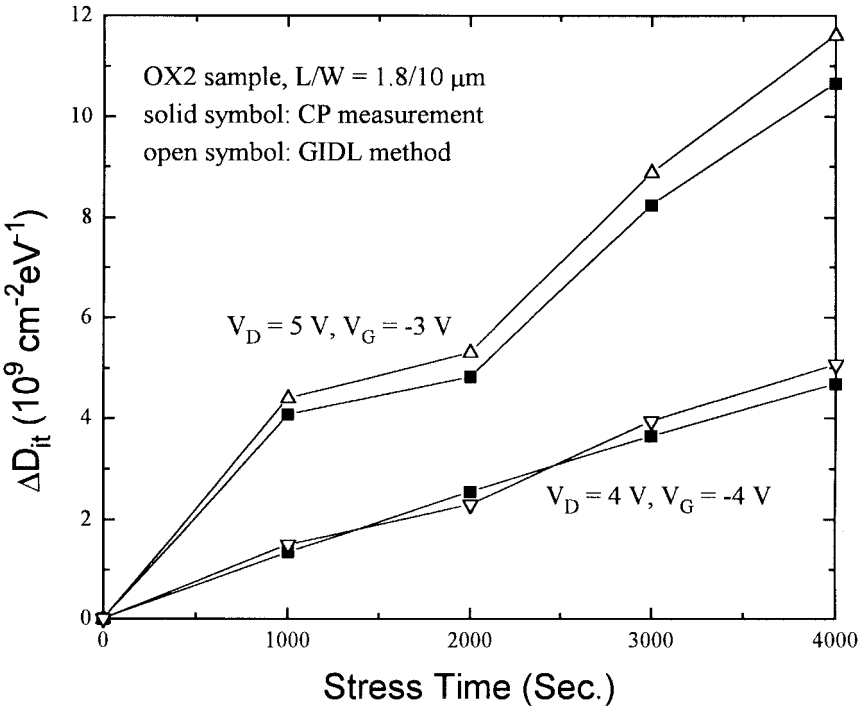
where B and C are constants, F_{tot} is the average total electric field which can be approximated by the surface electric field F_s at the point of maximum band-to-band tunneling [12]:

$$F_s = -\frac{3T_{\text{ox}}qN}{\varepsilon_s} + \sqrt{\left(\frac{3T_{\text{ox}}qN}{\varepsilon_s}\right)^2 + \frac{2qN(|V_{\text{DG}}| - V_{fb})}{\varepsilon_s}} \tag{8}$$

where the drain doping concentration N was simulated to be



(a)



(b)

Fig. 7. $\Delta D_{\rm it}$ of OX1 (a) and OX2 (b) samples obtained by GIDL current method and CP technique for different stress time. For OX2 sample, measurements for two different V_D's were performed on two different transistors because of oxide-charge trapping during GIDL measurement.

1.7×10^{19} cm^{-3}, which was verified by spreading-resistance measurements, while flatband voltage V_{fb} was measured to be -0.866 V for OX1 sample and -0.921 V for OX2 sample. If the $\ln(I_d/F_s)$ versus $1/F_s$ curve deviates from a straight line at the chosen $V_{\rm DG}$, it can be believed that trap-assisted tunneling coexists with B-B tunneling. The two trap-assisted mechanisms can be further distinguished by considering the temperature dependence of ΔI_d shown in Fig. 4. Obviously, in Fig. 8, our measurement condition of $V_{\rm DG} = 8$ V for the GIDL current at room temperature should correspond to the two-step tunneling mechanism because ΔI_d is basically constant around room temperature.

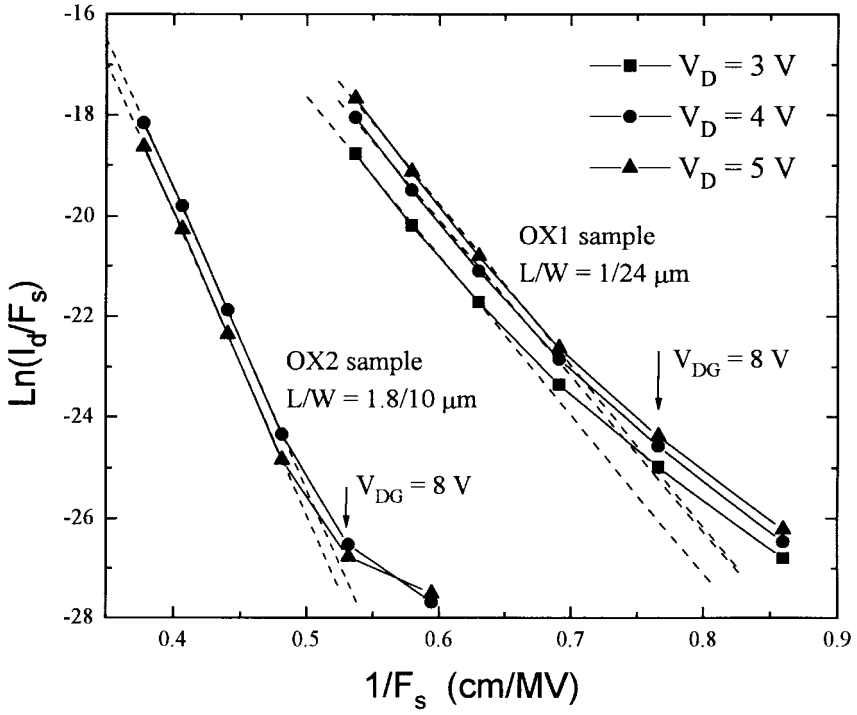


Fig. 8. Plot of $\ln(I_d/F_s)$ versus $1/F_s$ for post-stress OX devices. The deviation from linearity at $V_{\rm GD} = 8$ V shows the presence of the two-step tunneling, considering the temperature insensitivity of ΔI_d shown in Fig. 4.

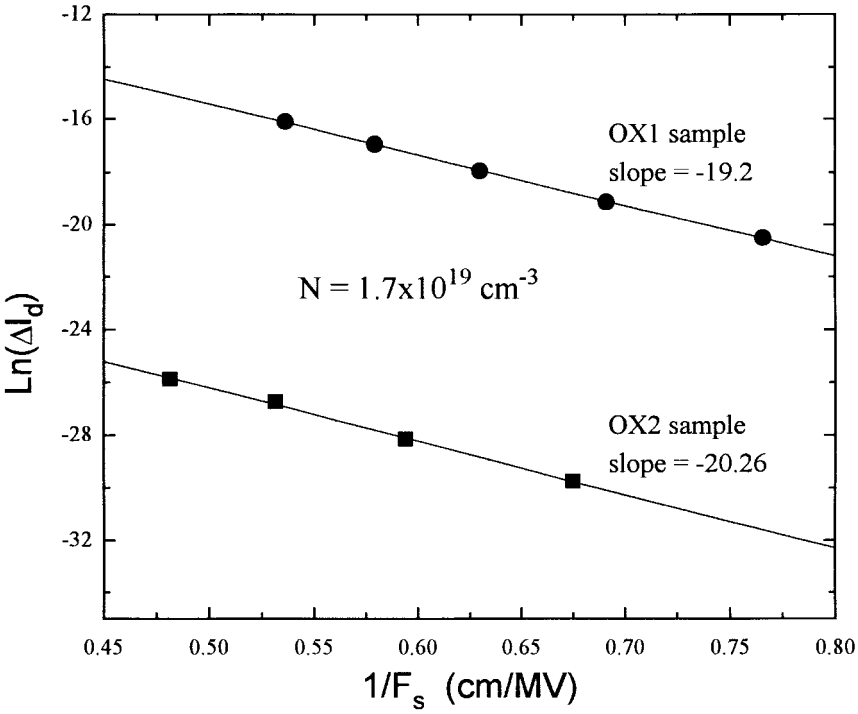


Fig. 9. Plot of $\ln(\Delta I_d)$ versus $1/F_s$ corresponding to the two-step tunneling for OX1 and OX2 samples. From the slope of the linear fit, the values of $B_{\rm it}$, 19.20 MV/cm for OX1 sample and 20.26 MV/cm for OX2 sample, are obtained.

It should be emphasized that if (1) is adopted with F taking the maximum value of the field distribution, the estimated $\Delta D_{\rm it}$ is much smaller than that by CP method (error $\sim$68% for $V_D = 5$ V, 78% for $V_D = 4$ V, and 84% for $V_D = 3$ V) as shown in Fig. 7(a), while one using the average field in (8) instead is several orders larger than that by CP method [not shown in Fig. 7(a)]. This indicates that the whole field distribution near the drain junction is needed in order to accurately link the GIDL increase with $\Delta D_{\rm it}$. Finally, the average value of $B_{\rm it}$ is directly found by plotting $\ln(\Delta I_d)$ versus $1/F_s$. As shown in Fig. 9 slope $= -19.20$ for OX1 sample, -20.26 for OX2 sample, i.e., $B_{\rm it}$ of OX1 and OX2 samples is 19.20 and 20.26 MV/cm, respectively, which are in good agreement with the average values of 19.45 MV/cm for

OX1 sample and 20.22 MV/cm for OX2 sample obtained by simulation of the field distribution, suggesting good accuracy of the field simulation.

IV. Summary

In summary, the dependence of post-stress GIDL current increase ΔI_d on the creation of interface states during hot-carrier stress was investigated by means of a two-step tunneling model. The increase can reflect the change of interface-state density $\Delta D_{\rm it}$ under proper drain-gate biases. The two-step tunneling results in a ΔI_d insensitive to temperatures up to about 50 °C. For a fixed $V_{\rm DG}$ of 8 V in our devices, the energy level of the traps which is effective for the two-step tunneling is within a range of 0.15–0.25 eV below the midgap and the width of the tunneling region is about 600–2000 Å near the drain junction for V_D of 3–5 V. From the developed relation between $\Delta D_{\rm it}$ and $\Delta I_d, \Delta D_{\rm it}$ can be estimated from the measured ΔI_d and 2-D device simulation, and the maximum error is smaller than 10% relative to the results of charge-pumping measurement. Further support is obtained by using devices with nitrided gate oxide (which show much suppressed $\Delta D_{\rm it}$), different gate-oxide thicknesses and different channel dimensions. Therefore, this work is conducive to understanding some properties of $\Delta D_{\rm it}$ and its relation with ΔI_d.

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