

Fabrication and Characteristics of a GaInP/GaAs Heterojunction Bipolar Transistor Using a Selective Buried Sub-Collector

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Abstract—A C-doped GaInP/GaAs heterojunction bipolar transistor (HBT) with a selective buried sub-collector has been fabricated by two growth steps. The active HBT region was made on the selective buried sub-collector layer with minimum overlap of the extrinsic base and the sub-collector region resulting in substantial reduction of the base-collector capacitance. The experiment shows that the base-collector capacitance is reduced to about half of that of a conventional HBT while the base resistance remains unchanged resulting in a 40–50% increase in the maximum oscillation frequency. Both DC and RF characteristics are investigated and compared with a conventional HBT. A current gain of 40, cutoff frequency of 50 GHz and maximum oscillation frequency of 140 GHz were obtained for the GaInP/GaAs HBT. It is demonstrated that the selective buried sub-collector provides an effective means for enhancing RF performance of an HBT.

I. INTRODUCTION

HETEROJUNCTION bipolar transistors (HBT's) are attractive for digital, analog, and microwave applications due to their excellent switching speed, high current driving capability and low $1/f$ noise [1], [2]. However, the speed and microwave performance are usually limited by parasitic parameters. For microwave applications, the base resistance and base-collector capacitance of HBT's are important factors limiting the RF performance and they should be made as low as possible. The base resistance can be reduced by increasing the base doping density which is limited by the highest allowable impurity concentration [3]. The extrinsic capacitance under the base ohmic contact region usually constitutes the bulk of the total base-collector capacitance (C_{BC}). Reduction of the extrinsic base-collector capacitance has therefore received a great deal of attention in enhancing RF performance. The conventional method of reducing the base-collector capacitance employs either H^+ or O^+ implantation into the extrinsic collector region [4], [5]. However, the contribution of the capacitance between the extrinsic base and the sub-collector is still noticeable. Deep H^+ implantation to sub-collector layer gives rise to a significant reduction in C_{BC} [6], but it also increases the base resistance. An InAlAs/InGaAs HBT with a buried sub-collector grown by

selective epitaxy was reported showing a significant reduction of the base-collector capacitance [7]. However, planarization of the selective growth in a groove is especially difficult.

This paper reports the fabrication and characteristics of a C-doped GaInP/GaAs HBT with reduced base-collector capacitance using a selective buried sub-collector (SBSC) layer. The HBT was grown on the selective buried sub-collector mesa, and the base contact region was formed on the lightly doped collector layer above the SI GaAs substrate. The collector layer under the base contact region is depleted so that the extrinsic base-collector capacitance is substantially reduced and the maximum oscillation frequency is significantly increased. Comparison of DC and RF performance between HBT's with without SBSC will also be presented.

II. DEVICE STRUCTURE AND FABRICATION

The HBT structure was grown by MOCVD. The growth conditions were the same as those reported earlier [8]. The n-type and p-type dopants were Si and C, respectively. A 4000 Å sub-collector GaAs layer ($n = 4 \times 10^{18} \text{ cm}^{-3}$) was first grown on the SI GaAs substrate. The sub-collector mesa was then defined and formed by photolithography and chemical etching. By using sulphuric acid based etchant [9], the sub-collector mesa has the shape of a trapezoid. The sample was cleaned with ultrasonic bath in acetone and methanol followed by rinses in HCl:H₂O solution (1:20) and DI water before the second growth. No special cleaning and in situ deoxidization was performed. The HBT structure was then regrown in normal growth conditions. The regrown HBT structure consists of a 5000 Å GaAs collector layer ($n = 3 \times 10^{16} \text{ cm}^{-3}$), a 1000 Å GaAs base layer ($p = 6 \times 10^{19} \text{ cm}^{-3}$), a 500 Å GaInP emitter layer ($n = 3 \times 10^{17} \text{ cm}^{-3}$), a 1500 Å n-GaAs emitter cap layer ($n = 4 \times 10^{18} \text{ cm}^{-3}$) and a 600 Å graded $n\text{-In}_x\text{Ga}_{1-x}\text{As}$ (x from 0 to 0.5) contact layer ($n = 5 \times 10^{18} \text{ cm}^{-3}$). A conventional GaInP/GaAs HBT was also grown and fabricated as a control sample. The base sheet resistance of 200 Ω/square was measured in both structures.

Devices were fabricated using the mesa structure and self-aligned techniques as described in [10]. Fig. 1 shows the schematic cross section and layout of the HBT with SBSC. The key difference of making the HBT with SBSC from the fabrication of a conventional HBT was that the active HBT region was made on the selective buried sub-collector region and most of the base contact region is formed outside. Due

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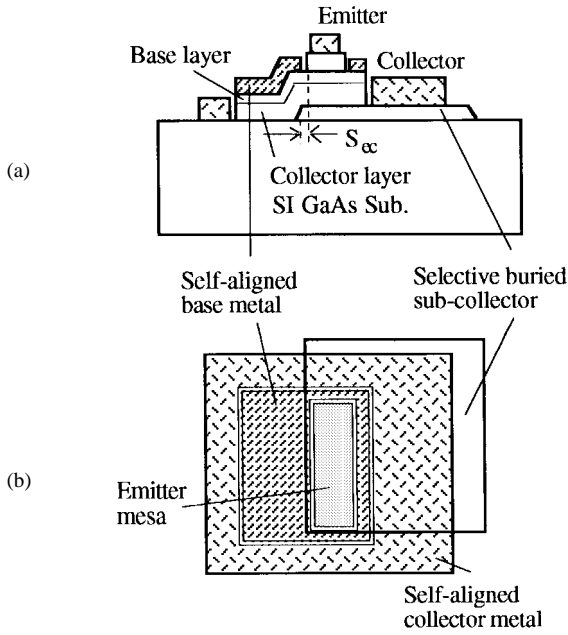
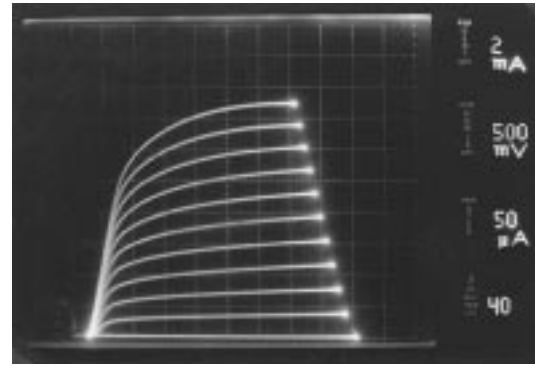


Fig. 1. (a) Cross section of the HBT with selective buried sub-collector; (b) schematic layout of the HBT. HBT's with S_{cc} of 0 and $1.0 \mu\text{m}$ are designated HBT-A and HBT-B. A conventional HBT is designated HBT-C.

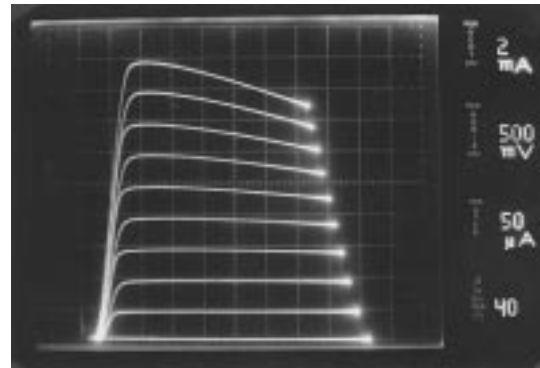
to the lateral growth at the edge of the sub-collector mesa, the emitter mesa was aligned within the mesa edge. The base contact metal covers the slope of the mesa and extend onto the mesa, which eliminates the possible high base resistance due to the slope of the mesa. We have fabricated two samples with a different gap (S_{cc}) between the emitter mesa edge and the sub-collector mesa edge as indicated in Fig. 1. The HBT's with SBSC having S_{cc} of 0 and $1.0 \mu\text{m}$ are designated HBT-A and HBT-B, respectively. The conventional HBT is designated HBT-C. In order to minimize the base resistance, the base contact is made surrounding the emitter mesa, but the overlap of the base contact and the sub-collector region is only along the half periphery of the emitter mesa with the width of $1 \mu\text{m}$. Both the HBT with SBSC and the conventional HBT were fabricated using the same set of mask with an emitter area of $3.5 \times 11.5 \mu\text{m}^2$ and a base mesa size of $11 \times 16 \mu\text{m}^2$. The effective collector area is $5 \times 14 \mu\text{m}^2$ and $6 \times 14 \mu\text{m}^2$ for HBT-A and HBT-B, respectively.

III. RESULTS AND DISCUSSION

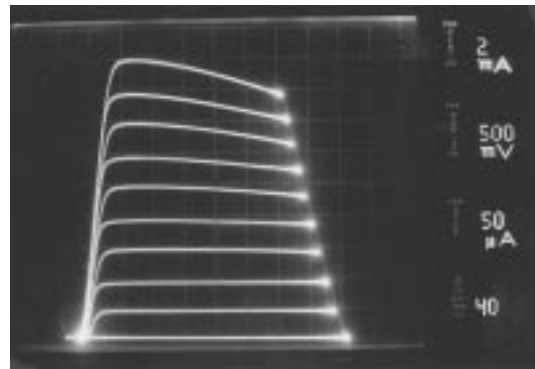
The device's DC characteristics were measured with a curve tracer and an HP4145B semiconductor parameter analyzer. Microwave measurements were made with an HP8510B network analyzer and cascade microwave probes in the frequency range from 100 MHz to 20 GHz. The cutoff frequency (f_T) was extrapolated from the current gain ($|h_{21}|$) by using a -20 dB/decade slope, and the maximum oscillation frequencies ($f_{\text{max}G}$ and $f_{\text{max}U}$) were obtained from maximum stable gain/maximum available gain (MSG/MAG) and unilateral gain (U), respectively. The base-collector capacitance was extracted using the method published by Pehlke [11].



(a)



(b)



(c)

Fig. 2. $I-V$ curves for (a) HBT-A, (b) HBT-B and (c) HBT-C.

A. DC Performance

Fig. 2 shows the common-emitter ($I-V$) curves for HBT-A, HBT-B, and HBT-C. HBT-A has a differential current gain (h_{fe}) of 35 and h_{fe} for both HBT-B and HBT-C is 40. The collector-emitter breakdown voltage (BV_{ceo}) is 9–10 V for all three devices. The $I-V$ curve for HBT-A exhibits a rounded section with gain suppression at low collector-emitter bias (V_{ce}), but it returns to normal at higher V_{ce} . From Fig. 2(b) and (c), the $I-V$ curves for HBT-B and HBT-C are essentially identical. This indicates that the regrown materials are of high quality and the regrown interface between the sub-collector and the collector does not degrade the device performance.

The typical Gummel plots of HBT-A and HBT-B are shown in Fig. 3. The collector and base current ideality factors are 1.19 and 1.65, respectively. Fig. 4 shows the DC current gain

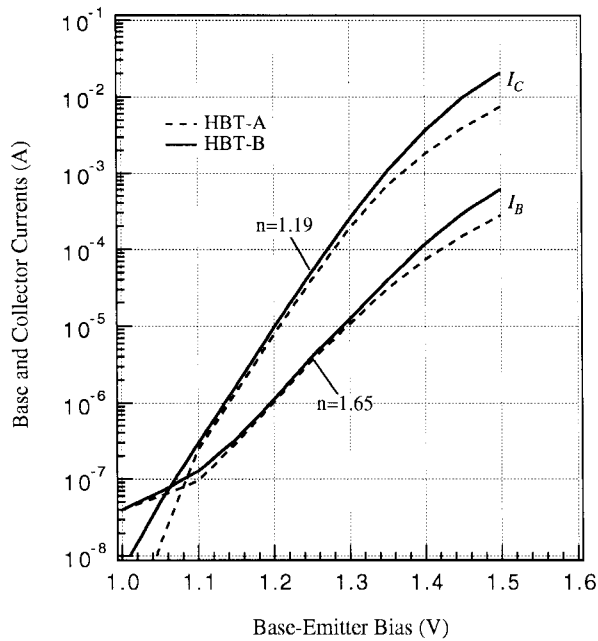


Fig. 3. Typical Gummel plots for HBT-A and HBT-B.

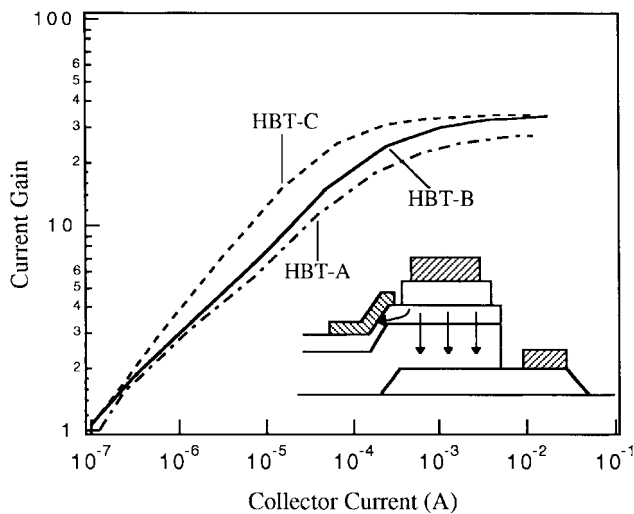


Fig. 4. Current gain versus collector current for HBT-A, HBT-B and HBT-C with an insert of the cross section of HBT-A.

versus the collector current for HBT-A, HBT-B and HBT-C. The current gain of HBT-C is the highest. HBT-B shows similar current gain as that of HBT-C at a high current level. Since there is no passivation ledge for our self-aligned devices, the lower gain of HBT-A and HBT-B at the low current regime is likely caused by the higher surface recombination current. The current gain for HBT-A is similar to that of HBT-B at low current but decreases at high current regime.

In Figs. 2(a) and 4, HBT-A shows not only abnormal $I-V$ curve (gain suppression) at low bias, but also lower current gain than that of HBT-B at a high current region. This gain suppression is possibly due to electrons spill over the edge of the sub-collector. A schematic picture is shown in the insert of Fig. 4 to illustrate the gain reduction. If the edge of the emitter mesa is close to the mesa, some electrons near the mesa edge

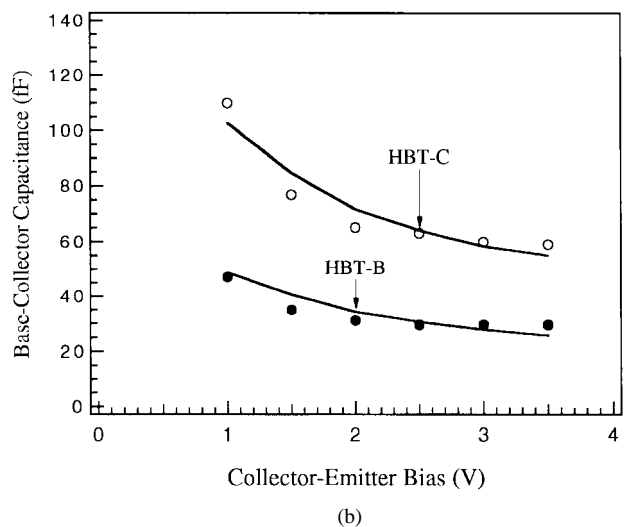
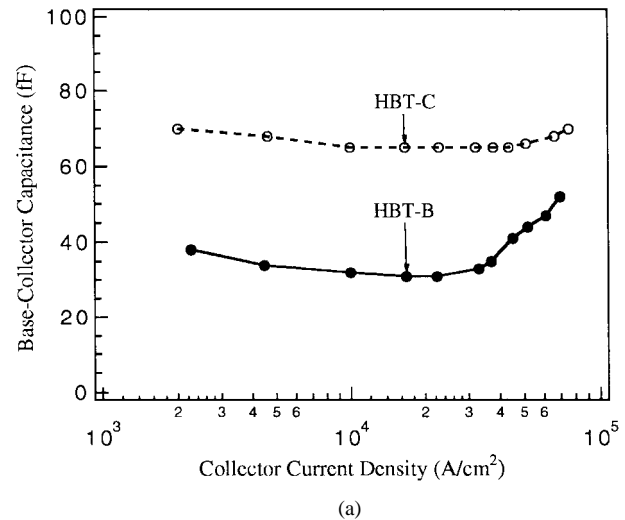


Fig. 5. (a) Extracted base-collector capacitance versus collector current density at V_{ce} of 2.5 V; (b) extracted (circles) and calculated (solid line) base-collector capacitances versus collector-emitter bias at J_c of 2.2×10^4 A/cm² for HBT-B and HBT-C.

injected into the base is more likely to go along the slope of the base layer into the base contact causing the increase of the base current at a high current level. If the emitter edge is far way ($1.0 \mu\text{m}$ for HBT-B) from the slope of the base layer, the electron injected into the base will be collected just like a normal device. Therefore, the emitter mesa should be properly aligned to the sub-collector mesa to eliminate abnormal characteristics and gain suppression. Very good DC characteristics of an HBT with SBSC can be obtained.

B. Base-Collector Capacitance and Small-Signal Parameters

Fig. 5 shows the extracted C_{BC} versus collector current density (at $V_{ce} = 2.5$ V) and collector-emitter bias at J_c of 2.2×10^4 A/cm² for HBT-B and HBT-C. The depletion capacitances are estimated using the effective collector area for HBT-B and base mesa area for HBT-C. The calculated values of C_{BC} for HBT-B and HBT-C are also shown in Fig. 5(b). There is good agreement between the extracted and calculated C_{BC} . Due to the fact that the effective base-collector area

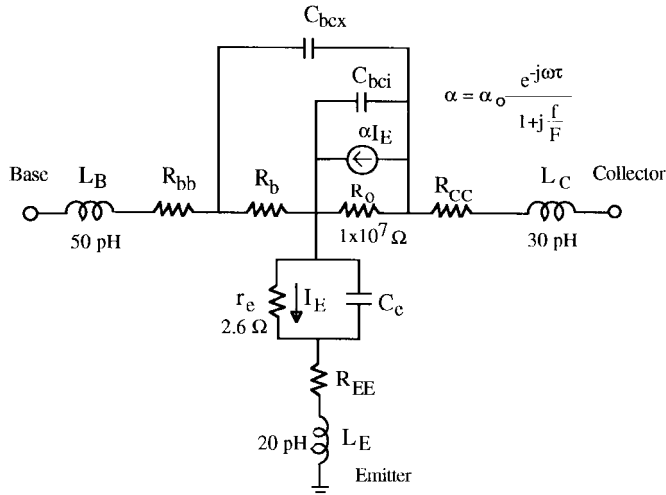
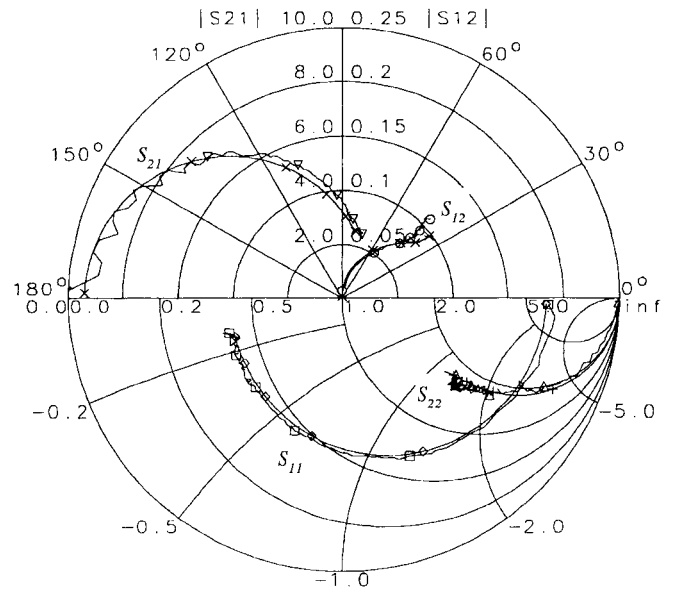


Fig. 6. Small-signal equivalent circuit for HBT's at V_{ce} of 2.5 V and J_c of 2.2×10^4 A/cm².

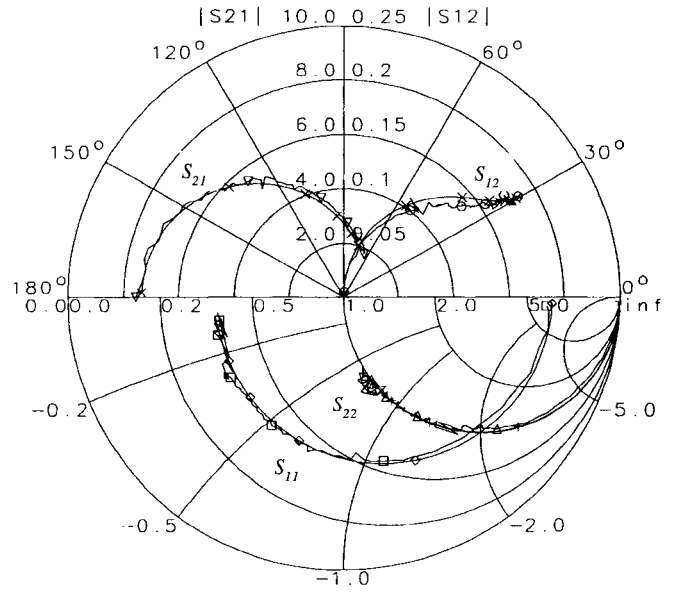
of HBT-B is about half of that of HBT-C, C_{BC} for HBT-B is reduced to about half of that of HBT-C even at low V_{ce} . This indicates that the capacitance under the base contact region is making negligible contributions to the total C_{BC} . From simple calculations using the depletion approximation, the collector depletion thickness is 2370 Å at V_{cb} of 0 V. We use a built-in potential of 0.64 eV at the interface between the semi-insulating GaAs substrate and n-GaAs collector, since the Fermi level of the semi-insulating GaAs substrate is at mid-gap [12], [13] and the Fermi level of the n-GaAs collector is at 0.06 eV below the conduction band. Thus the band bending of the interface creates a depletion layer of 1600 Å in the collector and most of the collector layer on the SI GaAs substrate is depleted at zero base-collector bias.

In order to check how much the extrinsic base-collector capacitance is reduced, a small-signal equivalent circuit was used to model the HBT's. Fig. 6 shows the small-signal equivalent circuit. The values of the circuit elements were optimized using HP-EEsof [14] to fit the measured S -parameters for all three devices at V_{ce} of 2.5 V and J_c of 2.2×10^4 A/cm². To minimize the fitting parameters, the parasitic inductors extracted from the method of [11] and the emitter resistance (r_e) calculated from kT/qI_c were fixed during the optimization. Fig. 7 shows the measured and modeled S -parameters of HBT-B and HBT-C at V_{ce} of 2.5 V and I_c of 10 mA. It is evident that S_{22} for HBT-B is less capacitive than that of HBT-C due to the reduction of the extrinsic base-collector capacitance (C_{bcx}). Since C_{bcx} is the feedback capacitance, the smaller C_{bcx} gives rise to a higher gain. As one can see from Fig. 7(a) and (b), the higher S_{21} and smaller S_{12} of HBT-B reflects the smaller C_{bcx} . As a result, the HBT with SBSC has a high gain and becomes nearly unilateral. The optimized circuit parameters are shown in Table I for three devices. It is shown that the extrinsic base-collector capacitances of the HBT with SBSC are significantly reduced compared to that of HBT-C. We are not sure why C_{bci} 's are different for HBT's with SBSC and HBT-C. However, the value of C_{BC} extracted using the method of reference [11] is the same as the sum of C_{bci} and C_{bcx} from optimization. Although the effective collector area of HBT-B is a little bit



Frequency 0.1 to 20 GHz

(a)



Frequency 0.1 to 20 GHz

(b)

Fig. 7. Measured and modeled S -parameters for (a) HBT-B and (b) HBT-C at V_{ce} of 2.5 V and I_c of 10 mA. \square , \circ , ∇ and Δ are measured data and \ast , \times , \times and $+$ are modeled data.

larger than that of HBT-A giving a small C_{bcx} of HBT-A, the base resistance of HBT-A is higher possibly due to the large resistance on the mesa slope. It may be noted from Table I that the base resistances are similar for HBT-B and HBT-C indicating the advantage of this approach over ion implantation method.

C. RF Performance

The cutoff frequency and maximum oscillation frequency versus collector current density and collector-emitter bias are shown in Fig. 8 for HBT-B and HBT-C. The values of f_{maxU}

TABLE I
OPTIMIZED PARAMETER VALUES OF SMALL-SIGNAL EQUIVALENT
CIRCUIT FOR HBT'S AT V_{ce} OF 2.5 V AND I_c OF 10 mA

	HBT-A	HBT-B	HBT-C
C_{bcx} (fF)	13	15	39
C_{bci} (fF)	15	15	20
C_e (pF)	0.15	0.18	0.18
R_{cc} (Ω)	1.0	1.0	0.5
R_b (Ω)	17	13	13
R_{bb} (Ω)	1.7	1.7	1.5
R_{ee} (Ω)	10.5	6.0	8.5
α_o	0.956	0.973	0.975
τ (ps)	1.7	1.6	1.6

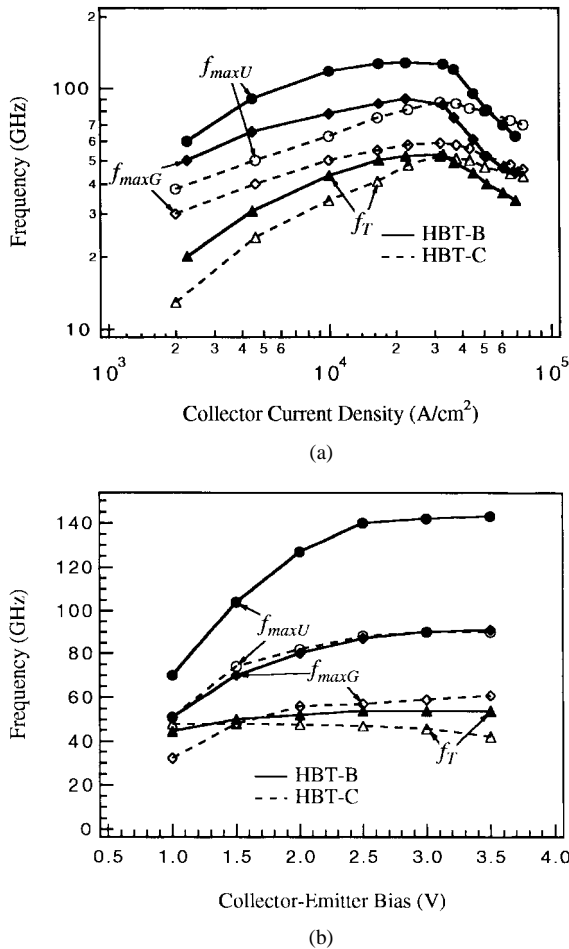


Fig. 8. (a) f_{maxU} , f_{maxG} , and f_T versus collector current density at V_{ce} of 2.5 V; and (b) f_{maxU} , f_{maxG} , and f_T , versus collector-emitter bias at J_c of $2.2 \times 10^4 A/cm^2$ for HBT-B (solid lines with symbols) and HBT-C (dashed lines with symbols).

and f_{maxG} for HBT-B are about 40–50% higher than those of HBT-C before the onset of the Kirk effect. f_T of HBT-B is about 10–20% higher compared with that of HBT-C due to the smaller C_{BC} . The peak f_{maxU} of 140 GHz, f_{maxG} of 90 GHz and f_T of 50 GHz for HBT-B were obtained at V_{ce} of 2.5 V and J_c of $2.2 \times 10^4 A/cm^2$. The values of f_{maxU} , f_{maxG} and f_T become higher than above after $V_{ce} > 2.5 V$ [see Fig. 8(b)]. Owing to the slightly high base resistance and low current gain of HBT-A, the measured f_{maxU} of 100 GHz

and f_{maxG} of 80 GHz (not shown in figures) for HBT-A are lower than those of HBT-B, but they are about 30% higher than those of HBT-C. From the relation of f_{max} and C_{BC} , if f_T and R_b are fixed, a 50% reduction in C_{BC} results in a 41% increase in f_{max} . Considering the slightly higher f_T of HBT-B, a 50% increase in f_{max} is reasonable.

From Fig. 8(a), Kirk effect in HBT-B is more pronounced than that in HBT-C, which results from the rapid increase of C_{BC} for HBT-B after the onset of Kirk effect. The reason for the more pronounced Kirk effect is due to the smaller effective collector area of HBT-B.

IV. CONCLUSION

A C-doped GaInP/GaAs HBT using a selective buried sub-collector was fabricated. It is shown that the regrown interface does not affect the device performance under normal device operation. Both current gain and breakdown voltage for the HBT with SBSC are same as those of a conventional HBT indicating the high quality of the regrown material. High performance of HBT's can be obtained with the properly alignment of the emitter mesa to the sub-collector mesa. A 50% reduction in C_{BC} and a 40–50% increase in f_{max} are observed with this technology. A maximum oscillation frequency of 140 GHz and a cutoff frequency of 50 GHz have been obtained. The device performance can be further improved by reducing the emitter size. It is demonstrated that the selective buried sub-collector provides an effective technique for reducing the extrinsic base-collector capacitance while keeping the base resistance unchanged for a GaInP/GaAs HBT.

REFERENCES

- [1] P. M. Asbeck, M. C. F. Chang, J. A. Higgins, N. H. Sheng, G. J. Sullivan, and K. C. Wang, "GaAlAs/GaAs heterojunction bipolar transistors: Issues and prospects for applications," *IEEE Trans. Electron Devices*, vol. 36, pp. 2032–2042, 1989.
- [2] M. E. Kim, A. K. Oki, G. M. Gorman, D. K. Umemoto, and J. B. Camou, "GaAs heterojunction bipolar transistor device and IC technology for high-performance analog and microwave applications," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 1286–1303, 1989.
- [3] J. Shirakashi, T. Azuma, F. Fukuchi, M. Konagai, and K. Takahashi, "InGaP/GaAs heterojunction bipolar transistors with an ultra-high carbon-doped base," *Jpn. J. Appl. Phys.*, vol. 34, pp. 1204–1207, 1995.
- [4] O. Nakajima, K. Nagata, Y. Yamauchi, H. Ito, and T. Ishibashi, "Improvement in AlGaAs/GaAs HBT power gains with buried proton-implanted layer," *Electron. Lett.*, vol. 22, pp. 1317–1318, 1986.
- [5] P. M. Asbeck, D. L. Miller, R. J. Anderson, and F. H. Eisen, "GaAs/AlGaAs heterojunction bipolar transistors with buried oxygen-implanted isolation layers," *IEEE Electron Device Lett.*, vol. EDL-5, pp. 310–312, 1984.
- [6] M. C. Ho, R. A. Johnson, W. J. Ho, M. F. Chang, and P. M. Asbeck, "High-performance low-base-collector capacitance AlGaAs/GaAs heterojunction bipolar transistors fabricated by deep ion implantation," *IEEE Electron Device Lett.*, vol. 16, pp. 512–514, 1995.
- [7] J. Song, M. R. Frei, J. R. Hayes, R. Bhat, and H. M. Cox, "Self-aligned InAlAs/InGaAs heterojunction bipolar transistor with a buried subcollector grown by selective epitaxy," *IEEE Electron Device Lett.*, vol. 15, pp. 123–125, 1994.
- [8] Y. F. Yang, C. C. Hsu, E. S. Yang, and Y. K. Chen, "Comparison of GaInP/GaAs heterostructure-emitter bipolar transistors and heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 42, pp. 1210–1215, 1995.
- [9] D. W. Shaw, "Localized GaAs etching with acidic hydrogen peroxide solutions," *J. Electrochem. Soc.*, vol. 128, pp. 874–880, 1981.
- [10] Y. F. Yang, C. C. Hsu, and E. S. Yang, "A high frequency and low noise C-doped GaInP/GaAs heterojunction bipolar transistor grown by

MOCVD using TBA and TBP," *Electron. Lett.*, vol. 32, pp. 689–691, 1996.

- [11] D. Pehkle and D. Pavlidis, "Evaluation of the factors determining HBT high-frequency performance by director analysis of *s*-parameter data," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 2367–2373, 1992.
- [12] P. F. Lindquist and W. M. Ford *GaAs FET Principles and Technology*, J. V. DiLorenzo and D. D. Khandelwalch, Eds. Norwood, MA: Artech House, 1982, ch. 1.
- [13] R. J. Krantz, D. C. Mayer, and W. L. Bloss, "The influence of Fermi-level pinning at the GaAs substrate on HEMT threshold voltage," *Solid-State Electron.*, vol. 33, pp. 1189–1195, 1990.
- [14] HP-EEsof Series IV, *Circuit User's Guide and Circuit Test Bench Catalog*, Hewlett-Packard, Westlake Village, CA, 1994.



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