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Charging Effect on Electrical Characteristics of MOS Structures with Si Nanocrystal Distribution in Gate Oxide

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We report a study of influence of charging and discharging in Si nanocrystals (nc-Si), which are embedded throughout the gate oxide in metal-oxide-semiconductor (MOS) structures, on the current-voltage and capacitance-voltage characteristics of the MOS structures. Very large current and capacitance are observed for the as-fabricated structures. However, charge trapping in the nanocrystals can reduce both the current and the capacitance dramatically. The trapped charges can also tunnel out from the nc-Si, leading to the recovery of both the current and the capacitance. The current reduction is attributed to the breaking of the nc-Si tunneling paths due to charge trapping in the nc-Si, while capacitance reduction is explained by an equivalent circuit in terms of the change of the nc-Si capacitance as a result of the charge trapping.
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Recently, Si nanocrystals (nc-Si) embedded in SiO_2 films have been studied extensively because such films can be used as active layers for single-electron devices and Si-based light-emitting devices (for example, see Ref. 1-3). For the application of single-electron devices, it is essential to have detailed information about the charge storage and or charge transport of the nc-Si in metal-oxide-semiconductor (MOS) structures. Some relevant research on this issue has been reported,[4-7] but usually the studies were carried out with memory-cell structures with the nanocrystals confined in a narrow layer embedded in the gate dielectrics. However, it would be interesting to examine the effects of charge storage and charge transport when the nc-Si distributes throughout the whole gate dielectric. For such a study, MOS capacitors containing nc-Si that distributes throughout the gate oxide with the nc-Si concentration peak close to the gate have been fabricated in this work. Using such MOS structures, some interesting phenomena related to charge transport such as the dramatic changes in the current and capacitance of the structures have been observed.

Silicon wafers were (100) oriented, boron-doped with a concentration of 2×10^{15} cm^{-3}. Si^+ ions were implanted at 14 keV with a dose of 3×10^{16} cm^{-2} into 30 nm SiO_2 films, which were thermally grown on Si wafers in dry oxygen at 950°C. The TRIM simulation shows that the Si ions distribute throughout the gate oxide with the peak concentration at a depth of about 20 nm below the SiO_2 surface, which is consistent with the secondary-ion mass spectroscopy (SIMS) result obtained after thermal annealing. Thermal annealing was carried out at 1000°C in N_2 ambient for 1 h to induce the nc-Si formation. Then the oxide layer was thinned in a diluted HF solution, and a 15 nm oxide was etched off so that the nc-Si concentration peak was located close to the surface. X-ray diffraction (XRD) measurement clearly showed the existence of nc-Si in the SiO_2 film. Figure 1a and b show the Bragg peaks due to the nc-Si before and after the etching off of 15 nm oxide, respectively. For both cases, the broadened Bragg peaks clearly showed the existence of nc-Si (with a mean size of ~4 nm as determined from the Pesudo-Voigt fit). In addition to the XRD measurement, we have also conducted some transmission electron microscopy (TEM) measurements for samples fabricated under similar conditions. The TEM measurement also showed the existence of nc-Si with a size of ~5 nm. Finally a 20 nm layer of aluminum was deposited on the oxide to form a 100×100 μm gate electrode. Ohmic contact on the back side of the wafer was formed by a standard aluminum alloy process. Current-voltage (I-V) and capacitance-voltage (C-V) measurements were performed with the Keithley 4200 semiconductor characterization system and the HP4284A LCR meter at a frequency of 1 MHz, respectively.

The I-V characteristics shown in Fig. 2a were obtained by sweeping the voltage from 0 to +5 V before and after applying +8 V to the MOS structure for 10 s. The curve for the virgin case (*i.e.*, before the application of +8 V) followed a power law, which is

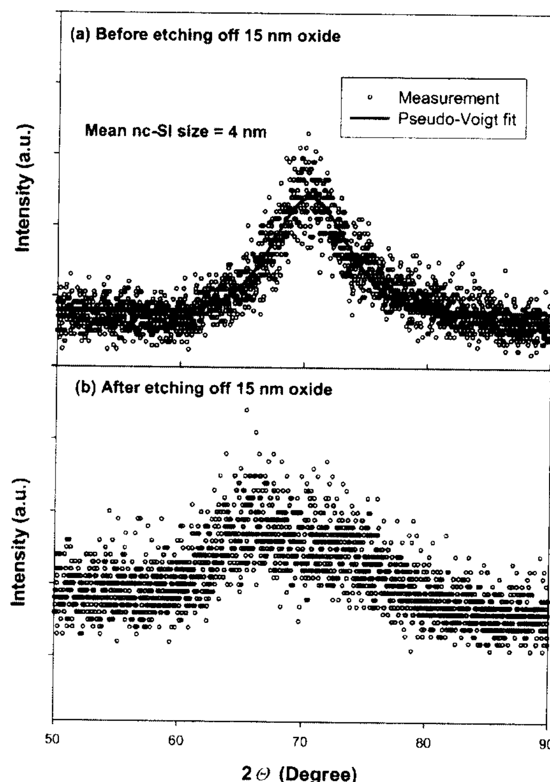

Figure 1. XRD measurements for nc-Si embedded in SiO_2 thin films; (a) before eching off 15 nm oxide and (b) after etching off 15 nm oxide (see the text).

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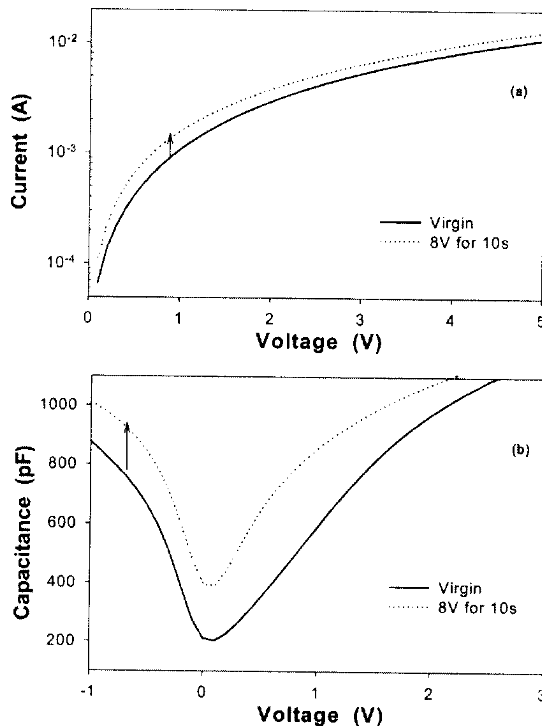

Figure 2. (a) I-V characteristics of the MOS structures before (*i.e.*, the virgin case) and after applying +8 V to the MOS structure for 10 s and (b) C-V characteristics of the MOS structures before (*i.e.*, the virgin case) and after applying +8 V to the MOS structure for 10 s.

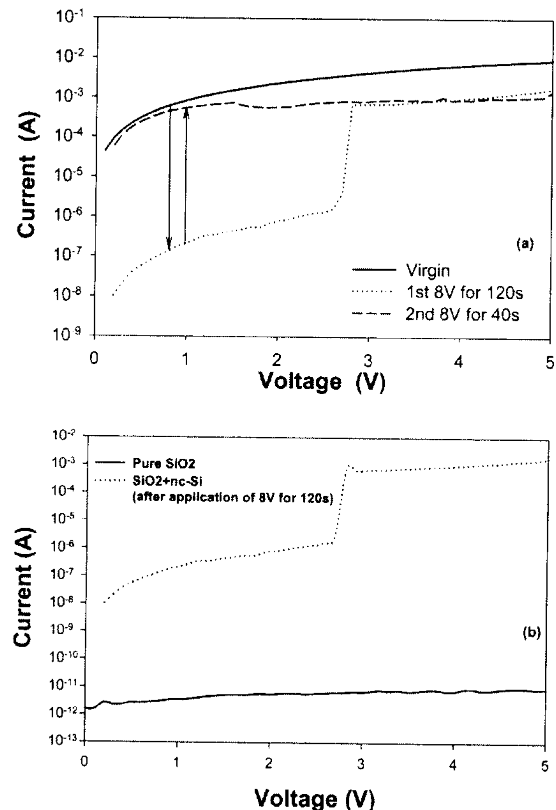

Figure 3. (a) Demonstration of the decrease and increase in the tunneling current after two applications of +8 V for different durations; (b) comparison of I-V characteristics between pure SiO_2 and SiO_2 containing nc-Si after the application of +8 V for 120 s.

similar to a typical post-breakdown I-V characteristic[8-12] of pure SiO_2 thin films. The current is over seven orders higher than that for pure SiO_2 film with identical oxide thickness as shown in Fig. 3b. This indicates that the nc-Si plays a key role in the current transport. As discussed below, the neutral (or uncharged) nc-Si can form tunneling paths connecting the Si substrate to the metal gate, and thus a large current can be expected. As shown in Fig. 2a, the application of +8 V for 10 s leads to a significant increase in the current. The application of voltage can also increase the capacitance of the MOS structure significantly, as shown in Fig. 2b. The capacitance of the MOS structures was measured from depletion to inversion. The C-V characteristics suggest an inversion of the Si substrate surface for all positive values of applied gate voltage during the C-V measurement. The increases in both the current and the capacitance are due to the discharge of the previously trapped charges in the nc-Si, which were trapped during the first I-V measurement, as a result of the application of the voltage. As shown in Ref. 13, the capacitance increases with the number of uncharged nanocrystals. Thus the discharge leads to a larger capacitance. At the same time, as more uncharged nanocrystals are available due to the discharge, more tunneling paths are formed giving rise to an increase in the current.

The application of a voltage can also charge up the nc-Si, leading to a decrease in the current. Figure 3a shows the I-V characteristics for the following situations: (*i*) virgin; (*ii*) after the first application of +8 V for 120 s; and (*iii*) the second application of +8 V for 40 s. The application of +8 V for 120 s leads to a dramatic current drop to a lower level (about four orders lower) in the voltage range of 0 to ~3 V in the I-V measurement. Such a current reduction can be explained in terms of the breaking of some tunneling paths due to the charge up in certain nanocrystals as a result of the application of the voltage. However, as can be seen in Fig. 3a, the current jumps to a higher level when the measurement voltage is larger than ~3 V, indicating that the I-V measurement itself can also lead to the discharge of some charged nanocrystals modifying the current conduction. The second application of +8 V for 40 s leads to the recovery of the current almost to its value of the virgin situation in the measurement voltage range of 0 to ~1 V, but the current drops a little bit to the values of the first application of +8 V for 120 s in the measurement voltages larger than ~3 V. Again these changes in the current are due to changes in the tunneling paths as a result of charge and discharge in the nc-Si.

The charge and discharge in nc-Si, which are responsible for the scenario shown in Fig. 3a, have serious impact on the C-V characteristics also, as shown in Fig. 4a. In this figure, the MOS capacitance was also measured from depletion to inversion. The application of +8 V for 120 s leads to the charge up of most of the nc-Si, which can be concluded from the dramatic reduction in the current shown in Fig. 3a. As the number of uncharged nc-Si has decreased dramatically, the capacitance drops to a very low level (~600 fF), which is even smaller than the capacitance for pure SiO_2 MOS structure as shown in Fig. 4b. After the second application of +8 V for 40 s, the current shows a recovery as shown in Fig. 3a, indicating a large increase of the number of uncharged nc-Si. Due to the increase of the number of uncharged nc-Si, the capacitance increases accordingly, as shown in Fig. 4a. It is clear from the above discussions that an increase (or decrease) in the current means an increase

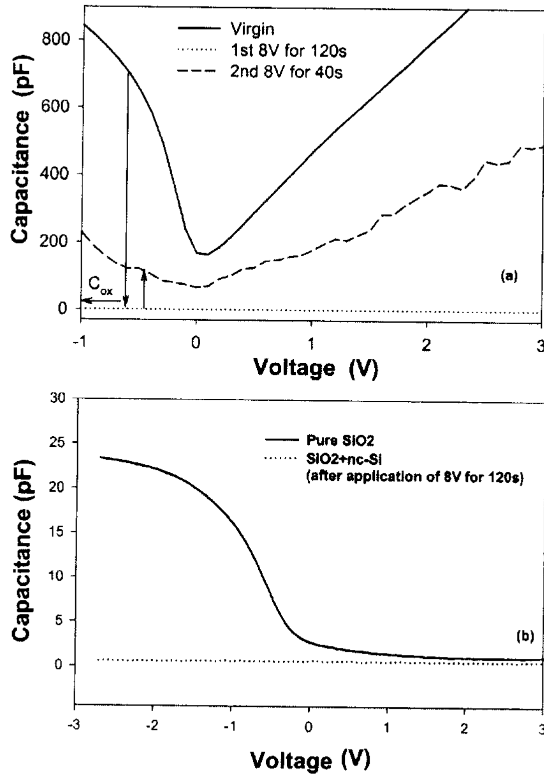

Figure 4. (a) Decrease and increase in capacitance after two applications of +8 V for different durations; (b) comparison of MOS capacitance between pure SiO_2 and SiO_2 containing nc-Si after the application of +8 V for 120 s.

(or decrease) in the capacitance also, and the changes in both the current and the capacitance are due to the discharge or charge of the nc-Si. More explanations are given below.

The effect of charge/discharge of nc-Si on the current conduction can be clearly illustrated with Fig. 5. Electron tunneling can take place between adjacent uncharged nanocrystals, and many such nanocrystals form tunneling paths connecting the Si substrate to the metal gate as shown in Fig. 5a. The nc-Si can be charged or discharged under the influence of a voltage. If some nanocrystals in a tunneling path are charged up, then the tunneling path is blocked by the charged nanocrystals and thus the current path disappears, as shown in Fig. 5b. Obviously, the current conduction of the MOS structure is determined by the tunneling paths, and thus the change of the current conduction is only the reflection of the disappearing/appearing of the tunneling paths due to the charge/discharge in the nc-Si.

To explain the changes in the capacitance shown in Fig. 2 and Fig. 4, an equivalent capacitance model is proposed here. Charge could be stored in the three elements, *i.e.*, the nanocrystals, the remaining gate oxide capacitor, and the Si depletion layer as shown in Fig. 6. The corresponding capacitances of the elements are denoted by C_{nc}, C'_{ox}, and C_D, respectively. The total capacitance C of the MOS structure is

$$C = \frac{(C_{nc} + C'_{ox})C_D}{(C_{nc} + C'_{ox}) + C_D} \qquad [1]$$

As C_D is very large, the total capacitance is approximately equal to $(C_{nc} + C'_{ox})$. With charge trapping in the nanocrystals, the nano-

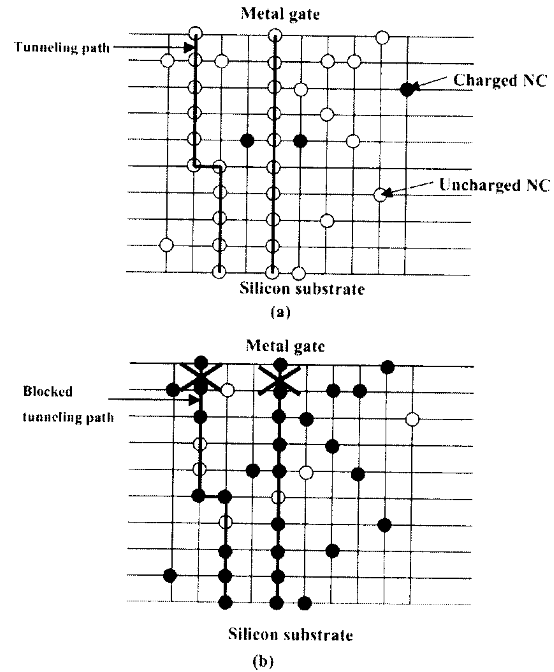

Figure 5. (a) Schematic illustration of the formation of tunneling paths between adjacent uncharged nanocrystals in the oxide; (b) illustration of the blocked tunneling paths resulting from charge trapping in some nanocrystals of the tunneling paths.

crystal capacitance C_{nc} should decrease as the numbers of uncharged nanocrystals or available electronic states responding to the small ac signal in the C-V measurement are reduced. With a high concentration of Si nanocrystals in the gate oxide locating close to the gate, many SiO_2 structures close to the gate are replaced by the nc-Si, and the MOS capacitor behavior is screened by the nc-Si. Thus, the remaining gate oxide capacitance C'_{ox} (*i.e.*, the capacitance

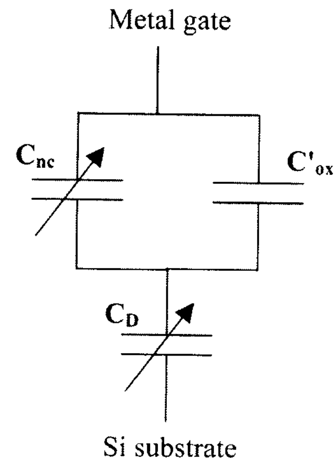

Figure 6. Equivalent capacitance circuit for the MOS structure with nc-Si embedded in the gate oxide.

from SiO_2 excluding the capacitance from nc-Si) should be much smaller than the conventional gate oxide capacitance (C_{ox}) without nanocrystals. As C'_{ox} is very small but the virgin C under accumulation is much larger than the C_{ox} of a conventional MOS capacitor ($C_{ox} = \sim 23$ pF), the C_{nc} before charge trapping in the nanocrystals should be much larger than the C_{ox}. However, as the nanocrystals are charged up, the C_{nc} is reduced, and thus the total capacitance C is reduced. If almost all nanocrystals are charged up, then the C_{nc} will be very small, and thus the total capacitance C will be very small as the C'_{ox} is also very small. This explains the reduction of the capacitance to a very low level after the first application of +8 V for 120 s as shown in Fig. 4a. The discharge of some charged nc-Si leads to the increase in the C_{nc} and thus gives rise to the increase in the total capacitance as shown in Fig. 2b.

In summary, MOS structures containing nc-Si embedded throughout the gate oxide were fabricated by thinning the Si^+ implanted SiO_2 layer thermally grown on Si substrate. Very large current and capacitance are observed for the as-fabricated structures. It is observed that charge transport via the nc-Si can strongly modify the current conduction and the capacitance of the MOS structures. The charge trapping in the nanocrystals can reduce both the current and the capacitance dramatically. The trapped charges can also tunnel out from the nc-Si under a bias, leading to the recovery of both the current and the capacitance. The current reduction is attributed to the breaking of the nc-Si tunneling paths due to the charge trapping in the nc-Si, while the capacitance reduction is explained by an equivalent circuit in terms of the change of the nc-Si capacitance as a result of the charge trapping.

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