Quality improvement of low-pressure chemical-vapor-deposited oxide by N_2O nitridation

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Quality of low-pressure chemical-vapor-deposited (LPCVD) oxide and N_2O-nitrided LPCVD (LN2ON) oxide is investigated under high-field stress conditions as compared to thermal oxide. It is found that LPCVD oxide has lower midgap interface-state density $D_{\text{it-m}}$ and smaller stress-induced $D_{\text{it-m}}$ increase than thermal oxide, but exhibits enhanced electron trapping rate and degraded charge-to-breakdown characteristics, which, however, are significantly suppressed in LN2ON oxide, suggesting effective elimination of hydrogen-related species. Moreover, LN2ON oxide shows further improved Si/SiO_2 interface due to interfacial nitrogen incorporation. © *1997 American Institute of Physics.* [S0003-6951(97)02808-8]

Low-pressure chemical-vapor-deposition (LPCVD) oxide is finding increasingly widespread applications in the field of microelectronics, such as gate dielectric for thin-film transistors in high-density static random-access memories[1] and stacked gate dielectric for metal–oxide–semiconductor field-effect transistors[2] (MOSFETs). Two primary problems encountered in using LPCVD oxide were significant bulk trappings[3–5] and high defect density.[6] To reduce defect density, a stacked thermal LPCVD gate oxide technology was developed,[2,6] however, bulk trapping still has no satisfactory solution. In addition, improvement in the quality of Si/SiO_2 interface is also an inevitable concern. For this reason, the N_2O-nitridation technique was applied to LPCVD oxide[7] and some improvements were achieved in terms of midgap interface-state generation $\Delta D_{\text{it-m}}$ and shift of flatband voltage ΔV_{fb}. In this letter, besides further descriptions of $\Delta D_{\text{it-m}}$ and ΔV_{fb}, improvements on charge-to-breakdown Q_{bd}, and change in gate voltage during constant-current stress ΔV_g, electron-trap generation and trapping rates are also reported and the involved mechanisms are analyzed.

MOS capacitors used in this study were fabricated on p-type (100) silicon wafers with a resistivity of 6–8 Ω cm by a self-aligned n^+ polysilicon-gate process. All oxidation and anneal processes were performed in a conventional horizontal furnace. LPCVD oxide (LOX) was deposited at 450 °C, 33.8 Pa using silane and oxygen. The flow rate of SiH_4 and O_2 were 0.75 and 100 sccm, respectively, which resulted in a low and controllable deposition rate of about 3 Å/min and good thickness uniformity. After deposition some samples were subjected to a 1000 °C anneal in N_2 ambient for 35 min, which makes the LPCVD oxide densified and H_2-related by products diffuse out of the oxide. Other samples received *in situ* nitridation at the same temperature and for the same time in pure N_2O ambient (LN2ON). Thermal oxide (OX) was grown at 850 °C for 70 min in dry O_2 to serve as control sample and then annealed at 1000 °C for 35 min, or 900 °C for 35 min in N_2 ambient (denoted as OX1 and OX2, respectively) to improve the quality of the Si/SiO_2 interface and oxide bulk to a different extent. Connection to gate electrode was formed by Al metallization and sintering in forming gas at 430 °C for 30 min following n^+ polysilicon-gate preparation. The area of the capacitors was 10^{-4} cm^2. Designed oxide thicknesses are 140 and 110 Å for OX and LOX oxides, respectively, which is mainly based on the consideration that LOX oxide would be thickened by ~25% after N_2O nitridation at 1000 °C for 35 min.[8] As a result, final oxide thicknesses measured by the capacitance–voltage ($C-V$) technique are 145, 145, 115, and 150 Å for OX1, OX2, LOX, and LN2ON oxides, respectively, with the thickness of LOX oxide increased by 30% after N_2O nitridation. All constant-current stresses were performed with electron injection from the gate, i.e., a negative gate bias. Midgap interface-state density $D_{\text{it-m}}$, flatband voltage V_{fb}, and fixed charge Q_f were determined by high-frequency and quasistatic $C-V$ measurements.

The initial Q_f and $D_{\text{it-m}}$ of the four MOS capacitors extracted from $C-V$ data have comparable values ($Q_f=1.2–2.1\times10^{11}$ cm^{-2}, $D_{\text{it-m}}=3.35–5.94\times10^{10}$ cm^{-2} eV^{-1}); however, different behaviors occur among the four dielectrics under high-field stress. Presented in Fig. 1 is $\Delta D_{\text{it-m}}$ under constant-current injection of -1 mA/cm^2 for the four dielectrics. Surprisingly, a smaller $\Delta D_{\text{it-m}}$ for LOX sample than OX sample is observed. This might imply that smoother SiO_2/Si interface for LOX oxide than OX oxide is formed[9] and the interfacial strain of LOX oxide is relieved to a larger extent than OX oxide during the high-temperature anneal in N_2.[10] To show the advantages of the annealing step, $\Delta D_{\text{it-m}}$ of OX1 and OX2 samples are compared in Fig. 1. As can be seen, OX1 sample exhibits slightly improved interface hardness than OX2 sample, which obviously results from the formation of stronger Si—O bonds at the interface[11] and a larger reduction of interfacial stress[12] at a higher annealing temperature. For N_2O-nitrided LPCVD oxide,

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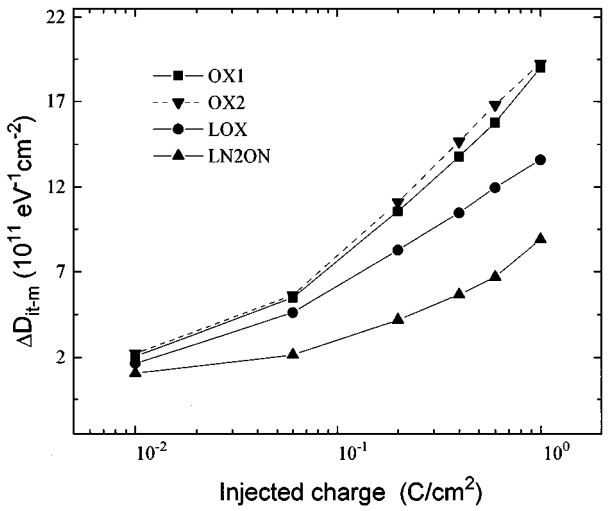

FIG. 1. Midgap interface-state creation $\Delta D_{\text{it-m}}$ of MOS capacitors with different gate dielectrics under constant-current injection stress of -1 mA/cm^2.

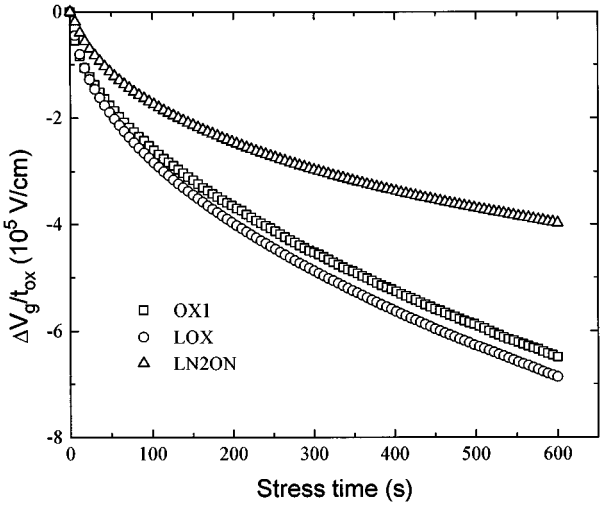

FIG. 3. Normalized change in gate voltage vs time during constant-current stressing (-10 mA/cm^2).

$\Delta D_{\text{it-m}}$ is more greatly reduced than LOX oxide, demonstrating the distinctive advantage of oxynitrides—an excellent interface hardness against hot-carrier bombardment as a result of interfacial nitrogen incorporation.

Shown in Fig. 2 is the corresponding ΔV_{fb} under the same stress conditions as those used in Fig. 1. The four dielectrics all display a negative-going shift in V_{fb} after stress, indicating hole trapping. Like $\Delta D_{\text{it-m}}$ in Fig. 1, ΔV_{fb} for OX1 is also slightly smaller than the one for OX2 because of slightly better interface qualities achieved at higher annealing temperature. Moreover, ΔV_{fb} for LOX sample is less than for OX samples, which is similar to that reported in Ref. 13. It is well known that ΔV_{fb} is the combined effect of charge trapping at the substrate interface and in the bulk oxide, and mainly reflects the charges near the Si/SiO_2 interface.[14] Hole trapping is likely due to generated donorlike interface states[15] and bulk trapping, which are positively charged when they are unoccupied under $C-V$ measurement

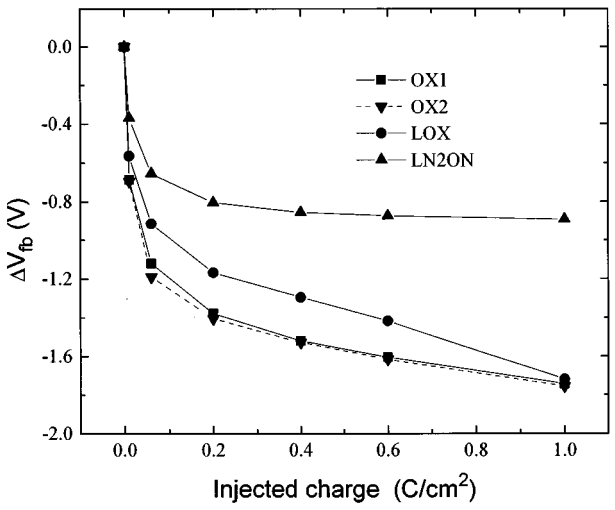

FIG. 2. Flatband voltage shift of MOS capacitors with injected charge under the same stress conditions as those in Fig. 1.

conditions. So, considering the results in Fig. 1, it can be deduced that LOX sample should have a lower donorlike interface-state creation than OX samples in the entire charge-injection range. However, it could not be concluded that bulk hole trapping in LOX oxide is less than OX oxide because the influence of hole trapping might be partly canceled by significant electron trapping in the bulk of LOX oxide as analyzed in the next paragraph; but, undoubtedly, both are considerably improved by the N_2O nitridation as shown in Fig. 2. Lastly, the ΔV_{fb} saturation of LN2ON sample with injected charge in Fig. 2 depicts again its better interface resistance against stress-induced degeneration and less bulk trapping than LOX and OX oxides.

Figure 3 shows the change in gate voltage ΔV_g during constant-current stressing (-10 mA/cm^2) for the oxides. Between the two thermal-oxide samples, OX1 sample is chosen for comparison purpose because it has better qualities and, more importantly, has about the same thermal budget as LOX and LN2ON samples. Unlike ΔV_{fb}, ΔV_g is very sensitive to charges located near the cathode. So, to eliminate the effect of oxide thickness t_{ox}, ΔV_g is normalized by respective oxide thickness. The increase of gate voltage during stressing implies electron trapping. Obviously, LPCVD oxide suffers from the highest electron-trap generation and trapping rates among the three oxides (see Fig. 4 below), which is similar to that reported in Ref. 13, and probably due to hydrogen-related species such as $-H$ and $-OH$ produced by the thermal decomposition of silane during deposition. However, LN2ON oxide shows only a small ΔV_g, suggesting greatly suppressed electron trapping. This indicates that N_2O nitridation for LOX oxide is very effective in annealing out the hydrogen species, hence reducing electron-trap generation and trapping rates.

Depicted in Fig. 4 are charge-to-breakdown Q_{bd} and corresponding electron-trap generation and trapping rates for the three oxides under different injection current densities $-J_g$. Q_{bd} of LOX sample is much lower than that of OX1 sample. This can be associated with two possible causes: a large defect density and enhanced electron trapping rate in the LPCVD oxide film.[16] Since Q_{bd} of LOX dielectrics is

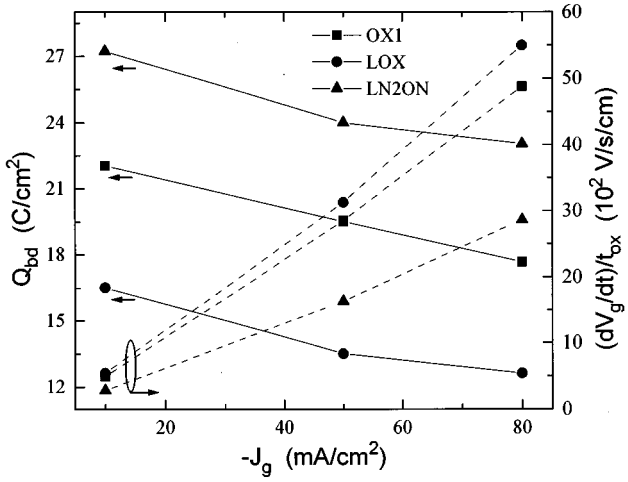

FIG. 4. Charge-to-breakdown Q_{bd} and electron trap generation/trapping rate dV_g/dt as a function of injection current density.

significantly improved after N_2O nitridation in our experiments and the charge trapping rate at localized defect sites in LPCVD oxide is lower than that in thermal oxide,[5] it can be suggested that Q_{bd} degradation is likely due to enhanced electron-trap generation and trapping rates induced by hydrogen-related species in our LOX oxide, which is proportional to the slope of the gate-voltage shift versus time during constant-current injection, i.e., dV_g/dt of the linear part of the curves in Fig. 3. It can clearly be seen that the higher the dV_g/dt, the lower the Q_{bd}.[16] The Q_{bd} and dV_g/dt values are averaged over 20 capacitors, and dV_g/dt is similarly normalized by respective oxide thickness. It can be evaluated that N_2O nitridation makes Q_{bd} of our LOX dielectrics increase by a factor of 1.6–1.8, and the corresponding dV_g/dt decrease by approximately the same factor.

In summary, N_2O-nitrided LPCVD oxide exhibits considerably suppressed electron-trap creation and trapping rates, excellent charge-to-breakdown characteristics and interface immunity against interface-state generation due to interfacial nitrogen incorporation, and reduction of H_2-related byproducts resulting from silane decomposition. Therefore, to obtain high-quality LPCVD gate dielectrics and enhanced device reliability, N_2O nitridation of deposited oxide is a very promising way. Even for stacked thermal/LPCVD gate oxide, the same treatment would probably result in further improvement of interface and bulk qualities of the composite oxide.

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