Nano Research

Open Access

Research Article

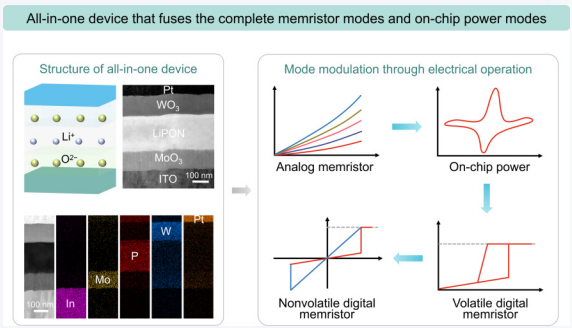
All-in-one iontronic device with memory, processing and power capabilities towards dust-sized computers

Dong Wang[1], Mingyang Wang[1], Zhihan Zhang[1], Jian Wang[1], Ziye Zhou[1], Peter To Lai[2], and Xiaodong Huang[1] ✉

[1] School of Integrated Circuits, Southeast University, Nanjing 210096, China
[2] Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong 999077, China

Cite this article: *Nano Research*, **2025**, *18*, 94907043. https://doi.org/10.26599/NR.2025.94907043

ABSTRACT: Fusion of memory, processing and power components enables creating autonomous and monolithically-integrated dust-sized computers for ubiquitous computing. However, this effort is limited by contradictory ion dynamics and performance variability of each component. Here we report an all-in-one dual-ion device that integrates memory, processing and power functionalities. By electrically modulating ion species (Li^+ and O^{2-}) and amounts participating in the electrochemistry, the complete memristor modes (including analog, volatile digital and nonvolatile digital types) and on-chip power modes are created on demand in this device. Because of their distinct properties, the roles of Li^+ and O^{2-} are easily distinguished and modulated by electrical operation for meeting the customized demand of each mode. Moreover, the homogeneous migration of Li^+ ensures high uniformity of the Li^+-based modes. The oxygen vacancy-based conductive filaments are finely defined by mechanical deformation through electrically controlling ion intercalation/deintercalation, thus guaranteeing high uniformity of the O^{2-}-based modes. Both neuromorphic and logic in-memory computing are well demonstrated based on this all-in-one device.



KEYWORDS: all-in-one fusion, memristor, on-chip power, ion dynamics, performance uniformity

1 Introduction

As an emerging class of computing platform, dust-sized computers (or called smart dusts) have attracted increasing interest due to their tiny size (< 1 mm^3) [1]. This causes that they display a great potential in applications that have demanding constraints on power and form factor, such as implantable medicals and edge computing in the internet of things [2, 3]. Besides information memory and processing components, microscale energy-storage component (e.g., supercapacitors and batteries) is also encouraged to be integrated into the dust-sized computers as on-chip power for forming an autonomous microsystem [4–6]. This enables the dust-sized computers to be available anywhere anytime, thus realizing ubiquitous computing.

So far, the dust-sized computers have been constructed by using three-dimensional (3D) heterogeneous integration, in which each component is stacked together by using wire bonding to form electrical connections [7, 8]. As an alternative, monolithic integration cannot only make the dust-sized computers more compact and miniaturized, but also improve their performance and energy efficiency by reducing the connection length and relevant parasitic effects. However, realizing a monolithically-integrated dust-sized computer is still challenging and is mainly hindered by fabrication complexity and incompatibility issues resulting from its heterogeneous components, particularly, the energy component differs substantially from the information ones in terms of their materials, structures and working principles [9–13].

All-in-one fusion of these heterogeneous components is quite desirable for achieving the monolithic integration (Fig. 1(a)). For instance, memristor, which fuses the information memory and processing components together (known as in-memory computing), not only simplifies the fabrication complexity by avoiding preparing each component individually, but improves the energy efficiency by avoiding frequent data shuttling between these two components [14, 15]. It is expected that the monolithic integration of the dust-sized computers can be further promoted by fusing the information and energy components together. This expectation is inspired by recent progresses of iontronic devices, which are based on ions as both information and energy carriers, thus providing feasibility of fusing the information and energy components [16–18]. However, this effort is limited by

Received: August 22, 2024; **Revised:** September 12, 2024
Accepted: September 18, 2024

✉Address correspondence to xdhuang@seu.edu.cn

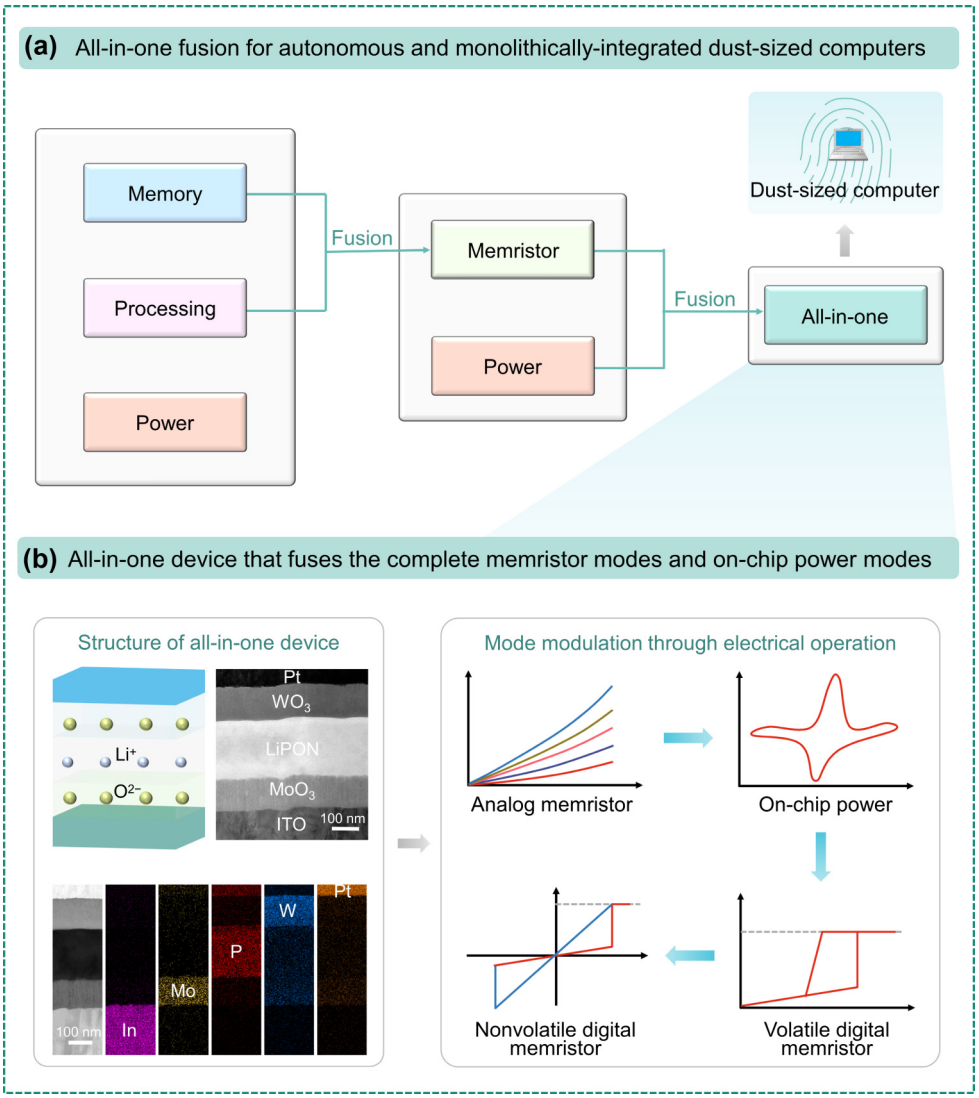


Figure 1 All-in-one iontronic device. (a) All-in-one fusion of the memory, processing and power components is quite desirable for constructing autonomous and monolithically-integrated dust-sized computers. (b) Schematic diagram, cross-sectional TEM and EDX mapping images of this all-in-one device (left). This all-in-one device acts as a stem cell that can be electrically tuned to the complete memristor modes and on-chip power modes (right).

contradictory ion dynamics required in each component. For instance, memristors usually rely on localized ion migration in conductive filaments; on the contrary, localized ion migration makes most active materials idle (rather than participating in energy storage) and forms filament-like structures (commonly known as dendrites), thus degrading their energy density and cycling lifespan of the energy-storage devices [19, 20]. Moreover, the stochastic nature of ion migration causes the iontronic devices suffer from performance variability and low yield, which make them difficult in practical use [21, 22]. The above two reasons lead to that a high-performance all-in-one device that fuses information and energy components is still unavailable.

In this article, we report an all-in-one iontronic device with dual-ion (Li^+ and O^{2-}) configuration, as seen in Fig. 1(b). By electrically modulating the ion species (Li^+ and O^{2-}) and their amounts participating in the electrochemical processes, the complete memristor modes (including analog, volatile digital and nonvolatile digital types) and on-chip power modes can be created on demand in this single device (Fig. 1(b)). It is noting that Li^+ and O^{2-} display distinct properties: Li^+ has low diffusion barrier and large diffusion coefficient while O^{2-} is opposite. Consequently, Li^+ intrinsically presents spatially homogeneous migration and works at a low voltage; for comparison, O^{2-} presents localized migration and only takes effect at a high voltage. Therefore, the roles of Li^+ and O^{2-} can be easily distinguished and modulated by using electrical operation for satisfactorily meeting the customized demand of each mode respectively. Therefore, the contradictory ion dynamics required in each component can be addressed. Moreover, the homogeneous migration of Li^+ results in the high performance uniformity of the Li^+-based modes. Through electrically controlling the mechanical deformation induced by ion intercalation/deintercalation, localized O^{2-} migration can be finely defined within a narrow-fixed region, thus improving the performance uniformity of the O^{2-}-based modes. As a result, each mode presents good performance with high uniformity, including: (i) analog memristor with large dynamic range (the maximum conductance of the device/the minimum conductance of the device (G_{max}/G_{min}) ~ 57.5) and quite small variation (~ 1%) of conductance modulation; (ii) on-chip power with both high energy and power densities (7.0 μWh/cm^2 at 27.9 μW/cm^2); (iii) volatile digital memristor with relatively high

selectivity (~ 10^2) and small variation (~ 2%); (iv) nonvolatile digital memristor with long retention time (> 10^5 s) and small variation (~ 3%). As a proof of concept, both neuromorphic and logic in-memory computing are also demonstrated based on this all-in-one device. This work paves a new strategy for developing area- and energy-efficient dust-sized computers.

2 Results and discussion

2.1 Principles of the all-in-one device

An all-in-one iontronic device with a Pt/WO_3/LiPON/MoO_3/ITO structure is presented. Figure 1(b) shows its cross-sectional transmission electron microscopy (TEM) images combined with energy dispersive X-ray (EDX) elemental mappings. All the layers are clearly distinguished with abrupt interfaces, demonstrating the uniform deposition of each layer. In this device, Pt and ITO act as the top and bottom electrodes, respectively; WO_3, LiPON and MoO_3 act as the anode, electrolyte and cathode, respectively. WO_3, LiPON and MoO_3 are chosen as the active materials mainly because they have memory, processing and power functions as well as good compatibility with the semiconductor processes [23–28]. This structure includes two kinds of ions (Li^+ and O^{2-}) that are active to participate in the electrochemical processes. Due to their distinct properties, the roles of Li^+ and O^{2-} are easily distinguished and modulated by electrical operation for meeting the customized demand of each mode. In addition, it is noted that Pt and ITO have opposite mechanical properties: Pt has quite low yield strength and high ductility [29, 30]; by contrast, ITO is the opposite [31, 32]. Therefore, Pt and ITO are easy and difficult to deform, respectively. Through electrically tuning the ion kinetics, the mechanical stress induced by ion intercalation/deintercalation can be easily controlled, thus modulating the deformation of the Pt layer. This deformation is effective to improve the device performance uniformity by defining the formation/rupture of the conductive filaments. The details will be discussed latter.

This as-prepared all-in-one device acts as a stem cell and the complete memristor modes and the on-chip power modes can be created on demand by modulating the ion species (Li^+ and O^{2-}) as well as their amounts participating in the electrochemical processes through electrical operation, as seen in Figs. 2(a) and 2(b). The homogeneous migration of Li^+ ensures high performance uniformity of the Li^+-based modes. Moreover, the performance uniformity of the O^{2-}-based modes can be significantly improved by defining the formation/rupture of oxygen vacancy (V_O)-based conductive filaments within a narrow-fixed region. The above efforts make sure that each mode has good performance with high uniformity. The working and modulation principles of each mode are described below.

(i) Analog memristor mode. For the pristine device, because of its low diffusion barrier and large diffusion coefficient, Li^+ presents spatially homogeneous migration between the anode and cathode films under an electrical stimulus (Fig. 2(c)) [33]. Two processes simultaneously occur as Li^+ intercalates/deintercalates in the films: (1) Li^+ has electrochemical reactions with the active films, resulting in electrochemical energy storage; (2) Li^+ also acts as dopant and thus changes the films electrical conductivity. Since the Li^+ amount far exceeds the values that the electrochemical reactions can accommodate in the pristine device, the second process dominates. Consequently, Li^+ intercalation/deintercalation caused by consecutive electrical stimuli lead to gradual change in conductance. Therefore, the pristine device works in the analog memristor mode.

(ii) On-chip power mode. Li^+ intercalation/deintercalation are known to induce mechanical stress and deformation, which become more obvious at a lower program-voltage sweep rate due to enhanced Li^+ transfer kinetics [34]. Therefore, by slowing down the sweep, the induced mechanical stress is large enough to stretch the Pt layer because of its low yield strength and high ductility (Fig. 2(d)). The stretching effect creates porosity at the center of the Pt layer, where the maximum stress occurs. Then, air penetrates through the porosity and has irreversible reactions with Li^+, consuming a significant amount of Li^+ in the device. Consequently, the electrochemical energy storage described in the first process dominates. The corresponding device behaves as supercapacitor and is electrically tuned to the on-chip power mode. Note that the homogeneous migration property of Li^+ guarantees that the active films are sufficient to participate in the energy storage. This is quite desirable to improve the energy density and cycling lifespan of the device as on-chip power.

(iii) Volatile digital memristor mode. By increasing the program voltage combined with a small compliance current (I_{CC}), the oxygen ions (O^{2-}) in the films are activated to become mobile and start to dominate in the following processes. Owing to its high diffusion barrier and small diffusion coefficient, O^{2-} intrinsically presents spatially localized migration in filaments (rather than homogeneous migration like Li^+) [33]. The formation/rupture of the V_O-based conductive filaments causes binary-like switching of the device conductance, and thus the device is electrically turned to the volatile digital memristor mode (Fig. 2(e)).

(iv) Nonvolatile digital memristor mode. By further increasing the program voltage combined with a large I_{CC}, more mobile O^{2-} are created and participate in the following processes. Compared with that in the volatile digital memristor mode, the V_O-based conductive filaments in this condition are robust due to their large V_O amount. Consequently, the device is electrically tuned to the nonvolatile digital memristor mode (Fig. 2(f)). It is worth mentioning that the stochastic nature of the formation/rupture of the filaments causes an inherent performance variability issue in the oxygen-based memristor [35]. The geometric deformation at the center of the Pt electrode induces local electric-field enhancement, which directionally induces and defines the filaments formation/rupture within a narrow-fixed region and thus is desirable to address the performance variability issue under both the volatile digital memristor and nonvolatile digital memristor modes.

2.2 Analog memristor mode

Figure 3(a) shows the current–voltage (I–V) curves of the pristine device under consecutive direct-current (DC) voltage sweeps (the sweep rate is 1 $V \cdot s^{-1}$). The conductance gradually increases and decreases with sequential negative and positive sweeps, respectively, demonstrating the analog resistive switching characteristics of the device. These characteristics are quite suitable for mimicking the plasticity of biological synapses. As seen in Fig. S1(a) in the Electronic Supplementary Material (ESM), the dependence of Li^+ conductivity (σ) on temperature obeys the Arrhenius equation and the corresponding activation energy E_A is extracted to be 0.5 eV, which is much lower than those of other ion species (e.g., ~ 1.7 eV for O^{2-}) [36], suggesting Li^+ is much easier to migrate and thus plays the dominant role in the analog memristor mode. Therefore, the analog resistive switching phenomenon also occurs even when the

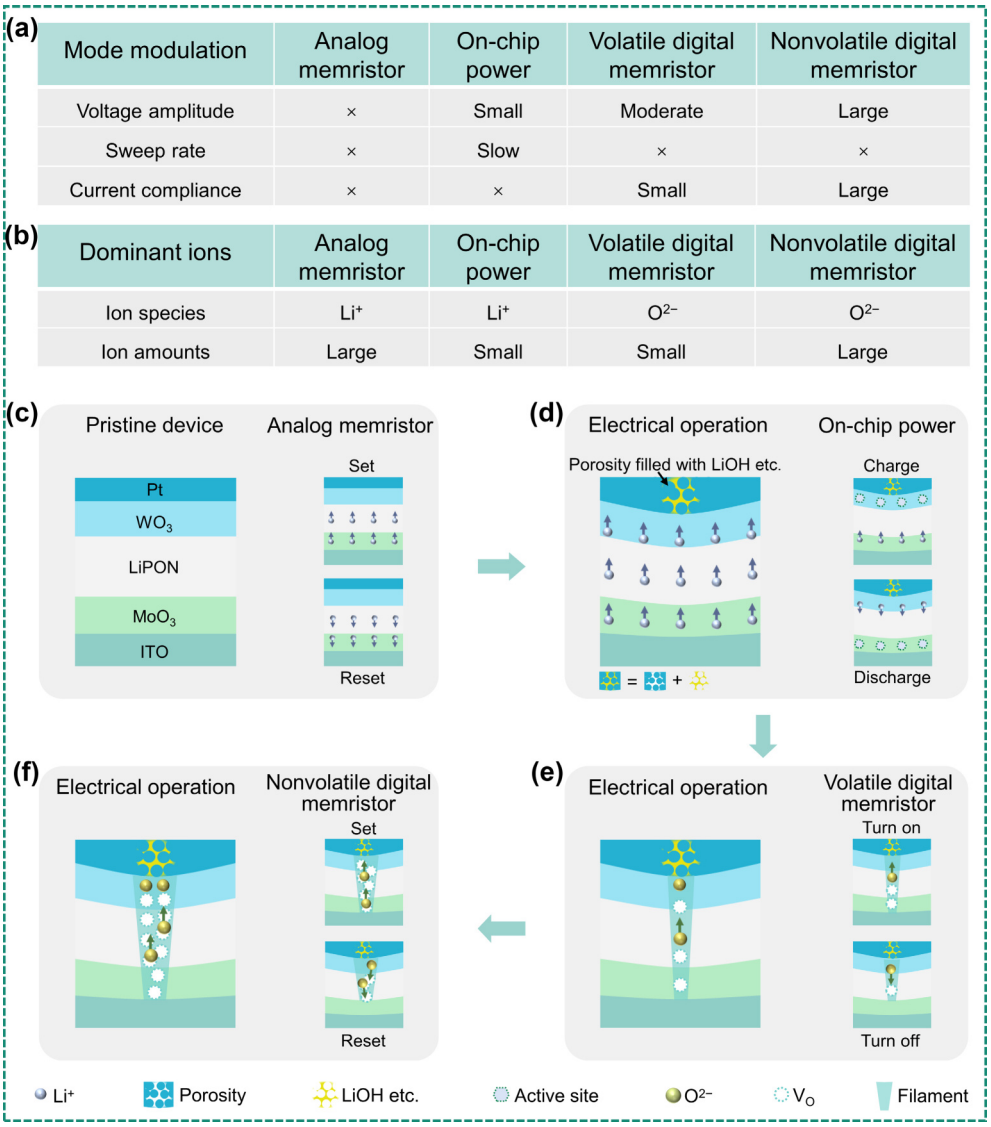


Figure 2 Modulation and working principles of this all-in-one iontronic device. (a) Mode modulation through electrical operation. (b) Dominant ion species and their amounts under each mode. (c) Under the analog memristor mode. (d) Under the on-chip power mode. (e) Under the volatile digital memristor mode. (f) Under the nonvolatile digital memristor mode.

sweep voltage is as low as ±0.5 V (Fig. S1(b) in the ESM). As seen in Fig. 3(b), the analog resistive switching can be also operated by applying voltage pulses. The conductance gradually increases and then tends to saturate with the negative pulse (−5 V, 5 ms); for comparison, the positive pulse (+5 V, 5 ms) causes the conductance decrease and saturation. These behaviors can be used for mimicking long-term potentiation (LTP) and long-term depression (LTD) processes of biological synapses. Moreover, the conductance modulation can be also realized by adjusting the pulse amplitude and a large modulation range (G_{max}/G_{min} ~ 57.5) is obtained for the device. As seen in Fig. 3(c), the device presents relatively small nonlinearity (~ 0.6/−7.7) and quite small cycle-to-cycle variation (~ 1%) mainly because of the homogeneous migration nature of Li^+. Based on the crossbar simulator (CrossSim), the MNIST recognition is simulated by adapting this all-in-one device as synapse and the recognition accuracy (~ 97%) is close to the ideal value (~ 98%) that CrossSim can achieve, demonstrating its potential in the neuromorphic in-memory computing (Figs. S1(c) and S1(d) in the ESM).

2.3 On-chip power mode

By reducing the Li^+ amount in the device through intentionally introducing irreversible reactions, the device can be tuned to the on-chip power mode. As seen in Fig. 3(d), the device displays a strong oxidation peak by reducing the sweep rate (≤ 50 mV/s) mainly due to the reaction of Li^+ with air. This oxidation peak disappears in the following sweeps (Fig. S2 in the ESM), suggesting that the reactions are irreversible and self-limiting. The detailed reaction mechanisms will be discussed later. These irreversible reactions consume excessive Li^+, thus causing the device to change from analog memristor mode to on-chip power mode. As demonstrated in Fig. 3(e), the device behaves as a supercapacitor and displays electrochemical energy storage characteristics with a pair of reversible redox peaks in the cyclic-voltammetry (CV) curves. Figure S3(a) in the ESM shows the galvanostatic charge/discharge (GCD) curves at different current densities. The device exhibits high areal capacitance (~ 4.1 mF/cm^2) with gradual degradation as the current increases (Fig. S3(b) in the ESM). As seen in Fig. 3(f), the device also operates well in both series and parallel connections,

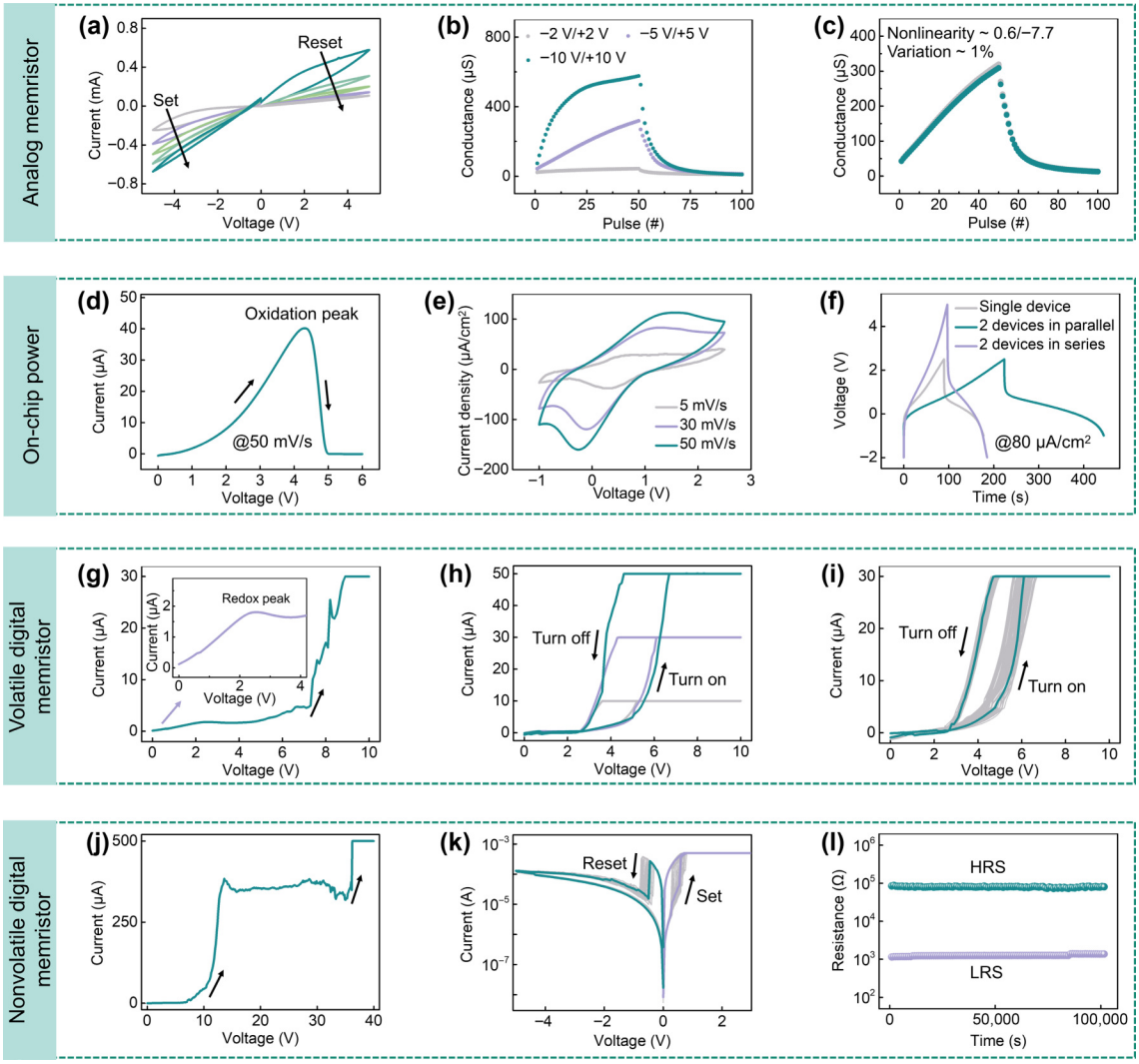


Figure 3 Performance characterizations of this all-in-one iontronic device under each mode. (a) *I*–*V* curves under consecutive negative and positive DC voltage sweeps for the device under the analog memristor mode. (b) Conductance modulation by voltage pulses with different magnitudes for the device under the analog memristor mode. (c) Cycle-to-cycle variation of conductance modulation for the device under the analog memristor mode. (d) Program process used for tuning the device to the on-chip power mode. (e) Cyclic-voltammetry curves at different sweep rates for the device under the on-chip power mode. (f) Galvanostatic charge–discharge curves obtained from two devices connected in series and parallel, respectively. (g) Program process used for tuning the device to the volatile digital memristor mode. (h) Volatile digital resistive switching characteristics under various compliant currents for the device under the volatile digital memristor mode. (i) *I*–*V* curves for 100 consecutive DC voltage sweep cycles for the device under the volatile digital memristor mode. (j) Program process used for tuning the device to the nonvolatile digital memristor mode. (k) *I*–*V* curves for 100 consecutive DC voltage sweep cycles for the device under the nonvolatile digital memristor mode. (l) Retention characteristics of the device under the nonvolatile digital memristor mode.

and the corresponding voltage and capacitance are twice as large as those of a single device respectively, suggesting its good performance uniformity and ability as on-chip power to meet various customized power demands. Figure S3(c) in the ESM exhibits the Ragone plots for this work as compared with other typical on-chip supercapacitors in the literature [37–39], and high energy density and high power density (7.0 μWh/cm^2 at 27.9 μW/cm^2) can be simultaneously achieved for the device. The device also presents a low self-discharge rate (Fig. S3(d) in the ESM). In addition, a good charge/discharge cycling lifespan with negligible capacity degradation over 3500 cycles can be obtained (Fig. S3(e) in the ESM).

2.4 Volatile digital memristor mode

By changing the ion species (from Li^+ to O^{2-}) participating in the electrochemical processes through an electroforming process, the device can be tuned to the volatile digital memristor mode. As seen in Fig. 3(g), the electroforming process is performed by increasing the program voltage at a small compliance current (I_{CC} < 100 μA). After this operation, O^{2-} in the films is activated to become mobile and then participates in the following processes. As seen in the inset of Fig. 3(g), the current peak at around 2.5 V corresponds to the Li^+-related electrochemical processes as discussed above (Fig. 3(e)). According to Fig. 3(g), the O^{2-}-induced current (~ 30.0 μA) is much larger than the Li^+-induced current (~ 1.8 μA), suggesting that O^{2-} plays the dominant role in the following processes. Figure 3(h) shows the *I*–*V* curves of the device under forward/backward sweeps between 0 and 10 V with various I_{CC}. The curves present volatile characteristics: When the applied voltage is above the threshold voltage (V_{th}), the current increases rapidly to reach I_{CC}, and then returns to off-state spontaneously as the applied voltage is swept back and below the hold voltage (V_{hold}). The V_{th} and V_{hold} under

different I_{CC} are similar. Figure 3(i) shows the *I*–*V* curves of the device under 100 consecutive sweeps. The selectivity is 10^2 with a relatively low off-current (~ 10^{-7} A, or 10^{-3} A/cm^2). Figure S4 in the ESM exhibits the cumulative distributions of V_{th} and V_{hold} extracted from the 100-cycle *I*–*V* curves. The variation (defined as the standard deviation divided by the mean value) is only 2% for V_{hold} and 4% for V_{th}, demonstrating good performance uniformity due to local electric-field enhancement caused by mechanical deformation as discussed later.

2.5 Nonvolatile digital memristor mode

By increasing the mobile O^{2-} amount in the device through an electroforming process, the device can be tuned to the nonvolatile digital memristor mode. As seen in Fig. 3(j), when the electroforming operation is performed by further increasing the program voltage at a large I_{CC} (≥ 500 μA), more mobile O^{2-} are created and then participate in the following processes. Note that the I_{CC} magnitude is critical and used to modulate the V_O amount. Unlike that in the volatile digital memristor mode, these V_O-based conductive filaments are robust enough due to their large V_O amount and can be retained even after removing the applied voltage. As a result, the device can be tuned to the nonvolatile digital memristor mode. The *I*–*V* curves display bipolar and nonvolatile digital resistive switching behaviors (Fig. 3(k)). Figure S5 in the ESM shows the high resistance state (HRS) and low resistance state (LRS) as a function of temperature, both of which present a semiconductor behavior with resistance decreasing linearly with increasing temperature. These are typical characteristics of V_O-based (rather than metallic ion-based, e.g., Li^+-based) conductive filaments. Figure S6 in the ESM exhibits the HRS/LRS (variation ~ 7% for HRS and 3% for LRS) cumulative probabilities extracted from the 100-cycle *I*–*V* curves. Both of them display uniform distributions due to local electric-field enhancement induced by the mechanical deformation as discussed later, which suppresses the stochastic formation/rupture of the filaments. As seen in Fig. 3(l), the HRS and LRS exhibit excellent retention with negligible degradation even after 10^5 s. Based on the good bipolar and nonvolatile digital resistive switching characteristics of the device, typical logic functions (including AND, OR and NOT) are well demonstrated in Figs. S7–S9 in the ESM, suggesting its capability of logic in-memory computing.

2.6 Ion dynamics of the all-in-one device

As seen in Figs. 4(a)–4(c), the 3D morphologies of the all-in-one device under various modes are constructed based on the chemical information collected by time-of-flight secondary ion mass spectroscopy (ToF-SIMS). For the device under the analog memristor mode, each layer is smooth (Fig. 4(a)). On the contrary, for the device under the on-chip power mode, its anode/electrolyte/cathode (WO_3/LiPON/MoO_3) layers display obvious deformation due to mechanical stress induced by Li^+ intercalation/deintercalation (Fig. 4(b)). This stress is greatly determined by Li^+ kinetics and can be enhanced by decreasing the sweep rate. Moreover, owing to its quite low yield strength and high ductility, the Pt layer, which is closely attached to the WO_3 layer, is stretched by the WO_3 deformation. This is consistent with the phenomenon that the inner surface (the Pt/WO_3 interface) of the Pt layer is deformed while its outer surface remains smooth (Fig. 4(b)). The stretching effect creates porosity at the center of the Pt layer, where the maximum stress occurs. Then, air penetrates through the porosity and reacts with Li^+ based on the following reactions (Eqs. (1)–(3))[40–42].

$$4Li + O_2 \rightarrow 2Li_2O \tag{1}$$

$$2Li + H_2O + 1/2O_2 \rightarrow 2LiOH \tag{2}$$

$$2Li + CO_2 + 1/2O_2 \rightarrow Li_2CO_3 \tag{3}$$

These reactions are irreversible and consume a large amount of Li^+ in the device. This supports that the lithium content in the device under the on-chip power mode is lower than that under the analog memristor mode. Therefore, energy storage (rather than doping) dominates in the subsequent processes and the device is tuned to the on-chip power mode. The above analysis is further confirmed by the 3D maps of secondary ion species obtained from ToF-SIMS (Figs. 4(d) and 4(e)). For the device under the on-chip power mode, the ion species (including Li^-, OH^-, LiO^-, CO_3^-, and CO_3Li^-), which are the products in the reactions (Eqs. (1)–(3)), indeed are concentrated at the center of the Pt layer (Fig. 4(e)); for comparison, these ions species cannot be found in the Pt layer for the device under the analog memristor mode (Fig. 4(d)). It is worth mentioning that once the reactions (Eqs. (1)–(3)) occur, their products fill the porosity in the Pt layer to block the air penetration and thus further reactions with Li^+. Therefore, the reactions are self-limiting in the device. This agrees well with the fact that once the reactions happen, the device works stably in the long term even in air (Fig. S10 in the ESM). Note that owing to the low diffusion barrier and large diffusion coefficient of Li^+, geometric deformation has negligible effect on the Li^+ transport [33]. Therefore, similar to that under the analog memristor mode (Fig. 4(g)), it still displays homogenous migration for the device under the on-chip power mode (Fig. 4(h)). This is desirable to enhance the energy density, cycling lifespan and performance uniformity of the all-in-one device as on-chip power.

In order to gain more insight into the all-in-one device switching from the analog memristor mode to the on-chip power mode, the device under various operating conditions was also characterized. When working under both the air ambient and high sweep rate, the device presents analog resistive switching characteristics (Figs. S11(a) and S11(b) in the ESM). This is because the mechanical stress under fast sweep is not high enough to cause the stretching (and thus porosity formation) of the Pt layer. Consequently, air cannot penetrate through Pt to react with Li^+. This causes numerous Li^+ in the device, thus resulting in its analog resistive switching characteristics. When working under vacuum and low sweep rate, the device still displays analog resistive switching characteristics (Figs. S11(c) and S11(d) in the ESM). Although the slow sweep has capability to create high mechanical stress and thus porosity in the Pt layer, no air is provided to participate in the reactions (Eqs. (1)–(3)). Therefore, the device has numerous Li^+ and shows analog resistive switching characteristics because the doping effect dominates. These results demonstrate that the change of mode can be achieved by adjusting the Li^+ amount in the device based on the above three reactions and the electrically induced mechanical stress is effective to control the reactions and thus varies the mode of the device.

The effects of the top-electrode material on the ion modulation were also studied. The materials include Pt, Ag, Ti and ITO. The main difference among these materials is yield strength (Pt:

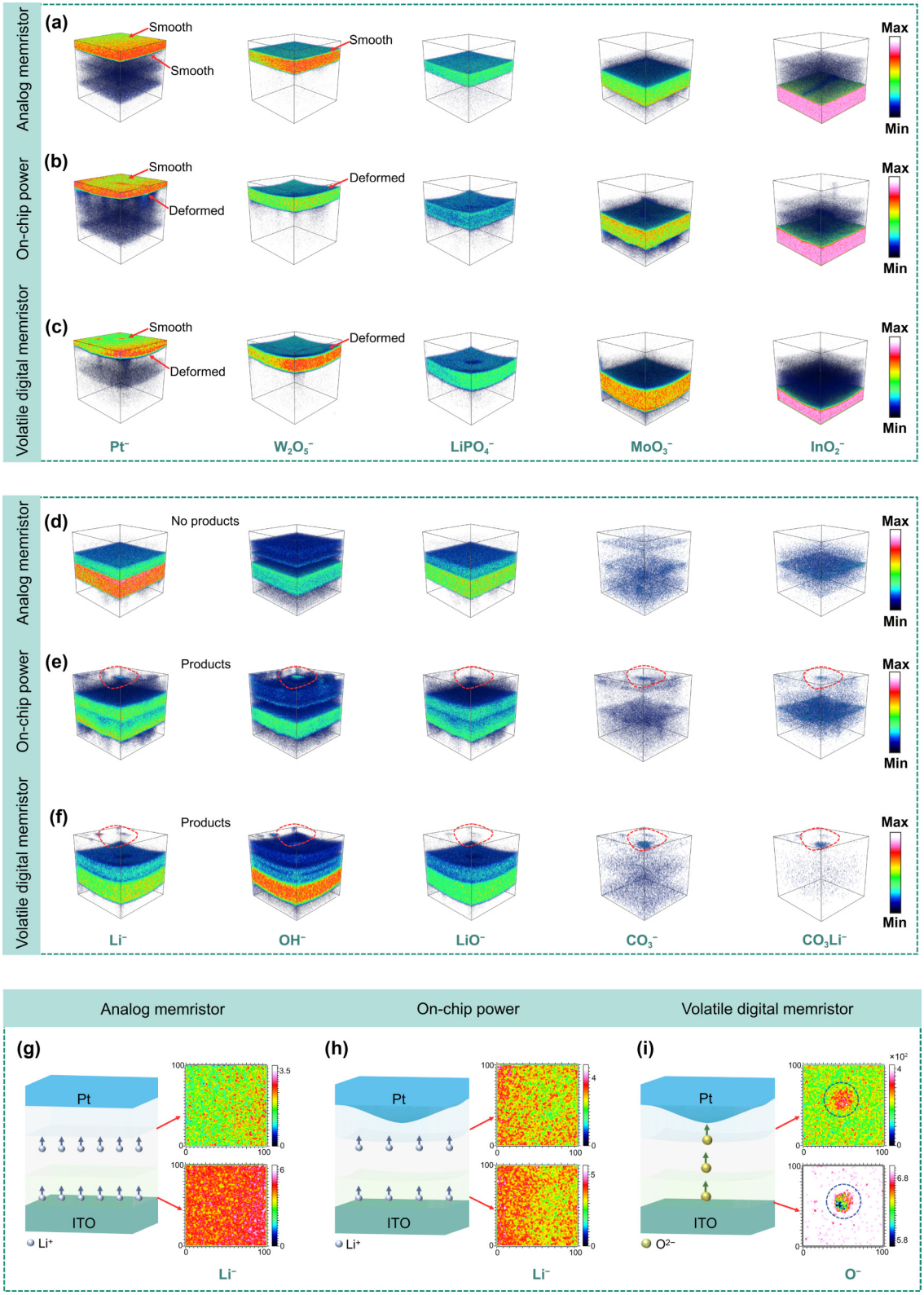


Figure 4 SIMS analysis for the all-in-one iontronic device under different modes. (a) 3D morphologies of each layer for the device under the analog memristor mode based on ToF-SIMS. (b) 3D morphologies of each layer for the device under the on-chip power mode based on ToF-SIMS. (c) 3D morphologies of each layer for the device under the volatile digital memristor mode based on ToF-SIMS. (d) 3D maps of secondary ion species (including Li^-, OH^-, LiO^-, CO_3^- and CO_3Li^-) for the device under the analog memristor mode based on ToF-SIMS. (e) 3D maps of secondary ion species (including Li^-, OH^-, LiO^-, CO_3^- and CO_3Li^-) for the device under the on-chip power mode based on ToF-SIMS. (f) 3D maps of secondary ion species (including Li^-, OH^-, LiO^-, CO_3^- and CO_3Li^-) for the device under the volatile digital memristor mode based on ToF-SIMS. Note that these ion species represent the products in the reactions (Eqs. (1)–(3)). (g) 2D distribution of the lithium elements along the depth profiles for the device under the analog memristor mode. (h) 2D distribution of the lithium elements along the depth profiles for the device under the on-chip power mode. (i) 2D distribution of the oxygen elements along the depth profiles for the device under the volatile digital memristor mode.

~ 10.0 MPa; Ag: ~ 56.6 MPa; Ti: ~ 840.0 MPa; ITO: ~ 1.2 GPa) [29, 31, 43, 44]. The lower the yield strength is, the more easily the plastic deformation occurs. As seen in Figs. S12(a) and S12(b) in the ESM, the irreversible reactions (Eqs. (1)–(3)) happen for the devices with Pt or Ag as the top electrode; by contrast, even under a quite low sweep rate, these reactions cannot occur for the ones with Ti or ITO top electrode mainly because of their high yield strengths (Figs. S12(c)–S12(f) in the ESM). Therefore, the mechanical stress induced by ion intercalation/deintercalation hardly causes the electrode plastic deformation, which is the prerequisite for porosity formation in the top electrode. Since no irreversible reactions occur for consuming excessive Li^+, the devices with the Ti or ITO top electrode show analog resistive switching characteristics and cannot be tuned to the on-chip power mode (Fig. S13 in the ESM). The above results suggest that the ion modulation can be facilely realized by rational material design.

The 3D morphology of each layer and 3D maps of secondary ion species for the device under the volatile digital memristor mode are also shown in Figs. 4(c) and 4(f), respectively, both of which are similar to those for the device under the on-chip power mode, suggesting that the device structure is stable. As discussed earlier, the volatile digital memristor mode mainly relies on the formation/rupture of the V_O-based conductive filaments. Owing to the stochastic nature of this process, an inherent performance variability issue exists in this type of memristor [35]. Herein, the considerable geometric deformation at the center of the Pt electrode leads to local electric-field enhancement, which causes directional O^{2-} migration just below the center of the Pt layer (as confirmed by Fig. 4(i)), thus defining formation/rupture of the V_O-based conductive filaments. This is quite helpful to improve the device performance uniformity (variation ~ 2% for V_{hold} and 4% for V_{th}). Note that the as-prepared device can be also directly tuned to the volatile digital memristor mode by using an electroforming process (Fig. S14 in the ESM). However, the corresponding device presents worse performance uniformity (variation ~ 5% for V_{hold} and 6% for V_{th}) than the one tuned from on-chip power mode to volatile digital memristor mode because the former has no geometric deformation (and thus no local electric-field enhancement). The as-prepared device can be also directly tuned to the nonvolatile digital memristor mode by an appropriate electroforming process (Fig. S15 in the ESM). Nevertheless, owing to the lack of electric-field enhancement, the corresponding device displays much worse performance uniformity (variation ~ 30% for LRS and 77% for HRS) than the one tuned from on-chip power mode to nonvolatile digital memristor mode (variation ~ 3% for LRS and 7% for HRS). The above comparisons validate the effectiveness of the electrically induced mechanical stress and deformation in improving the device performance uniformity under both the volatile digital memristor and nonvolatile digital memristor modes by tailoring the O^{2-} dynamics.

The resistance of each active film and the resistance of the all-in-one device under various modes are shown in Figs. S16(a) and S16(b) in the ESM, respectively. The electrolyte LiPON, which is known for high ionic and low electronic conductivities [45], displays much higher resistance than the WO_3 and MoO_3 films. Therefore, the device resistance is mainly determined by LiPON (Fig. S16(a) in the ESM). It is further found that the device resistance under the nonvolatile digital memristor mode decreases significantly compared with those under other modes and is even lower than the LiPON resistance, suggesting structural changes in the LiPON film (Fig. S16(b) in the ESM). As confirmed by XPS characterization in Fig. S17 in the ESM, for the LiPON film under the nonvolatile digital memristor mode, non-bridging compositions increase obviously because the high program voltage during the electroforming process breaks its phosphate chains. This leads to obvious increase in the O^{2-} amount and thus the device is tuned to the nonvolatile digital memristor mode.

It is worth noting that the potential fringe effect in the current all-in-one device is not obvious due to its large device size (200 μm in diameter). As the device size is further down scaled, the fringe effect would become severe [46–48]. The influences of this fringe effect on our all-in-one device are closely related to the device modes: (1) When the device works in the analog memristor and on-chip power modes, Li^+ plays the dominant role. Due to its low diffusion barrier and large diffusion coefficient, the fringe effect (or local electric field enhancement effect in our manuscript) has negligible effect on the Li^+ transport. This can be confirmed by 2D distribution of the lithium elements along the depth profiles for the device under the on-chip power mode (Fig. 4(h)), which shows that despite the enhanced electric field occurs at the center of the top Pt electrode, Li^+ still displays homogenous migration. (2) When the device works in the volatile and nonvolatile digital memristor modes, O^{2-} plays the dominant role. Due to its high diffusion barrier and small diffusion coefficient, the fringe effect (or local electric field enhancement effect in our manuscript) affects the O^{2-} transport and thus the device performance. This can be confirmed by 2D distribution of the oxygen elements along the depth profiles for the device under the volatile digital memristor mode (Fig. 4(i)), which shows that the enhanced electric field causes directional O^{2-} migration just below the center of the Pt layer. It has been demonstrated that rational electrode design can effectively suppress the fringe effect as well as its detrimental influence [49].

3 Conclusion

To sum up, we have reported an all-in-one dual-ion (Li^+ and O^{2-}) device that fuses memory, processing and on-chip power components. By electrically modulating the ion species and their amounts participating in the electrochemical processes, the complete memristor modes (including analog, volatile digital and nonvolatile digital types) and on-chip power modes can be created on demand in this single device. Due to their distinct properties, the roles of Li^+ and O^{2-} are easily distinguished and modulated by electrical operation for meeting the customized demand of each mode respectively. Therefore, the contradictory ion dynamics between each mode are addressed. Moreover, the homogeneous migration property of Li^+ results in the high performance uniformity of the Li^+-based modes. The performance uniformity of the O^{2-}-based modes is improved by defining the formation/rupture of the V_O-based conductive filaments within a narrow-fixed region, which is realized by the mechanical deformation through electrically controlling the ion intercalation/deintercalation kinetics. The above efforts guarantee this all-in-one device has excellent performance with high uniformity. As a proof of concept, both neuromorphic and logic in-memory computing are also well demonstrated. Our work paves a new strategy for developing autonomous and monolithically-integrated dust-sized computers with high area and energy efficiencies, thereby facilitating the realization of ubiquitous computing anywhere anytime.

Electronic Supplementary Material: Supplementary material (detailed experimental sections and the methods of neuromorphic

in-memory computing and logic in-memory computing, and additional electrical and electrochemical measurement data and the characterization of the LiPON films) is available in the online version of this article at https://doi.org/0.26599/NR.2025.94907043.

Data availability

All data needed to support the conclusions in the paper are presented in the manuscript and the ESM. Additional data related to this paper may be requested from the corresponding author upon request.

Acknowledgements

This work was supported by the National Natural Science Foundation of China (No. 61974026), the National Key R&D Program of China (No. 2020YFB2007400) and the Research Grants Council of the Hong Kong Special Administrative Region, China (No. T45-701/22-R).

Declaration of competing interest

All the contributing authors report no conflict of interests in this work.

Author contribution statement

D. W.: Data curation, data collection, validation, writing manuscript, experimental design. M. Y. W.: Data collection, data analysis. Z. H. Z.: Data collection, data analysis. J. W.: Data collection, data analysis. Z. Y. Z.: Data collection, data analysis. P. T. L.: Project administration, funding acquisition, polishing manuscript. X. D. H.: Data curation, experimental design, project administration, funding acquisition, writing manuscript.

Use of AI statement

None.

References

[1] Zhu, M. S.; Schmidt, O. G. Tiny robots and sensors need tiny batteries-here's how to do it. *Nature* **2021**, *589*, 195–197.

[2] Fischer, T.; Agarwal, A.; Hess, H. A smart dust biosensor powered by kinesin motors. *Nat. Nanotechnol.* **2009**, *4*, 162–166.

[3] Piech, D. K.; Johnson, B. C.; Shen, K.; Ghanbari, M. M.; Li, K. Y.; Neely, R. M.; Kay, J. E.; Carmena, J. M.; Maharbiz, M. M.; Muller, R. A wireless millimetre-scale implantable neural stimulator with ultrasonically powered bidirectional communication. *Nat. Biomed. Eng.* **2020**, *4*, 207–222.

[4] Li, Y.; Zhu, M. S.; Bandari, V. K.; Karnaushenko, D. D.; Karnaushenko, D.; Zhu, F.; Schmidt, O. G. On-chip batteries for dust-sized computers. *Adv. Energy Mater.* **2022**, *12*, 2103641.

[5] Ma, J. C.; Quhe, R.; Zhang, W. L.; Yan, Y. P.; Tang, H. M.; Qu, Z.; Cheng, Y. P.; Schmidt, O. G.; Zhu, M. S. Zn microbatteries explore ways for integrations in intelligent systems. *Small* **2023**, *19*, 2300230.

[6] Lee, Y.; Bandari, V. K.; Li, Z.; Medina-Sánchez, M.; Maitz, M. F.; Karnaushenko, D.; Tsurkan, M. V.; Karnaushenko, D. D.; Schmidt, O. G. Nano-biosupercapacitors enable autarkic sensor operation in blood. *Nat. Commun.* **2021**, *12*, 4967.

[7] Lee, Y.; Bang, S.; Lee, I.; Kim, Y.; Kim, G.; Ghaed, M. H.; Pannuto, P.; Dutta, P.; Sylvester, D.; Blaauw, D. A modular 1 mm^3 die-stacked sensing platform with low power i^2c inter-die communication and multi-modal energy harvesting. *IEEE J. Solid-State Circuits* **2013**, *48*, 229–243.

[8] Liu, A. T.; Hempel, M.; Yang, J. F.; Brooks, A. M.; Pervan, A.; Koman, V. B.; Zhang, G.; Kozawa, D.; Yang, S.; Goldman, D. I. et al. Colloidal robotics, *Nat. Mater.* **2023**, *22*, 1453–1462.

[9] Li, Y. X.; Song, S. B.; Kim, H.; Nomoto, K.; Kim, H.; Sun, X. Y.; Hori, S.; Suzuki, K.; Matsui, N.; Hirayama, M. et al. A lithium superionic conductor for millimeter-thick battery electrode. *Science* **2023**, *381*, 50–53.

[10] Kyeremateng, N. A.; Brousse, T.; Pech, D. Microsupercapacitors as miniaturized energy-storage components for on-chip electronics. *Nat. Nanotechnol.* **2017**, *12*, 7–15.

[11] Li, J. C.; Ren, S. G.; Li, Y.; Yang, L.; Yu, Y. J.; Ni, R.; Zhou, H. J.; Bao, H.; He, Y. H.; Chen, J. et al. Sparse matrix multiplication in a record-low power self-rectifying memristor array for scientific computing. *Sci. Adv.* **2023**, *9*, eadf7474.

[12] Zhang, W. B.; Yao, P.; Gao, B.; Liu, Q.; Wu, D.; Zhang, Q. T.; Li, Y. K.; Qin, Q.; Li, J. M.; Zhu, Z. H. et al. Edge learning using a fully integrated neuro-inspired memristor chip. *Science* **2023**, *381*, 1205–1211.

[13] Fu, Y. Y.; Zhou, Y.; Huang, X. D.; Gao, B.; He, Y. H.; Li, Y.; Chai, Y.; Miao, X. S. Forming-free and annealing-free V/VO_x/$HfWO_x$/Pt device exhibiting reconfigurable threshold and resistive switching with high speed (< 30 ns) and high endurance (> 10^{12}/> 10^{10}). In *Proceedings of the 2021 IEEE International Electron Devices Meeting* (*IEDM*), San Francisco, CA, USA, 2021, pp 12.6.1–12.6.4.

[14] Yao, P.; Wu, H. Q.; Gao, B.; Tang, J. S.; Zhang, Q. T.; Zhang, W. Q.; Yang, J. J.; Qian, H. Fully hardware-implemented memristor convolutional neural network. *Nature* **2020**, *577*, 641–646.

[15] Xu, G. H.; Zhang, M. L.; Mei, T. T.; Liu, W. C.; Wang, L.; Xiao, K. Nanofluidic ionic memristors. *ACS Nano* **2024**, *18*, 19423–19442.

[16] Yan, Y. P.; Tang, H. M.; Qu, Z.; Zhang, W. L.; Schmidt, O. G.; Zhu, M. S. Dynamic switching and energy storage unified by electrochemical ion intercalation. *Adv. Mater. Technol.* **2023**, *8*, 2200466.

[17] Li, T. M.; Xiao, K. Solid-state iontronic devices: Mechanisms and applications. *Adv. Mater. Technol.* **2022**, *7*, 2200205.

[18] Mastragostino, M.; Soavi, F. Pseudocapacitive and ion-insertion materials: A bridge between energy storage, electronics and neuromorphic computing. *ChemElectroChem* **2021**, *8*, 2630–2633.

[19] Li, Y.; Long, S. B.; Liu, Q.; Lv, H. B.; Liu, M. Resistive switching performance improvement via modulating nanoscale conductive filament, involving the application of two-dimensional layered materials. *Small* **2017**, *13*, 1604306.

[20] Yang, Q.; Li, Q.; Liu, Z. X.; Wang, D. H.; Guo, Y.; Li, X. L.; Tang, Y. C.; Li, H. F.; Dong, B. B.; Zhi, C. Y. Dendrites in Zn-based batteries. *Adv. Mater.* **2020**, *32*, 2001854.

[21] Li, Y. S.; Xiong, Y.; Zhai, B. X.; Yin, L.; Yu, Y. L.; Wang, H.; He, J. Ag-doped non-imperfection-enabled uniform memristive neuromorphic device based on van der Waals indium phosphorus sulfide. *Sci. Adv.* **2024**, *10*, eadk9474.

[22] Yufit, V.; Tariq, F.; Eastwood, D. S.; Biton, M.; Wu, B.; Lee, P. D.; Brandon, N. P. Operando visualization and multi-scale tomography studies of dendrite formation and dissolution in zinc batteries. *Joule* **2019**, *3*, 485–502.

[23] Zhang, F.; Zhang, Y.; Li, L. L.; Mou, X.; Peng, H. N.; Shen, S. C.; Wang, M.; Xiao, K. H.; Ji, S. H.; Yi, D. et al. Nanoscale multistate resistive switching in WO_3 through scanning probe induced proton evolution. *Nat. Commun.* **2023**, *14*, 3950.

[24] Hai, Z. Y.; Akbari, M. K.; Wei, Z. H.; Xue, C. Y.; Xu, H. Y.; Hu, J.; Zhuiykov, S. Nano-thickness dependence of supercapacitor performance of the ALD-fabricated two-dimensional WO_3. *Electrochim. Acta* **2017**, *246*, 625–633.

[25] Zhou, F. C.; Zhou, Z.; Chen, J. W.; Choy, T. H.; Wang, J. L.; Zhang, N.; Lin, Z. Y.; Yu, S. M.; Kang, J. F.; Wong, H. S. P. et al.

Optoelectronic resistive random access memory for neuromorphic vision sensors. *Nat. Nanotechnol.* **2019**, *14*, 776–782.
[26] Jia, Y. L.; Ma, Y. Advances in MoO_3-based supercapacitors for electrochemical energy storage. *J. Energy Storage* **2024**, *85*, 111103.
[27] Fuller, E. J.; Gabaly, F. E.; Léonard, F.; Agarwal, S.; Plimpton, S. J.; Jacobs-Gedrim, R. B.; James, C. D.; Marinella, M. J.; Talin, A. A. Li-ion synaptic transistor for low power analog computing. *Adv. Mater.* **2017**, *29*, 1604310.
[28] Cheng, D. Y.; Wynn, T. A.; Wang, X. F.; Wang, S.; Zhang, M. H.; Shimizu, R.; Bai, S.; Nguyen, H.; Fang, C. C.; Kim, M. C. et al. Unveiling the stable nature of the solid electrolyte interphase between lithium metal and LiPON via cryogenic electron microscopy. *Joule* **2020**, *4*, 2484–2500.
[29] Mantese, J. V.; Alcini, W. V. Platinum wire wedge bonding: A new IC and microsensor interconnect. *J. Electron. Mater.* **1988**, *17*, 285–289.
[30] Rakhtsaum, G. Platinum alloys: A selective review of the available literature. *Platinum Met. Rev.* **2013**, *57*, 202–213.
[31] Lee, S.; Kwon, J. Y.; Yoon, D.; Cho, H.; You, J.; Kang, Y. T.; Choi, D.; Hwang, W. Bendability optimization of flexible optical nanoelectronics via neutral axis engineering. *Nanoscale Res. Lett.* **2012**, *7*, 256.
[32] Lee, S.; Guo, L. J. Bioinspired toughening mechanisms in a multilayer transparent conductor structure. *ACS Appl. Mater. Interfaces* **2022**, *14*, 7440–7449.
[33] Zhu, Y. T.; Gonzalez-Rosillo, J. C.; Balaish, M.; Hood, Z. D.; Kim, K. J.; Rupp, J. L. M. Lithium-film ceramics for solid-state lithionic devices. *Nat. Rev. Mater.* **2021**, *6*, 313–331.
[34] Han, S. Y.; Lee, C.; Lewis, J. A.; Yeh, D.; Liu, Y.; Lee, H. W.; McDowell, M. T. Stress evolution during cycling of alloy-anode solid-state batteries. *Joule* **2021**, *5*, 2450–2465.
[35] Rao, M. Y.; Tang, H.; Wu, J. B.; Song, W. H.; Zhang, M.; Yin, W. B.; Zhuo, Y.; Kiani, F.; Chen, B.; Jiang, X. Q. et al. Thousands of conductance levels in memristors integrated on CMOS. *Nature* **2023**, *615*, 823–829.
[36] Wan, Z. N.; Mohammad, H.; Zhao, Y. Q.; Darling, R. B.; Anantram, M. P. Bipolar resistive switching characteristics of thermally evaporated V_2O_5 thin films. *IEEE Electron Device Lett.* **2018**, *39*, 1290–1293.
[37] Göhlert, T.; Siles, P. F.; Päßler, T.; Sommer, R.; Baunack, S.; Oswald, S.; Schmidt, O. G. Ultra-thin all-solid-state micro-supercapacitors with exceptional performance and device flexibility. *Nano Energy* **2017**, *33*, 387–392.
[38] Wang, Y. L.; Zhang, Y.; Wang, G. L.; Shi, X. W.; Qiao, Y. D.; Liu, J. M.; Liu, H. G.; Ganesh, A.; Li, L. Direct graphene-carbon nanotube composite ink writing all-solid-state flexible microsupercapacitors with high areal energy density. *Adv. Funct. Mater.* **2020**, *30*, 1907284.
[39] Chang, Y. K.; Sun, X. H.; Ma, M. D.; Mu, C. P.; Li, P. H.; Li, L.; Li, M. Z.; Nie, A. M.; Xiang, J. Y.; Zhao, Z. S. et al. Application of hard ceramic materials B_4C in energy storage: Design B_4C@C core-shell nanoparticles as electrodes for flexible all-solid-state micro-supercapacitors with ultrahigh cyclability. *Nano Energy* **2020**, *75*, 104947.
[40] Ma, C.; Rangasamy, E.; Liang, C. D.; Sakamoto, J.; More, K. L.; Chi, M. F. Excellent stability of a lithium-ion-conducting solid electrolyte upon reversible Li^+/H^+ exchange in aqueous solutions. *Angew. Chem., Int. Ed.* **2015**, *54*, 129–133.
[41] Park, S.; You, M. J.; Byeon, Y. S.; Song, C. H.; Oh, S. M.; Kim, J. H.; Park, M. S. Stabilizing the surface of Li_2NiO_2 cathode additive by coating amorphous niobium oxy-carbide for lithium-ion batteries. *Mater. Today Energy* **2023**, *36*, 101351.
[42] Gowda, S. R.; Brunet, A.; Wallraff, G. M.; McCloskey, B. D. Implications of CO_2 contamination in rechargeable nonaqueous Li-O_2 batteries. *J. Phys. Chem. Lett.* **2013**, *4*, 276–279.
[43] Huo, Y. J.; Lee, C. C. The growth and stress vs. strain characterization of the silver solid solution phase with indium. *J. Alloys Compd.* **2016**, *661*, 372–379.
[44] Ertorer, O.; Topping, T.; Li, Y.; Moss, W.; Lavernia, E. J. Enhanced tensile strength and high ductility in cryomilled commercially pure titanium. *Scr. Mater.* **2009**, *60*, 586–589.
[45] Sarkar, S.; Thangadurai, V. Critical current densities for high-performance all-solid-state Li-metal batteries: Fundamentals, mechanisms, interfaces, materials, and applications. *ACS Energy Lett.* **2022**, *7*, 1492–1527.
[46] Kim, K. M.; Zhang, J. M.; Graves, C.; Yang, J. J.; Choi, B. J.; Hwang, C. S.; Li, Z. Y.; Williams, R. S. Low-power, self-rectifying, and forming-free memristor with an asymmetric programing voltage for a high-density crossbar application. *Nano Lett.* **2016**, *16*, 6724–6732.
[47] Lee, S. H.; Cheong, S.; Cho, J. M.; Ghenzi, N.; Shin, D. H.; Jang, Y. H.; Han, J.; Park, T. W.; Kim, D. Y.; Shim, S. K. et al. In-materia annealing and combinatorial optimization based on vertical memristive array. *Adv. Mater*. **2024**, *36*, 2410191.
[48] Wan, Z. N.; Darling, R. B.; Majumdar, A.; Anantram, M. P. A forming-free bipolar resistive switching behavior based on ITO/V_2O_5/ITO structure. *Appl. Phys. Lett.* **2017**, *111*, 041601.
[49] Sacchetto, D.; Gaillardon, P. E.; Zervas, M.; Carrara, S.; De Micheli, G.; Leblebici, Y. Applications of multi-terminal memristive devices: A review. *IEEE Circuits Syst. Mag.* **2013**, *13*, 23–41.

This is an open access article under the terms of the Creative Commons Attribution 4.0 International License (CC BY 4.0, https://creativecommons.org/licenses/by/4.0/).

© The Author(s) 2025. Published by Tsinghua University Press.