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Temperature dependence of the electrical characteristics of ZnO thin film transistor with high-*k* NbLaO gate dielectric

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ABSTRACT

ZnO thin film transistor with high-*k* $NbLaO/SiO_2$ bilayer gate dielectric was fabricated by sputtering, and the temperature dependence of the electrical properties of the device was investigated in the temperature range of 293–353 K for clarifying thermally activated carrier generation and carrier transport mechanisms in the conducting channel. With the increase in the temperature, the transfer curve shifts toward the negative gate voltage direction with a negative shift of the threshold voltage, an increase in the off-state current and the subthreshold slope, and a significant increase in carrier mobility. The decrease in the threshold voltage is originated from the formation of oxygen vacancy and the release of free electrons in the ZnO channel, and the formation energy can be estimated to be approximately 0.3 eV. In both subthreshold and above-threshold regimes, the temperature dependence of the drain current shows Arrhenius-type dependence, and the activation energy is around 0.94 eV for a gate voltage of 2 V, reducing with the increase in the gate voltage. The temperature dependence of the ZnO film resistance also exhibits an Arrhenius-type behavior, indicating that the thermal activation conduction process is the dominant conduction mechanism in the ZnO film. Two types of thermal activation conduction processes are observed in the 303–373 K temperature range. This is explained in terms of the existence of two types of deep donors that are consecutively excited to the conduction band as the temperature increases.

I. INTRODUCTION

Zinc oxide (ZnO)-based thin film transistors (TFTs) have attracted much attention due to their advantages such as high field-effect mobilities, good uniformities, high transparencies in the visible light range, compatibility with the conventional a-Si TFT fabrication process, and the low-temperature deposition process for flexible electronics.[1–3] Over the past two decades, many efforts have been made to improve the device performance of oxide TFTs by optimizing the device structure,[4] using multicomponent ZnO-based oxides as an active layer,[5] and optimizing gate dielectric and its interface matching with the active channel layer[6] for next-generation active-matrix liquid-crystal displays (AMLCDs) and active-matrix organic light-emitting diode (AMOLED) displays. Recently, ZnO-based TFTs with ultralow-voltage operation have attracted special interest to make them particularly suitable for low-power applications such as portable and wearable electronics, flexible electronics, and integrated biosensors.[7,8] A widely accepted approach to decrease the operation voltage of TFTs is using high relative permittivity (high-*k*) gate dielectric (e.g., La_2O_3, ZrO_2, Nb_2O_5, and HfO_2) as well as decreasing the thickness of the gate dielectric film. Among them, Nb_2O_5 has a dielectric constant of over 40, which has great potential in reducing the threshold voltage of TFTs.[9] However, Nb_2O_5 film has high defect concentration, small bandgap, and high polarizability, which cause an increase in the gate leakage current. Fortunately, it has been reported that the incorporation of lanthanum in Nb_2O_5 can enlarge its bandgap, inhibit the generation of oxygen vacancy, and reduce the defect concentration at the interface.[10,11] As a result, NbLaO may be a promising alternative high-k material as the gate dielectric of ZnO-based TFTs.

On the other hand, it is of great importance to investigate the temperature dependence of the electrical characteristics of ZnO-based TFTs for understanding thermally activated free carrier generation and electrical transport mechanisms in the conducting channel and temperature reliability. So far, there are a few reports about the temperature characteristics of oxide TFTs.[12–14] Huang *et al.*[12] suggested that the dominant carrier transport mechanism is hopping between localized band-tail states in the low-temperature range but is multiple trapping and release in the high temperature range, which is based on the dependence of field-effect mobility and channel conductance on temperature and gate bias in the temperature range from 70 to 300 K. Heo *et al.*[13] proposed an equivalent circuit model of thermionic field emission for reverse bias and a thermionic emission mechanism for forward bias, which successfully describe the Arrhenius behavior of the drain current and the Mott variable-range hopping conduction mechanism in a low-temperature regime below 230 K. It should be noted that most of the studies on the temperature dependence of the electrical properties of oxide TFTs were mostly focused on the low-temperature regions (<300 K); however, the operating temperature of the TFT devices in real applications such as AMLCDs and AMOLED displays is normally higher than room temperature, even up to 350 K due to Joule heat. To date, the effects of temperature on the electrical characteristics of ZnO TFTs in the range from room temperature to extremely high temperature have been rarely reported. In this work, a NbLaO/SiO_2 bilayer thin film was utilized as gate dielectric to achieve low-voltage and high-performance ZnO-TFT. Furthermore, the temperature dependence of the electrical characteristics of the device was investigated at high ambient temperatures from 293 to 353 K to clarify thermally activated carrier generation and carrier transport mechanisms in the conducting channel and temperature reliability of electrical performance of the device.

II. EXPERIMENTAL SECTION

The bottom-gate top-contact configuration ZnO TFT with NbLaO/SiO_2 gate dielectric was fabricated on the indium tin oxide (ITO) coated glass substrate, where the ITO layer is used as a common gate electrode, NbLaO/SiO_2 as a bilayer gate dielectric, ZnO thin film as a channel layer, and Al thin film as source and drain electrodes, and the main processing steps are shown in Fig. 1. The ITO-coated glass substrates were cleaned by ultrasonic treatment in acetone, ethanol, and de-ionized water, successively. Next, an 8-nm SiO_2 layer acting as the buffer layer was deposited on the ITO layer by radio frequency (RF) sputtering (Discovery 635, Denton Vacuum) with a SiO_2 target in an Ar/O_2 (24/2 SCCM) gas mixture. During deposition, RF power and sputtering time were adjusted to be 50 W and 20 min, respectively. Then, the NbLaO film was deposited by the co-sputtering of the Nb metal target and La_2O_3 ceramic target in an Ar/O_2 (26/4 SCCM) mixed ambient. During this process, the direct current/RF power for the Nb/La_2O_3 targets was set as 0.02 A/45 W, and the sputtering time was set as 20 min. NbLaO/SiO_2 bilayer gate dielectric was utilized to effectively lower the threshold voltage and improve interface characteristics. After that, all the samples were annealed in N_2 (with a flow rate of 800 ml/min) at 300 °C for 30 min to improve the quality of the dielectric films.[15] Subsequently, a 77-nm ZnO

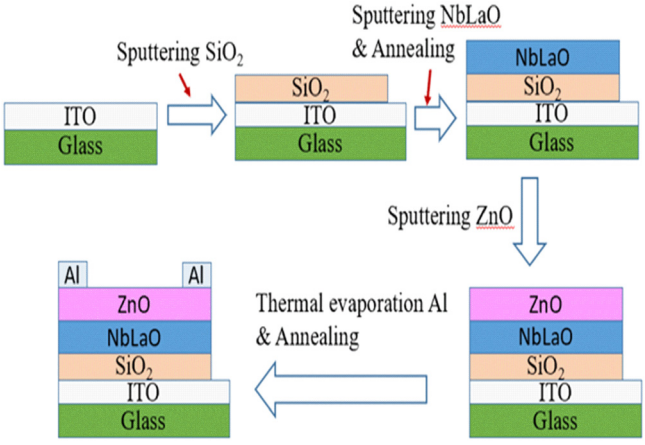

FIG. 1. Main processing steps of the ZnO-TFT with NbLaO/SiO_2 stacking gate dielectric.

channel layer was deposited on the gate dielectric at room temperature by RF sputtering with a power of 50 W and sputtering time of 50 min in an Ar/O_2 (24/1 SCCM) gas mixture. Next, Al is thermally evaporated onto the active region through a shadow mask to form source and drain contact electrodes. Finally, all the samples were annealed in N_2 (800 ml/min) at 200 °C for 30 min to reduce the contact resistance of the source/drain electrodes. The TFT has a channel length (L) of 100 μm and a channel width (W) of 350 μm. In particular, except the annealing processes, all the other processes were carried out at room temperature.

The physical thicknesses of all films were measured by the spectroscopic reflectometer (NanoCalc-2000, Ocean Optics). X-ray diffraction (XRD) measurement was performed at room temperature in air using the Cu Kα line (D8 ADVANCE, Bruker). The surface morphology of the ZnO film was analyzed by atomic force microscopy (AFM) (CPSM400S, Benyuan). The chemical composition of the NbLaO film was characterized by x-ray photoelectron spectroscopy (XPS) (Axis Ulatra DLD, Kratos). The electrical characteristics of the ZnO-TFTs and the ZnO film resistance at various temperatures were performed on cascade probe station with a *Temptronic* TP0315A temperature controller using a *Keithley* B1500A precision semiconductor parameter analyzer. To ensure the device is in the thermal equilibrium state at each fixed temperature to improve the accuracy of measurement, the I-V measurements were done after a hold time of 5 min at each fixed temperature.

III. RESULT AND DISCUSSION

The chemical composition of the NbLaO film is determined by XPS, and the Nb $3d_{5/2}$, La $3d_{5/2}$, and O 1s portions of the XPS signal are shown in Fig. 2, in which Gaussian fitting was made. According to the XPS results, the atomic ratio of Nb/(Nb + La) is calculated to be 18.5%. In Fig. 2(a), the peak position of the Nb $3d_{5/2}$ spectrum is located at 207.18 eV, which is lower than the value of the Nb $3d_{5/2}$ spectrum in the Nb_2O_5 film without La doping.[11] The lower binding energy is due to the suppression of

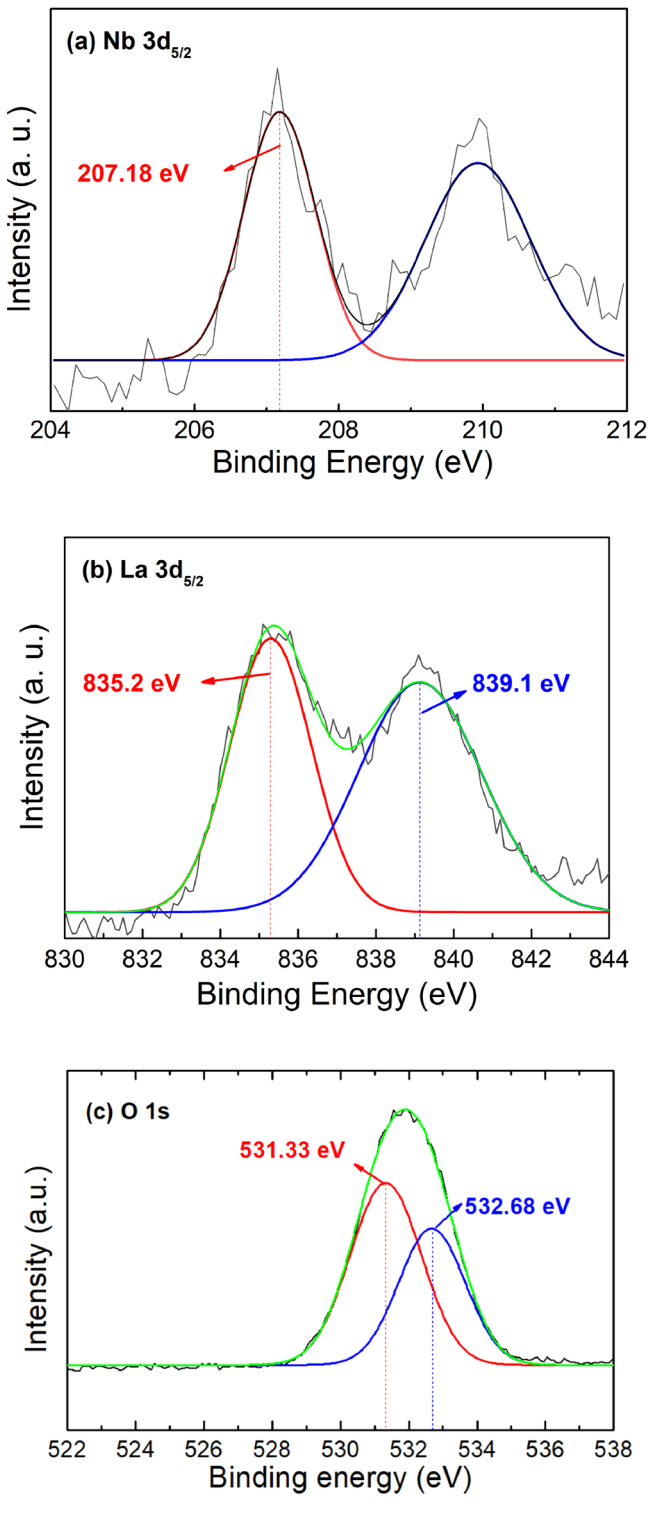

FIG. 2. XPS spectra of (a) Nb $3d_{5/2}$, (b) La $3d_{5/2}$, and (c) O 1s for the NbLaO film.

oxygen vacancy by the La incorporation. The oxygen vacancy is positively charged with an electric field generated, thus resulting in an increase in binding energy.[16] In Fig. 2(b), the La $3d_{5/2}$ peak is located at 835.2 eV, which is higher than the ideal La_2O_3 reference peak (at 834 eV).[16] The increase in binding energy is originated from the formation of La–OH bond due to the moisture absorption of La_2O_3 and the presence of La–O–Nb bond in NbLaO films.[11] The two O 1s peaks at 531.33 and 532.88 eV as shown in Fig. 2(c) should be originated from the La–OH bond and the Nb–OH bond,[17] respectively, while the two O1s peaks corresponding to La–O and Nb–O were not observed. A possible cause is the surface moisture absorption due to the absence of x-ray surface treatment of the sample.

Figure 3 shows the XRD pattern of the ZnO film. It can be seen from Fig. 3 that the ZnO film has a hexagonal wurtzite structure and a strong *c* axis orientation along the (002) plane. Besides the (002) peak, there are also other very small diffraction peaks corresponding to (100), (102), and (103) of ZnO. The crystallite size (D) of the ZnO film can be calculated to be 10.44 nm using Scherer's formula [$D = k\lambda/(\beta\cos\theta)$] from the full width at half maxima (FWHM) of the (002) peak, where λ is the wavelength of Cu ka radiation (1.5406 Å), k is the correlation factor (0.89), β is the FWHM of the (002) peak, and θ is Bragg's diffraction angle. The inset of Fig. 3 shows AFM surface morphology images ($1 \times 1\,\mu m^2$) of the ZnO film. It is observed that the grains are clearly visible, the surface shows numerous micropores, and the mean grain size can be estimated to be about 65 nm with a root mean square roughness of 2.1 nm.

Figure 4(a) shows the typical transfer characteristics of the ZnO TFT with the NbLaO/SiO_2 bilayer gate dielectric, which were measured at a drain voltage (V_{DS}) of 5 V for various temperatures, ranging from 293 to 353 K. With the increase in the temperature, the transfer curve shifts toward the negative gate voltage direction, and the on-state current and the off-state leakage current increase clearly. In order to further reveal the temperature dependence of electrical properties of the device, the main electrical parameters,

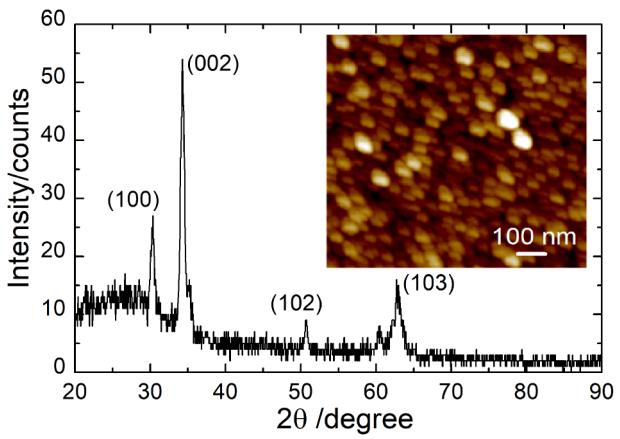

FIG. 3. XRD pattern of the ZnO film. Inset: AFM surface morphology image of the ZnO film.

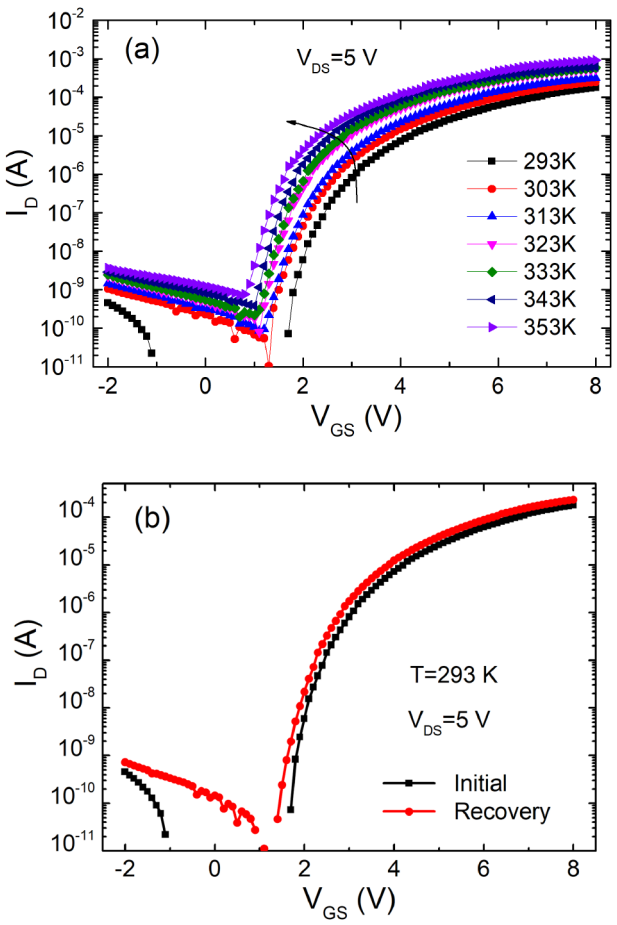

FIG. 4. Temperature-dependent transfer curves of the ZnO TFT. (a) for the temperature increased from room temperature (293 K) to 353 K, and (b) at room temperature (293 K) before and after the temperature-dependent measurement.

such as field-effect mobility (μ_{FE}), threshold voltage (V_{th}), off-state current (I_{off}), and sub-threshold swing (SS), extracted from the transfer curves at various temperatures are shown in Fig. 5. μ_{FE} and V_{th} were obtained by the equation $I_D = \mu_{FE} W C_{ox} (V_{GS} - V_{TH})^2/2L$, where W and L are the channel width and length, respectively, and C_{ox} is the gate insulator capacitance per unit area of 141 nF/cm^2 measured by a metal–insulator–semiconductor (MIS) structure for a testing frequency of 100 KHz. The device at room temperature exhibits high performance with a field-effect mobility of 32.46 cm^2 V^{-1} s^{-1}, a threshold voltage of 3.16 V, a sub-threshold swing of 110 mV/Dec, a current on/off ratio of 1.8×10^7, and a low operation gate voltage of less than 5 V.

Figure 4(b) shows the transfer characteristics of the ZnO TFT at room temperature (293 K) before and after the temperature-dependent measurement. Previous reports indicated that the temperature effect in the transfer characteristics of oxide TFT is reversible.[18,19] However, it should be noted that the transfer characteristics at room temperature (293 K) cannot be fully reproduced

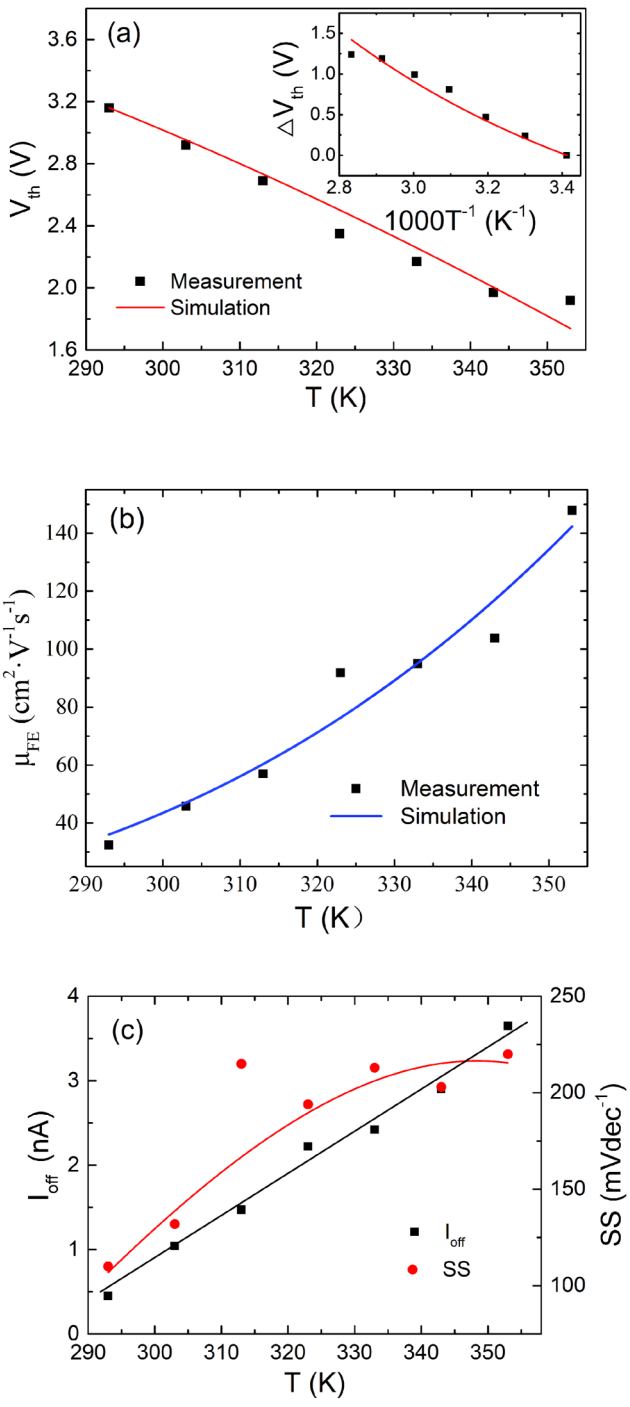

FIG. 5. Temperature dependence of electrical parameters of the ZnO-TFT. (a) $Vth \sim T$, the inset shows the experimental plot and the fitted curve for ΔV_{th} vs 1000/T in the temperature range between 293 and 353 K, (b) μ_{FE}-T curve, and (c) I_{off}-T curve at $V_{GS} = -2$ V and SS-T curve. Symbols represent experimental data, and solid lines represent linear (I_{off}) and polynomial (SS) approximate curves.

after the high temperature measurements, implying that the change in the transfer characteristics due to increasing temperature is not fully reversible. This can be explained that a few oxygen atoms leaving the lattice sites due to thermal excitation do not return to their original sites and still reside in the interstitial sites and thus causing oxygen vacancies to be higher than that before the temperature characteristic measurement. Therefore, a slight shift toward negative gate voltage is observed in the transfer characteristic curve compared to room temperature before the temperature-dependence measurement.

It can be clearly seen from Fig. 5(a) that V_{th} decreases from 3.16 to 1.92 V with the increase in temperature from 293 to 353 K, which is related to an increase in carrier concentration in the channel. In general, free electrons in oxide semiconductor materials are mainly induced by oxygen vacancies.[20] When the temperature increases, thermally excited oxygen atoms can leave their original sites and move into the interstitial sites, thus inducing vacancies (point defects) and releasing free electrons. Therefore, the lower threshold voltage observed at higher temperatures can be attributed to these free electrons generated along with the oxygen vacancies in the ZnO active layer.[19,21] Based on the assumption that an oxygen vacancy induces two free electrons and the density of point defects n is much lower than the densities of lattice and interstitial sites, n can be expressed as[19]

$$n = S_1 \cdot \exp\left(-\frac{E_P}{3k_B T}\right), \quad (1)$$

where S_1 denotes the constant related to the entropy for the formation of one vacancy and two free electrons, E_P is the defect formation energy of oxygen vacancy, and k_B is the Boltzmann constant.

Therefore, the V_{th} decrease (ΔV_{th}) in Fig. 5(a) can be described in terms of temperature and defect formation energy by

$$\Delta V_{th} \cdot C_{ox} = \Delta Q = 2qt_{ZnO}S_1 \cdot \left(\exp\left(-\frac{E_P}{3k_B T}\right) - \exp\left(-\frac{E_P}{3k_B T_0}\right)\right), \quad (2)$$

where T_0 stands for the room temperature (293 K), q the electric charge, and t_{ZnO} the thickness of the ZnO active layer. The inset of Fig. 5(a) shows the experimental plot of $\Delta V_{th} - 1000/T$, which is in good agreement with numerical simulation by using Eq. (2), indicating the validity of the model. The corresponding fitting parameters E_p and S_1 are 0.3 eV and 4.42×10^{18} cm^{-3}, respectively. Based on the obtained parameter values, the oxygen vacancy concentration in the ZnO active layer is calculated to be 8.45×10^{16} and 1.66×10^{17} cm^{-3} at the temperatures of 293 and 353 K, respectively. The estimated defect formation energy in the ZnO active layer is less than those of the typical oxide semiconductor reported in previous literature,[19,20,22] which should be related to low crystallinity and low density of the ZnO channel layer resulted from sputtering deposition at room temperature and annealing treatment at low temperature (300 °C) for 30 min.

In order to further understand the carrier transport mechanism in ZnO-TFT, the electron mobility as a function of temperature was extracted and plotted in Fig. 5(b). The carrier mobility always increases with increasing temperature, with an electron mobility of 32.46 cm^2 V^{-1} s^{-1} at room temperature (293 K) and 147.85 cm^2 V^{-1} s^{-1} at the temperature of 353 K, indicating that the carrier transport process within the ZnO-TFT is not governed by band conduction or percolation in the conduction band[22] but by thermal-activation-type conduction. At higher temperatures, more electrons can escape from localized states and contribute to the free carrier, which causes an increase in μ_{FE} and a decrease in V_{th}.

Temperature dependence of off-state current (I_{off}) and SS of the device is shown in Fig. 5(c). The relatively high off-state current could be due to the large area of the source/drain electrodes that overlap with the gate electrode (not patterned). The increase in I_{off} with increasing temperature should be attributed to the increases in the gate-leakage current and defects in the ZnO active layer. As already mentioned above, defects induced by thermal activation increase with increasing the temperature, thereby causing an increase of generation-recombination current in the depletion region, in which the transistor is in off-state operation (VGS = −2 V). On the other hand, the gate-leakage current seems to be thermally activated and increases with increasing temperature. This behavior might be related to the properties of the gate dielectric layer. The increase in SS with increasing temperature should be attributed to the increases in defects induced by thermal activation in the bulk of the ZnO active layer and gate dielectric and at the interface between gate dielectric and the channel layer.

Based on the above mentioned, the carrier transport process in the ZnO-TFT is governed by thermal-activation-type conduction. To further study the conduction mechanism present in the ZnO-TFT, the corresponding temperature dependence of the drain current (I_{DS}) versus 1000/T in the above-threshold region was obtained for different gate voltages varying from 2 to 6 V and a fixed V_{DS} of 5 V as shown in Fig. 6. Clearly, the log (I_{DS}) −1000/T plots exhibit a good linear dependency, indicating that the thermally activated carrier transport process is followed by Arrhenius-type temperature dependence. Based on the Arrhenius model, the drain current can be expressed with the following

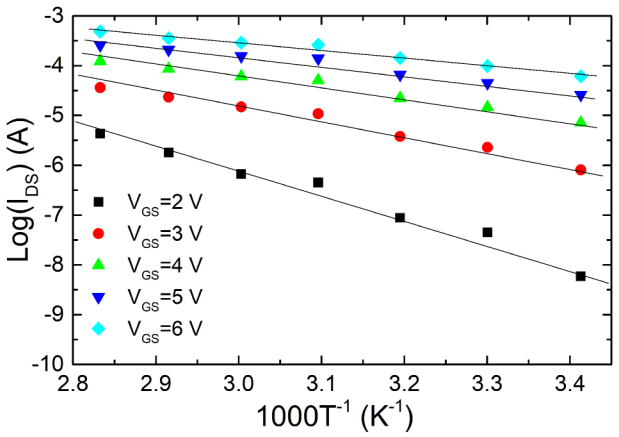

FIG. 6. Temperature dependence of I_{DS} vs 1000/T for different V_{GS} in both subthreshold and above-threshold regimes.

equation:[23,24]

$$I_{DS} = I_{DS0} \cdot \exp\left(-\frac{E_a}{k_B T}\right), \quad (3)$$

where I_{DS0} is a prefactor, E_a is the activation energy, and k_B is the Boltzmann constant. If the predominant conduction mechanism is hopping, E_a describes the energy required to release an electron from the localized states and is equal to the difference in energy between the minimum of the conduction band E_C and the Fermi level E_F. As shown in Fig. 4(a), the sub-threshold current and above-threshold current have strong temperature dependence implying high activation energy. The dependence of E_a extracted from Fig. 6 on the gate voltage is plotted in Fig. 7. E_a decreases monotonically with the increase in the gate voltage, which is 0.94 and 0.3 eV for $V_{GS} = 2$ V and $V_{GS} = 6$ V, respectively. It is well known for the MIS structure that the gate voltage determines the energy band structure of the semiconductor surface. Figures 7(b) and 7(c) show the schematic energy band diagram illustrating the suggested carrier transport mechanisms for $V_{GS} = V_{GS1}$ and $V_{GS} = V_{GS2}$ ($V_{GS1} < V_{GS2}$). For oxide semiconductor TFTs, most of the induced charges in the channel are captured by localized states with a small fraction going into the conduction band, which have contributed to the drain current. With increasing gate voltage (e.g., $V_{GS} = V_{GS2}$), the Fermi level E_F moves closer to the edge of the conduction-band until it reaches the tail states, and thus, the extracted E_a decreases. The density of the tail states is so high that the Fermi level is pinned in the tail states,[25] thereby causing the reduced slope of the E_a versus gate voltage curve in Fig. 7(a). In addition, it is worth mentioning that the E_a values for various V_{GS} are close to those of the amorphous silicon TFTs, but significantly higher than those obtained in oxide semiconductor TFTs.[19] The result may originate from the high density of states in the bulk of ZnO and at ZnO/NbLaO interface due to low crystallinity and low density of the ZnO channel layer deposited at room temperature and low-temperature (300 °C) annealing.

To escape the effect of the gate voltage on carrier transport in the ZnO film, the gate electrode is open, where the ZnO film is regarded as a resistance and the external voltage was applied between the source and drain electrodes. The measurement on the temperature dependence of the resistance can provide very useful information about the carrier transport mechanism and the associated impurity levels and their energy distribution in the semiconductor material. The current-voltage (I-V) characteristics were measured at various fixed temperatures between 303 and 373 K, as shown in Fig. 8(a). It can be noted that the current increases significantly with the increase in temperature under same applied voltage, and the I-V characteristics are nonlinear for a fixed temperature. This can be explained as follows: It can be manifested based on the XRD pattern in Fig. 3 that the ZnO film is polycrystalline with a hexagonal wurtzite structure. As the temperature increases, the carrier at the donor level in the grain is thermally excited to the conduction band and its mobility is improved, thus enhancing the grain conductivity. On the other hand, the oxygen diffuses into the grain boundary to form the acceptor surface state during radio frequency sputtering of the ZnO film, thus forming the Schottky barrier with a certain barrier height

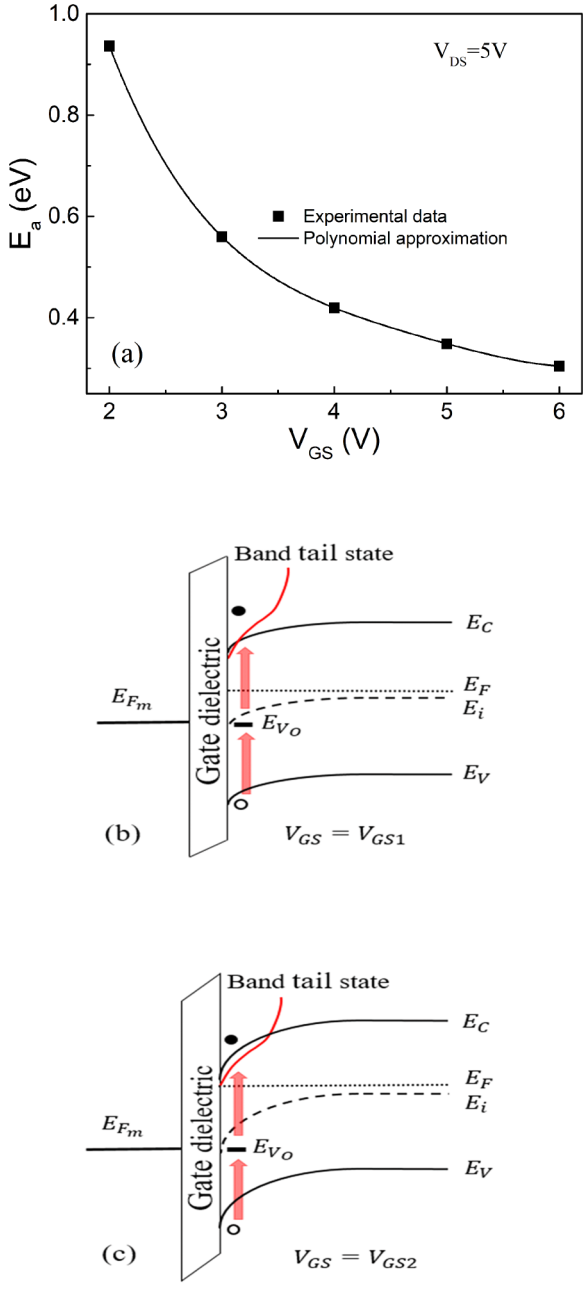

FIG. 7. (a) Dependence of the activation energy (E_a) on the V_{GS} for I_D in the above-threshold region for the ZnO-TFT; (b) and (c) they show the schematic energy band diagram illustrating the suggested carrier transport mechanisms for $V_{GS} = V_{GS1}$ and $V_{GS} = V_{GS2}$ ($V_{GS1} < V_{GS2}$).

which is the cause of appearance of the nonlinear I-V characteristics. As the temperature increases, the ability of thermally activated carriers to cross the Schottky barrier increases and the grain boundary resistivity decreases, so resulting in an increase in the current. Taking

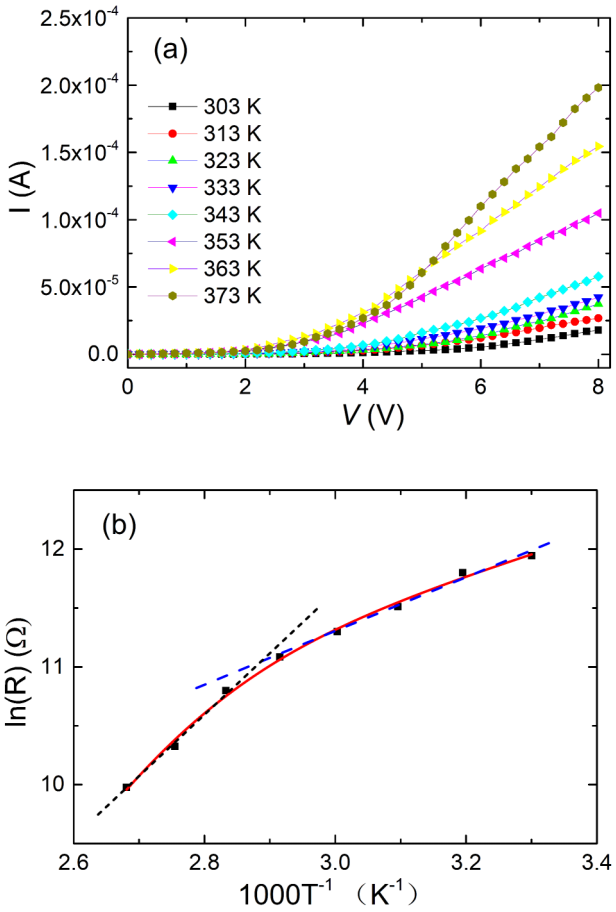

FIG. 8. (a) Current-voltage curves of the ZnO thin-film resistance at different temperatures. (b) The logarithm of the resistance as a function of the reciprocal of temperature. The symbols are experimental data and the solid curve is a least-squares fit to Eq. (4).

the nonlinear I-V curves into account, the resistance at a given temperature was determined from the linear regime around the bias voltage of 7 V in Fig. 8(a). Figure 8(b) shows the variation in the logarithm of the ZnO film resistance with reciprocal temperature between 303 and 373 K. Two distinct slopes can be clearly seen in the two different temperature regimes of ~303–343 K (straight dashed line) and ~353–373 K (straight dotted line), respectively, indicating that the charge transport is obeyed by Arrhenius-type behavior. The experimental data (square symbols) can be quantitatively described by the following equation:[26]

$$\frac{1}{R} = \frac{1}{R_1} e^{-\frac{E_1}{k_B T}} + \frac{1}{R_2} e^{-\frac{E_2}{k_B T}}, \quad (4)$$

where R_1 and R_2 are temperature insensitive resistance prefactors, and E_1 and E_2 are the relevant activation energies associated with the two kinds of thermal activation conduction processes. The fitted results by using Eq. (4) is plotted as the solid curve in Fig. 8(b), indicating that Eq. (4) can well describe the experimental result, where the fitted parameters of E_1 and E_2 are 0.79 and 0.15 eV, respectively. This observation illustrates that there exist two types of deep donors with an activation energy of $E_1 \approx 0.79$ eV and of $E_2 \approx 0.15$ eV in the ZnO film. For the temperature region below ~345 K, the deep donors at 0.15 eV can be easily excited to the conduction band, and thus, the temperature dependence of the resistance is largely determined by the number of the deep donors being excited to the conduction band. For the temperature region above ~345 K, two types of deep donors can be excited to the conduction band and are responsible for the electrical transport behavior. However, the temperature dependence of the resistance is mainly governed by the number of deep donors at 0.79 eV that are being excited to the conduction band.

IV. CONCLUSIONS

The temperature-dependent electrical properties of ZnO TFT with NbLaO/SiO_2 as gate dielectric are investigated in the temperature range of 293–353 K to clarify thermally activated carrier generation and carrier transport mechanisms in the conducting channel. With the increase in the temperature, the drain current dramatically increases in all operation regions with a significant increase in the carrier mobility from 32.46 to 147.85 $cm^2 V^{-1} s^{-1}$ and a decrease in the threshold voltage from 3.16 to 1.92 V. The decrease in the threshold voltage is originated from the formation of oxygen vacancy and the release of free electrons in the ZnO channel. In both subthreshold and above-threshold regimes, the temperature dependence of the drain current shows Arrhenius-type dependence. The temperature dependence of the ZnO film resistance is also well described by the thermally activated electrons. The thermally activated Arrhenius model proposes that the activated electrons are released from two types of deep donors with different activation energies into the conduction band and may result in the increase in the current.

ACKNOWLEDGMENTS

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]S. Vyas, Johns Matthey Technol. Rev. **64**, 202 (2020).
[2]K. Kandpal and N. Gupta, Microelectron. Int. **35**, 52 (2018).
[3]M. F. Wang, X. F. Li, X. Xiong, J. Song, C. R. Gu, D. Zhan, Q. L. Hu, S. M. Li, and Y. Q. Wu, IEEE Electron Device Lett. **40**, 419 (2019).
[4]E. J. Park, H. M. Lee, Y. S. Kim, H. J. Jeong, J. Park, and J. S. Park, IEEE Electron Device Lett. **41**, 401 (2020).
[5]R. N. Bukke, J. K. Saha, N. N. Mude, Y. Kim, S. Lee, and J. Jang, ACS Appl. Mater. Interfaces **12**, 35164 (2020).

[6]J. M. Lee, B. H. Choi, M. J. Ji, J. H. Park, J. H. Kwon, and B. K. Ju, Semicond. Sci. Technol. **24**, 055008 (2009).
[7]J. Jung, S. J. Kim, T. S. Jung, J. Na, D. H. Yoon, M. M. Sabri, and H. J. Kim, IEEE Trans. Electron Devices **64**, 515 (2017).
[8]G. Cantarella, J. Costa, T. Meister, K. Ishida, C. Carta, F. Ellinger, P. Lugli, N. Munzenrieder, and L. Petti, Flex. Print. Electron. **5**, 033001 (2020).
[9]S. J. Kim, B. J. Cho, M. Bin Yu, M. F. Li, Y. Z. Xiong, C. X. Zhu, A. Chin, and D. L. Kwong, IEEE Electron Device Lett. **26**, 625 (2005).
[10]L. N. Liu, W. M. Tang, and P. T. Lai, Coatings **9**, 217 (2019).
[11]J. Q. Song, C. Y. Han, and P. T. Lai, IEEE Trans. Electron Devices **63**, 1928 (2016).
[12]X. M. Huang, C. F. Wu, H. Lu, F. F. Ren, D. J. Chen, R. Jiang, R. Zhang, Y. D. Zheng, and Q. Y. Xu, Solid-State Electron. **86**, 41 (2013).
[13]K. Heo *et al.*, IEEE Trans. Electron Devices **64**, 3183 (2017).
[14]C. C. Hsu, C. H. Chou, W. C. Jhang, and P. T. Chen, Physica B **569**, 80 (2019).
[15]Y. R. Liu and Y. X. Xiang, J. Vac. Sci. Technol. B **37**, 062202 (2019).
[16]P. S. Bagus, F. Illas, G. Pacchioni, and F. Parmigiani, J. Electron Spectrosc. Relat. Phenom. **100**, 215 (1999).
[17]J. Bhattarai, E. Akiyama, H. Habazaki, A. Kawashima, K. Asami, and K. Hashimoto, Corros. Sci. **40**, 19 (1998).
[18]G. W. Chang, T. C. Chang, J. C. Jhu, T. M. Tsai, Y. E. Syu, K. C. Chang, Y. H. Tai, F. Y. Jian, and Y. C. Hung, Appl. Phys. Lett. **100**, 182103 (2012).
[19]K. Takechi, M. Nakata, T. Eguchi, H. Yamaguchi, and S. Kaneko, Jpn. J. Appl. Phys. **48**, 011301 (2009).
[20]P. Bonasewicz, W. Hirschwald, and G. Neuman, Phys. Status Solidi A **97**, 593 (1986).
[21]V. Gavryushin, G. Raciukaitis, D. Juodzbalis, A. Kazlauskas, and V. Kubertavicius, J. Cryst. Growth **138**, 924 (1994).
[22]P. Kofstad, J. Phys. Chem. Solids **23**, 1571 (1962).
[23]S. C. Kim, Y. S. Kim, and J. Kanicki, Jpn. J. Appl. Phys. **54**, 051101 (2015).
[24]C. Chen, K. Abe, H. Kumomi, and J. Kanicki, IEEE Trans. Electron Devices **56**, 1177 (2009).
[25]Y. S. Lee, S. K. Fan, C. W. Chen, T. W. Yen, and H. C. Lin, *2013 International Conference on Advanced Infocomm Technology (ICAIT)*, Hsinchu, Taiwan, July 6–9, 2013 (IEEE, New York, 2013).
[26]C. C. Lien, C. Y. Wu, Z. Q. Li, and J. J. Lin, J. Appl. Phys. **110**, 063706 (2011).