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**A transfer method for high-mobility, bias-stable, and flexible organic field-effect transistors**

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## Introduction

The crystallinity of organic semiconductor (OSC) dominates the electrical performance of OSC-based devices such as organic field-effect transistors (OFETs),[1] organic light-emitting diodes (OLEDs),[2] and organic photovoltaics (OPVs).[3] OFET devices with highly crystalized active layers, especially for small molecule-based OSC layers, can benefit from the higher field-effect mobility, and smaller subthreshold swing.[1, 4-9] In general, the substrate conditions and growth process determine the

crystallinity of the OSC to a large extent.[10, 11] Owing to a smooth surface, strong dielectric strength, and high compatibility with simple pre-treatment process, Si/$SiO_2$ wafers have been widely employed as the substrates for the OSC materials, and a number of them have exhibited reliable mobility of 10 $cm^2V^{-1}s^{-1}$ or higher.[9, 11-17] The surface of Si/$SiO_2$ can be chemically modified with silane-based self-assemble monolayers (SAMs) to show different surface properties. For example, low-surface-energy alkylated SAMs such as octyltrichlorosilane (OTS) and octadecyltrichlorosilane (ODTS) are widely used for the thermal sublimation of OSC thin films, where elevated substrate temperature is usually required to facilitate better packing of molecules and thus higher field-effect mobility.[18-20] For the OSC materials with large conjugated systems, the appropriate substrate temperature during sublimation may be as high as 200-300 $^{o}$C.[20, 21] On the other hand, high-surface-energy phenylated SAMs such as phenyltrhichlorosilane (PTS) and 2-(phenylhexyl)trimethoxysilane (PHTS) are usually employed to modify the $SiO_2$ surface for the solution-processing of OSC crystals.[13, 22, 23] In these solution-processed OFETs, as the Si/$SiO_2$ is inert to most organic solvents, it is an excellent candidate to examine different fabrication parameters such as solute concentration, spin coating speed, shearing speed and others. Other than the crystallinity of the OSC films, the dielectric material on the substrate would also affect the operation stability, as the performances of the OFETs are very sensitive to the quality of the dielectric/semiconductor interfaces.[24-27] Firstly, the dielectric surface may contain defects which would become the carrier traps for in the channel. Secondly, not all the dielectric materials and substrates (such as the polymer one) support high temperature processing of OSC to achieve better crystallinity. Moreover, the selection of the dielectric surface and substrates, especially for the solution-processing of OSC crystals, is also restricted by the requirements of high surface energy, smooth surface

roughness, and chemical inertness to organic solvents. To date, there has been no single dielectric and substrate couple which can fulfill all different demands such as low-voltage operation, high crystallinity of OSC, bias stress stability, and mechanical flexibility. As a result, we need to compromise among different performance indicators, which inevitably restrict the development and applications of OFETs.

Herein, we address this limitation by reporting a transfer method for the organic semiconductor active layers, which separates the crystal growth and the rest fabrication steps of OFETs. The compatibility of this transfer method with the large area processing and photolithography allows it to be utilized in the mass production of OFETs and it is an important corner stone towards the commercialization of OFETs. We firstly obtained the crystallized organic thin films on specific SAM treated Si/$SiO_2$ substrates by both vacuum sublimation and solution shearing approaches. We then transferred the active layers to other substrate/dielectric surfaces for the better electrical performances like low-voltage operation, near-zero turn-on voltage, small hysteresis, and high bias-stress stability. The vacuum sublimation transferred devices, showed only < 2% drain current decay after 20,000 s of continuous bias. For the solution shearing transferred devices, a remarkable improvement in the bias stability (77% vs 27% drain current drop) and operating voltage (80 V vs 4 V) can also be observed by transferring the highly crystallized $C_{10}$-DNTT from PTS treated Si/$SiO_2$ to OPDA treated Al/$AlO_x$. These highly crystallized $C_{10}$-DNTT OFETs can also operate under significant bending (bending radius = 215 μm). In addition, we further applied photolithography on the organic semiconductor layers within the single crystal domains to build high-performance, low-voltage, and ultra-flexible OFET 4 × 4 arrays. The presented transfer method here can not only broaden our choice of high-mobility OSC, dielectric materials

and substrates, but also offers new alternatives to tailor-made high-performance OFET-based devices and circuits for specific applications.

**Results and discussion**

The schematic illustrations and experimental processes of the transfer method are shown in **Figure 1** and **Movie S1, S2**. In the transfer method, the 2,9 dioctyldinaphtho[2,3-b:2 ',3 '-f]thieno[3,2-b]thiophene ($C_{10}$-DNTT) films were grown on Si/$SiO_2$ substrates by either vacuum sublimation or solution shearing (Figure 1a). A protective layer (OSCoR SL1, Orthogonal) was first spin coated on top of the $C_{10}$-DNTT films (Figure 1a). The protective layer is orthogonal to aqueous and common organic solvents and will not dissolve the $C_{10}$-DNTT films. Next, the $C_{10}$-DNTT film with the sacrificial layer were lifted off together by hydrofluoric acid (HF) and DI water (the hydrophobicity of the layers allowed the film to flow on the liquid surface), as shown in Figure 1c. After diluting with the deionized water (Figure 1d and e), the film was transferred to an isopropanol container in which a target substrate was used to host the free-standing film (Figure 1f). The volatility (boiling point:82.6$^{o}$C) of isopropanol made it easy to be removed via evaporation in ambient conditions, so that the film became firmly attached to the target surface (Figure 1g and h). The protective layer was finally dissolved, thereby only leaving the OSC films on the target substrate (Figure 1i). The transferred OSC films were annealed in a vacuum oven at 80 $^{o}$C for 12 h to remove solvent residuals.

The vacuum sublimated $C_{10}$-DNTT thin films were first employed to evaluate the effectiveness of transfer process. From the X-ray photoelectron spectroscopy (XPS) measurements of the transferred thin films in **Figure 2b** and c, the carbon 1s and sulfur 2p peaks are observed as the indicators of the $C_{10}$-DNTT molecules. On the other hand,

the negligible signal from silicon 1s orbitals suggests that neither the ODTS molecules nor the Si atoms in $SiO_2$ were transferred to the target substrate. As shown in Figure 2a, the Si-O bonds at the ODTS/$SiO_2$ interface as well as inside $SiO_2$ will be opened by the HF. In this way, the $C_{10}$-DNTT thin film can be dissociated. We then examined the upper surface of the transferred film by the Fourier transform infrared (FT-IR) spectroscopy. The missing of the strong hydroxyl group peaks from 3100 to 3300 $cm^{-1}$ after the transfer and dissolving of the protective layer (blue curve in Figure 2d) implies that the surface of the $C_{10}$-DNTT thin film is clean for OFET applications.

We utilized Grazing-incident wide angle X-ray scattering (GIWAXS) to study the possible crystallinity change before and after the transfer. The GIWAXS result of 30-nm-thick vacuum sublimated $C_{10}$-DNTT thin films on ODTS-treated Si/$SiO_2$ is shown in **Figure 3a**. Majority of the $C_{10}$-DNTT molecules follow the layer-by-layer growth mode, with the long axis standing vertical to the substrate plane. The in-plane (020) peak is located at $Q_{xy}$ = 16.0 $nm^{-1}$. Yet a small number of molecules exhibit a polycrystalline nature without preferred orientation, corresponding to the diffraction ring starting at $Q_{xy}$ = 15.0 $nm^{-1}$. For the as-grown thin film, Au source and drain electrodes were thermal evaporated to form a bottom-gate top-contact OFET structure. Representative transfer curves based on the as-grown thin films are presented in Figure 3b. The devices show a peak mobility of 8.05 $cm^2V^{-1}s^{-1}$ ($\sigma$ = 0.17 $cm^2V^{-1}s^{-1}$), a hysteresis window of 1.34 V ($\sigma$ = 0.09 V), and a subthreshold swing of 0.91 V/decade ($\sigma$ = 0.08 V/decade). We further conducted the bias-stress test for a device with the highest mobility. By continuously applying $V_{DS}$ = -60 V and $V_G$ = -60 V for 20,000 s, the drain current decreased by 35% from its original value (Figure 3c). The 30-nm-thick $C_{10}$-DNTT film transferred from the as-grown ODTS-treated Si/$SiO_2$ substrate to another ODTS-treated Si/$SiO_2$ substrate (i.e. the same dielectric layer). The almost

identical electrical performance (Figure S2) indicates the transfer process did not degrade the OSC film.

The as-grown $C_{10}$-DNTT thin films were transferred to SAM-treated $AlO_x$/Al surfaces for the low-voltage OFETs. We herein selected three different SAMs, namely Octadecylphosphonic acid (ODPA), Phenylphosphonic acid (PhPA), and 1H,1H,2H,2H-Perfluorooctanephosphonic acid (FOPA) to study their effects on the transferred thin films. From Figure S1, the PhPA-treated surface has the largest surface energy (44.7 mN/m), the ODPA-treated surface has moderate surface energy (25.9 mN/m), while the FOPA-treated surface shows the lowest surface energy (16.2 mN/m). From the GIWAXS results of the transfer films in Figure 3d, g, and j, the major out-of-plane diffraction peaks were clearly observable, which means the layer-by-layer packing mode of the molecules remained the same. But the in-plane diffraction peaks became narrower than the as-grown films (Figure 3a), showing a more regular packing and less fluctuations on the lattice parameters. The extra ring for the random polycrystalline structure disappears after the transfer process. We believed the rings are caused by some randomly oriented or physiosorbed molecules on the as-grown films, which were cleaned during the transfer process. More importantly, the $Q_{xy}$ values of the (11L) and (020) peaks shifted to from 13.3 and 16.0 $nm^{-1}$ (before transfer, as shown in Figure S3) to 13.5 and 16.3 $nm^{-1}$ (after transfer). It indicated these two d-spacing values are shortened by 1.5% and 1.9%, respectively. Since the pristine films were deposited at high temperature (80 $^{o}$C) and cool down to room temperature (25 $^{o}$C), the mismatch in the coefficients of thermal expansion (CTE) between the organic semiconductor materials and the $SiO_2$ substrates would induce certain amount of tensile strain, which was stored in the OSC films.[28] When the films were detached from the as-grown substrates, the tensile strain could be released and in-plane distance between

molecules became shorter. The representative transfer curves of the three cases were plotted in Figure 3e, h, and k, with the statistical electrical performance summarized in Table S1. The field-effect mobility of the three transferred thin films on different SAMs were similar, while the on-set voltage became different. The fluorinated SAM (FOPA) gave a near-zero on-set voltage, and the phenylated (PhPA) one gave the most negative on-set voltage. It clearly suggests the fluorinated SAM provides an interface with lowest trap density and the channel can be turned-on with a relatively smaller gate bias. The bias-stress tests encores with the transfer measurements. The FOPA-based device shows the best bias-stability, with < 2% drain current change during the 20,000s continuous bias. The ODPA-based device shows the second-best stability with 6% current decay at the same bias condition, while the PhPA-based device has the worst stability (19% current decay). From the comparison among three different SAMs, the fluorinated-SAM is the best in terms of suppressing interface trap states, which is beneficial for near-zero on-set voltage, small hysteresis window, and bias-stress stability of the OFETs. However, when the $C_{10}$-DNTT was directly sublimated on the three SAM-treated $AlO_x$/Al substrates, the FOPA-based device shows much lower current than the ODPA and PhPA-based devices (Figure S4). It is presumably due to the very low surface energy (16.2 mN/m) restricted the crystallization of the thin film during vacuum sublimation. Due to the poor quality, the as-grown $C_{10}$-DNTT on FOPA-surface shows the lowest mobility. While at the same time bias-stability of the poorly grown $C_{10}$-DNTT is also the weakest among the three SAMs (Figure S4d). This observation suggests that although FOPA-treated $AlO_x$ can offer the lowest trap density, the poor quality of the as-grown $C_{10}$-DNTT film would also lead to unsatisfactory bias-stability. It suggests one specific SAM-treated dielectric surface maybe difficult to satisfy the two important requirements, (i) suitable for the growth of highly crystallized

thin film, (ii) low density of trap states at dielectric/semiconductor interface, at the same time. With the transfer method presented in this work, the highly crystallized OSC films can be first grown on substrates with suitable surface energy, and then transferred onto another substrate with a low density of trap states. By modifying dielectric-semiconductor interface, this transfer approach can enhance the bias stability of the OFET, while at same time without sacrificing the field-effect mobility of the OSC films.

The transfer method is also compatible with the solution-processed OSC materials although the substrate and dielectric treatment will be different from the vacuum sublimated OFETs. Solution-processing methods have been proved to deposit OSC films with large single crystals domain and high mobility in the range of 5-15 $cm^2V^{-1}s^{-1}$.[5, 11-14, 29-31] For example, in the solution shearing method, the solution must wet well on the dielectric in order to form a stable solid-liquid-air contact line. The small contact angle between the solution and the dielectric is crucial to evaporate the solvent and initiate the nucleation due to supersaturation.[32, 33] The substrate temperature and shearing speed need to be carefully controlled to facilitate the growth of large single-crystalline domains.[12, 13] Herein, the high-surface-energy PTS SAM was employed to treat the $SiO_2$ surface (contact angle and surface energy summarized in Figure S1), so that large single crystals (millimeter-scale size) of $C_{10}$-DNTT can be grown (**Figure 4a** and b). The out-of-plane (inset of Figure 4a) and in-plane (inset of Figure 4b) X-ray diffraction results indicate a good crystallinity of the crystals. However, as observed from Figure 3, although the high surface energy can improve wettability, the SAM with phenyl tail-group is not be the best for the stable operation of OFETs. The electrical performance of the OFET device fabricated on the as-grown PTS/$SiO_2$ substrate is shown in Figure 4c and d. Although it shows a peak mobility of c.a. 10 $cm^2V^{-1}s^{-1}$ (statistical data summarized in Table S1) and a large on/off ratio > $10^8$, the hysteresis

window is relatively large, and the drain current decreased by 77% after 20,000 continuous bias (Figure 4d). To address this issue, we applied our proposed method to transfer the as-grown $C_{10}$-DNTT crystals from PTS/$SiO_2$ to ODPA/$AlO_x$ (Movie S1) and the completed device structure is shown in Figure 4e. The channel area defined by the source and drain electrodes is within a single crystal domain, as shown in Figure 4f and g. In Figure 4h and i, the OFET shows text-book-like transfer and output curves based on the transferred crystals, thanks to the combination of single-crystallinity and the low density of trap states at the dielectric/semiconductor interface. The averaged mobility is up to 11.6 $cm^2V^{-1}s^{-1}$ and the hysteresis is negligible at only 12.4 mV within the 4 V operating voltage (statistical data is summarized in Table S1). The mobility plot against $V_{GS}$ is shown in Figure S5, indicating the mobility extracting is reliable. The same device exhibited higher mobility at low testing temperature (Figure S6), which is a sign of band-like transport and reveals the good crystallinity of the semiconductor. At the same time, the bias stability of the device is improved from 77% drain current drop (Figure 4d) to 27% decrease (Figure 4j) after the 20,000 s continuous bias. Similarly, the shift in threshold voltage after the bias-stress test is only 260 mV, as compared to the 5 V shift of the device on the PTS/$SiO_2$ substrate (Figure S7). The transfer method combines the solution-processed OSC crystals with low-surface-energy and low-trap-density dielectric for the first time. The devices thus show outstanding and comprehensive performance among the reported low-voltage OFETs, as summarized in Table S2.

Apart from transferring the high-mobility crystals onto low-surface-energy substrate, the transfer method could also facilitate the application of flexible substrates in high-performance OFETs. Due to the difficulties in handling, low glass transition temperature, weak resistivity to solvent, etc., utilization of flexible substrates in the

solution-growth of high-mobility organic semiconductor crystals has been problematic. Such limitations could be addressed by the presented transfer method, as the target substrate (after the detachment of SL + OSC and washing steps) is only in touch of isopropanol at room temperature. We have thus used the Cytop/polyacrylonitrile double layer (detailed fabrication steps please see Figure S8 and Methods) as the substrate for ODPA/$AlO_x$/Al, and perform the transfer of $C_{10}$-DNTT crystals (Figure S9). Relatively large-area of crystals could be entirely transferred, and 30 device were fabricated to study the yield rate and distribution in mobility (Figure S9d). The average saturation mobility is 7.3 $cm^2V^{-1}s^{-1}$, with a standard deviation (σ) of 1.7 $cm^2V^{-1}s^{-1}$. The bias-stress stability test is conducted in ambient air, with a current increase of ~10% after 20,000 s continuous bias (Figure S10). The different trend in bias-stress current change is due to the existence of the Cytop encapsulation layer. [25] Herein, two trapping interfaces have a combined effect on the drain current, which could be divided into three regimes (Figure S10). The ultra-flexible device could then be detached by water and become freestanding. (Figure S9c). The mobility histogram (Figure S9e) of the freestanding ultra-flexible devices remains almost identical to Figure S9d (mean: 7.2 $cm^2V^{-1}s^{-1}$, σ: 1.7 $cm^2V^{-1}s^{-1}$), which means the mechanical manipulation did little effect on the performance of the ultra-flexible devices.

With the success in ultra-flexible devices, we further demonstrate the utilization of single crystals as the active layer materials for OFET circuits. High-performance circuits requires the OFETs to have high field-effect mobility, low-voltage operation, good bias-stress stability, and small device-to-device variation. The single crystal domains of OSC could fulfill the requirements, as they provide excellent homogeneity from the nanometer scale to the millimeter scale. Figure 6a, b, and c show a $4 \times 4$ OFET array fabricated on ultra-flexible substrates based on Cytop/polyacrylonitrile double

layer (detailed fabrication steps please see Figure S6). The active layers in all the 16 pixels were patterned from a single crystal domain of $C_{10}$-DNTT (as confirmed by the cross-polarized optical microcopy in Figure S8), hence the pixel-to-pixel deviation can be minimized. A thin layer (4 nm thick) of n-type dopant (2,3,5,6-tetrafluoro-tetracyanoquinodimethane, F4-TCNQ) was inserted between the Au electrodes and the semiconductor to further improve the charge injection. 16 devices show uniform transfer characteristics with small hysteresis (Figure 6d). Even after the multiple photolithography and etching processes, the average mobility of the array device maintained at 5.1 $cm^2V^{-1}s^{-1}$ with a standard deviation of only 0.7 $cm^2V^{-1}s^{-1}$ (Figure 6e). At the same time, the single-crystallinity ensured the narrow distribution of threshold voltage (an average of -0.61 V and a standard deviation of 0.07 V, as shown in Figure 6f).

A wrapping text onto a 1 mL syringe tip was conducted to evaluate the flexibility of the array under extreme bending conditions (Figure 6g). The diameter of the tip is 430 μm ($r$ = 215 μm), as measured by a microscope (Figure 6h). In order to test the device under bending, a “L” shaped electrode was utilized as the extension of the gate electrode (Figure 6i). The wrapping procedure was conducted on water surface and the transfer curves of this device were tested before the wrapping (Figure 6i), during the wrapping (Figure 6j), and after the wrapping (Figure 6k), as plotted in Figure 6l. The nearly unchanged performance of the representative pixel suggests such wrapping test did little effects on the ultra-flexible array. The array device can be wrapped for more than 10 times or stay in the wrapped condition for over 1 week before the releasing, without any significant damage to the OFETs. As the total thickness of the ultra-flexible array is less than 1 μm, the actual strain applied to the devices is less than 0.5%, thus the transfer curves show almost no difference in drain and gate current under wrapping.

We believe these devices can broaden the application scope of the OFET significantly. Logic circuits, sensors, and radio-frequency identification (RFID) tags can be potentially fabricated onto ultra-flexible substrates by the presented methods. These OFETs can also be freely bended, folded or wrapped to function as transformable or injectable electronics for the robotic and healthcare applications. The ultra-flexible array can be transferred onto various surfaces with the help of the surface tension of water, as shown in Figure S9.

**Conclusion**

In conclusion, we demonstrated a feasible transfer method for organic semiconductor active layers that could overcome the trade-offs when selecting proper dielectric surfaces for OFETs. The method is proved efficient for both the vacuum sublimated thin films and the solution-processed single crystals. The highly crystallized thin films or single crystals can first be grown on $SiO_2$ substrates with appropriate SAM pre-treatments to obtain the high mobility character, and then be transferred on other substrates to gain better electrical properties such as low-voltage operation, near-zero turn-on voltage, negligible hysteresis, and bias-stress stability. Substrates that are originally not suitable for the vacuum sublimated thin films can now be utilized as the dielectric in OFETs, which showed only < 2% drain current decay after 20,000 s of continuous bias. Low-surface-energy substrates were allowed to work with solution-processed single crystals, exhibiting a remarkable mobility of 11.6 $cm^2V^{-1}s^{-1}$ and a negligible hysteresis window of 12.4 mV within an operating voltage of 4 V. The drain-current decay of the solution-processed single crystals after bias test is improved to 27%, corresponding to a threshold voltage shift of 260 mV. In addition, solution-processed single crystals were for the first time utilized to build high-performance, low-

voltage, and ultra-flexible OFET arrays. The presented transfer method reduces the rely of high-mobility OSC materials on growth substrates and offers new feasible approaches to construct high-performance OFET-based devices and circuits.

**Experimental Section**

*Fabrication of the vacuum-sublimated & transferred OFET devices*

Si wafers ($1.5 \times 1.5$ cm$^2$) with 300-nm-thick thermal oxide were cleaned with oxygen plasma (30 W, Harrick Plasma) for 15 min. ODTS (Sigma-aldrich) was deposited on the oxide wafers by immersing into its m-Xylene solution (1 mM) for 12 hours. $C_{10}$-DNTT thin films were vacuum sublimated at 80°C substrate temperature (base pressure $< 2 \times 10^{-6}$ Torr, deposition rate ≈ 0.4 Å/s). The 70-nm-thick Al gate electrodes were deposited through metal shadow masks by thermal evaporation (base pressure $< 2 \times 10^{-6}$ Torr, deposition rate > 100 Å/s). A 6.25 V anodization potential resulted in an $AlO_x$ layer on the Al electrode.[34] Three kinds of phosphonic acid-based SAMs were formed by immersing the freshly-generated $AlO_x$ into 1 mM isopropanol solutions of the SAM molecules. The areal capacitance of the $AlO_x$/ODPA dielectric at 1 kHz was measured as 309±10 nF/cm$^2$ from 16 metal-insulator-metal capacitors. The averaged areal capacitance of $AlO_x$/PhPA and $AlO_x$/FOPA was 340 ±15 nF/cm$^2$ and 320 ±13 nF/cm$^2$, respectively. Au (50 nm) source/drain electrodes were evaporated through a metal shadow mask (base pressure $< 2 \times 10^{-6}$ Torr, deposition rate ≈ 0.3 Å/s). For accurate device characterization, excess semiconductor areas outside the channel areas were properly trimmed or etched.

*Fabrication of the solution-processed & transferred OFET devices*

Si wafers (1.5 x 1.5 $cm^2$) with 300-nm-thick thermal oxide were cleaned with oxygen plasma (30 W, Harrick Plasma) for 15 min. PTS (J&K Scientific) self-assembled monolayer was deposited on the oxide wafers using the vapor phase method at 150 °C for 30 min. $C_{10}$-DNTT crystals (thickness of 8 nm, corresponding to 2 molecular layers) were deposited from a 0.2 mg/ml tetralin solution using the solution-shearing technique described in our previous work. The substrate and shearing blade were heated to 65°C and moved at a constant speed of 2 μm/s. After the crystal deposition, the samples were annealed in a vacuum oven at 80 °C overnight to remove any solvent residue. The ultra-flexible Cytop/polyacrylonitrile substrate was prepared by two steps: i) spin-coating of 35 mg/ml polyacrylonitrile on $SiO_2$ substrate and 90°C annealing for 1 hr; ii) spin-coating of 4.5 wt% Cytop on polyacrylonitrile surface and 100°C annealing for 1hr. The photolithography processes for the patterning of the gate electrodes, semiconductors, and source/drain electrodes were completed with OSCoR 5001 (Orthogonal Inc.) photoresist.

*The transfer method for thin films and crystals*

The protective layer was formed by spin-coating Orthogonal SL1 solution (Orthogonal Inc.) at 1000 RPM for 1 min. The film was then backed at 90 °C for 1 min to dry. The Si/$SiO_2$ wafer with $C_{10}$-DNTT films/crystals and the protective layer was placed in a polystyrene petri dish and HF was dropped at the edges of the wafer to initialize the film detachment. DI water was then slowly added to the petri dish to dilute the HF and lift the film up. After the whole film had been detached, the liquid was drained, and DI water was added (repeated five times). Afterward, the film was carried using a piece of glass from the original petri dish to one filled with DI water (repeated five times). Finally, the film was transferred to a petri dish filled with isopropanol with

the target substrate immersed inside. By draining the isopropanol, the film slowly dropped onto the target substrate and was attached firmly to it after the isopropanol had dried. Orthogonal Stripper solution (Orthogonal Inc.) was used to dissolve the protective layer and only leave the $C_{10}$-DNTT crystals on the target substrate.

*Characterization methods*

All electrical measurements were performed in an $N_2$-filled glove box. The electrical performance of the OFETs was measured with a Labview-programmed dual-channel Sourcemeter (Keithley 2636A). For the $SiO_2$-based high-voltage OFETs, the $V_{GS}$ scanning rate for the transfer curves was 5 V/s and the bias-stress condition was $V_{GS} = V_{DS} = -60$ V. For the $AlO_x$-based low-voltage OFETs, the $V_{GS}$ scanning rate for the transfer curves was 0.1 V/s and the bias-stress condition was $V_{GS} = V_{DS} = -3$ V. The peak mobility ($\mu_{peak}$) mentioned in the manuscript is defined as the highest value in Figure 1f, Figure 2i and Figure 4g during the forward ($V_{GS}$ from positive to negative) scan. The threshold voltage ($V_{TH}$) and subthreshold swing (SS) are calculated from the forward scan transfer curves. The hysteresis is defined as the $V_{TH}$ difference between the forward and reverse ($V_{GS}$ from positive to negative) transfer curves. The GIWAXS measurement was performed at the small and wide angle X-ray scattering beamline at the Australian Synchrotron.[35] A Pilatus 1M 2-dimentional detector with 0.172 mm × 0.172 mm active pixels was utilized in integration mode. The detector was positioned approximately 300 mm downstream from the sample location. The precise sample-to-detector distance was determined with a silver behenate standard. 11 keV incident X-ray with approximately a 0.25 mm × 0.1 mm spot was used to provide large enough $q$ space. The 2-dimentional raw data was reduced and analyzed with a modified version of Nika.[36] GIWAXS patterns shown have been corrected to represent real $Q_z$ and $Q_{xy}$

axes with the consideration of missing wedge. Critical incident angle was determined by the maximized scattering intensity from sample scattering with negligible contribution from underneath layer scattering. The XRD results were obtained using a Rikagu SmartLab 9kW system, while the AFM images were acquired with a Bruker Multimode 8 system. The CPOM images were obtained using a Nikon LV100POL microscope and the XPS analysis was performed with Thermo Scientific ESCALab 250Xi equipment. For XPS measurement, the thin film was transferred onto a 200-nm-thick Au-coated silicon wafer. Last, the FT-IR spectra were obtained using a Bruker Tensor 27 system.

**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

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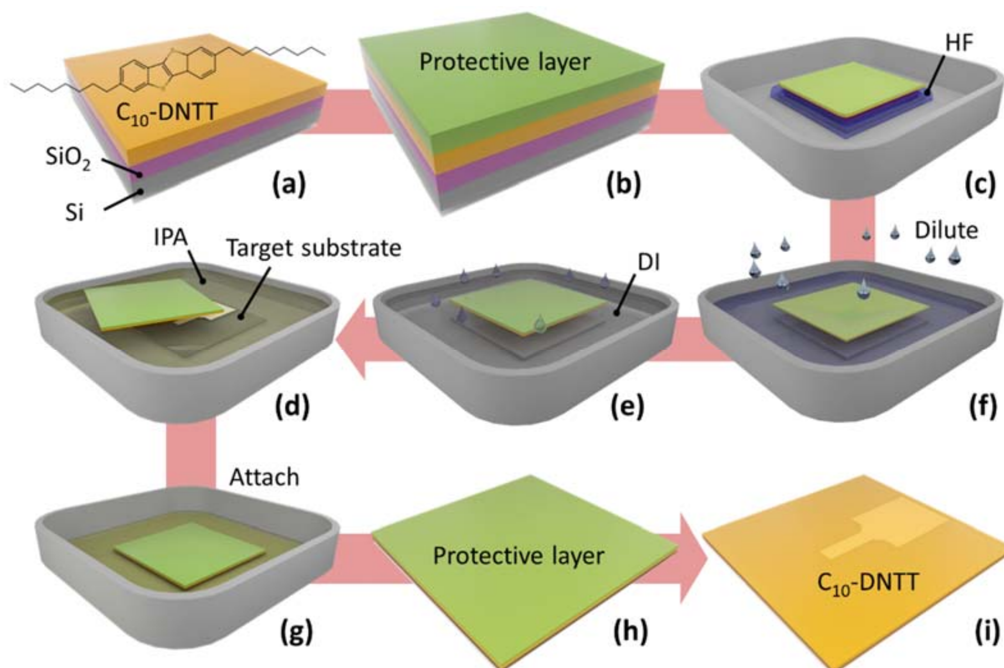


**Figure 1.** a) $C_{10}$-DNTT crystals on an $Si/SiO_2$ wafer. b) Formation of protective layer using the spin-coating method. c) Initial peeling off at the edges of the wafer induced with HF. d) DI water was used to lift the film up. e) DI water was added to dilute the HF until it was negligible. f) The film was transferred to an isopropanol container with the target substrate. g) The isopropanol was drained off and the film was left attached to the target substrate surface. h) The film on the target surface was left to dry. i) The protective layer was removed.

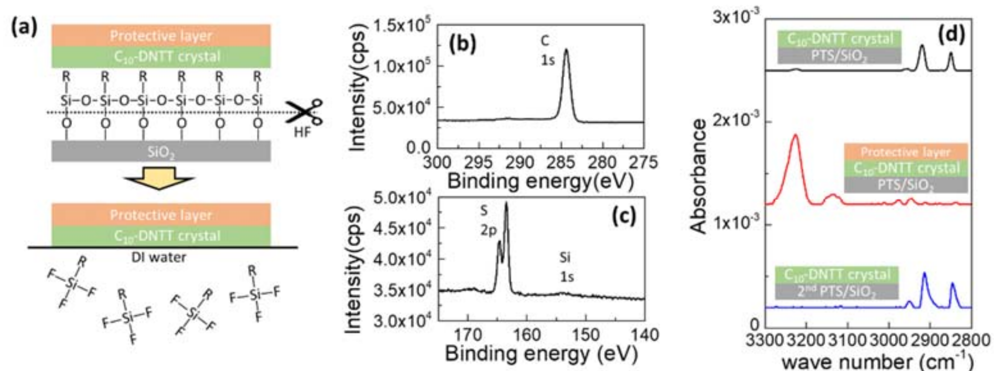


**Figure 2.** a) Schematic of the film releasing process. HF breaks Si-O bonds at the interface. The reacted silane molecules (PTS) disassemble into the liquid phase without the support of $SiO_2$ substrate, leaving a clean lower surface of the crystals to be attached to new substrates. b, c) XPS analysis of $C_{10}$-DNTT thin film after the transfer process. d) Reflective FT-IR analysis on pristine $C_{10}$-DNTT thin film, film with protective layer before transfer, and film after the transfer process.

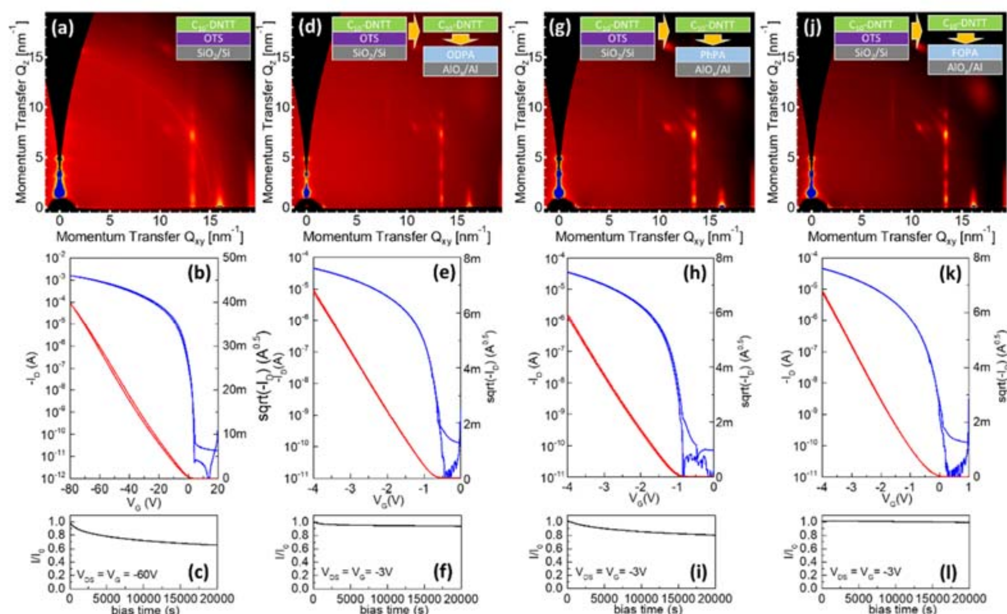


**Figure 3.** a) GIWAXS results of the as-grown 30-nm-thick $C_{10}$-DNTT deposited on ODTS-treated $SiO_2$ at substrate temperature of 80$^o$C. b) The transfer curves (blue lines) and $I_{DS}$ square-root plot (red lines) of the bottom-gate top-contact OFET based on the organic film in (a). The drain-source voltage is -80 V. c) The bias-stress measurement result of the transistor in (b). GIWAXS results of the 30-nm-thick $C_{10}$-DNTT in (a) transfered onto d) ODPA-treated $AlO_x$, g) PhPA-treated $AlO_x$, and j) FOPA-treated $AlO_x$. The transfer curves (blue lines) and $I_{DS}$ square-root plots (red lines) of the OFETs based on the transfered organic films onto e) ODPA-treated $AlO_x$, h) PhPA-treated $AlO_x$, and k) FOPA-treated $AlO_x$. The drain-source voltage is -4 V. The bias-stress measurement result of the transistor based on the transfered $C_{10}$-DNTT films onto f) ODPA-treated $AlO_x$, i) PhPA-treated $AlO_x$, and l) FOPA-treated $AlO_x$. The drain/source electrodes were formed by 50-nm-thick evaporated Au through metal shadow masks. The channel width and length were 480 μm and 60 μm.

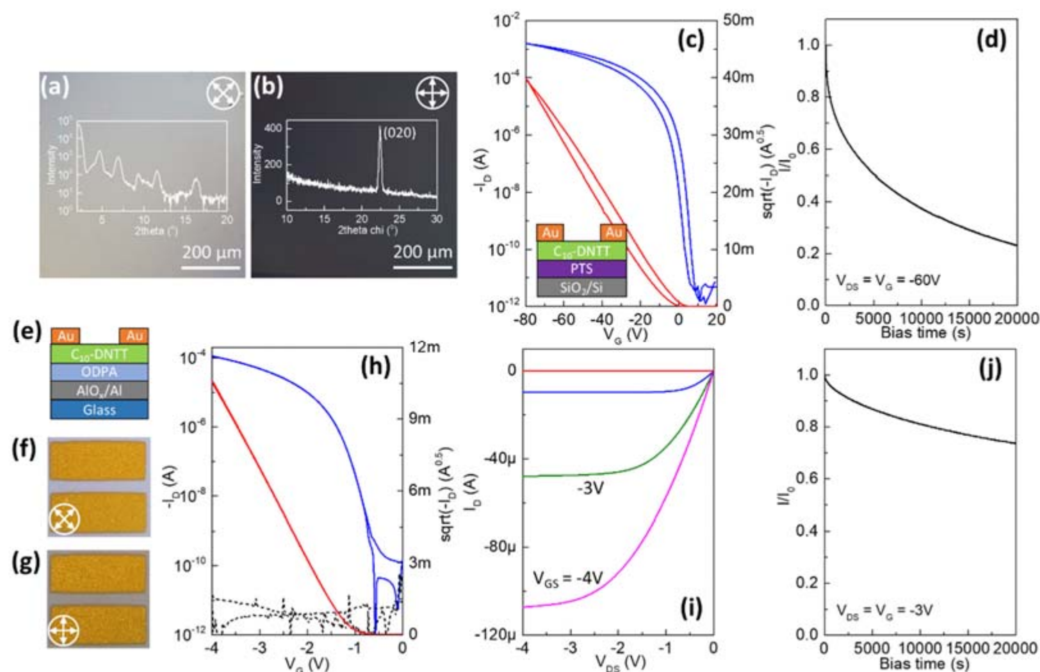


**Figure 4.** a) Cross-polarized optical microscopy (CPOM) image of the solution-processed $C_{10}$-DNTT crystals (The crossed white arrows denote the directions of the polarizer and analyzer.) Inset: the out-of-plane XRD results of the crystals. b) CPOM image of the crystals in (a) by rotating clockwisely for 45$^{o}$. Inset: the in-plane XRD results of the crystals. c) Transfer curves and square-root plot of $I_{DS}$ of the device based on as-grown $C_{10}$-DNTT crystals. Inset: the schematic device structure on the as-grown substrate. d) The bias-stress measurement result of the transistor in (c). e) The schematic OFET device structure with the $C_{10}$-DNTT crystals transferred onto ODPA/$AlO_x$/Al. f, g) CPOM images of the device based on single crystal of $C_{10}$-DNTT. h) Transfer curves (blue lines), $I_{DS}$ square-root plot (red lines), and gate leakage current (black dashed lines) of the device in (f). i) The output curves of the device in (f). The bias-stress measurement result of the device in (f). The drain/source electrodes were formed by 50-nm-thick evaporated Au through metal shadow masks. The channel width and length were 480 μm and 60 μm.

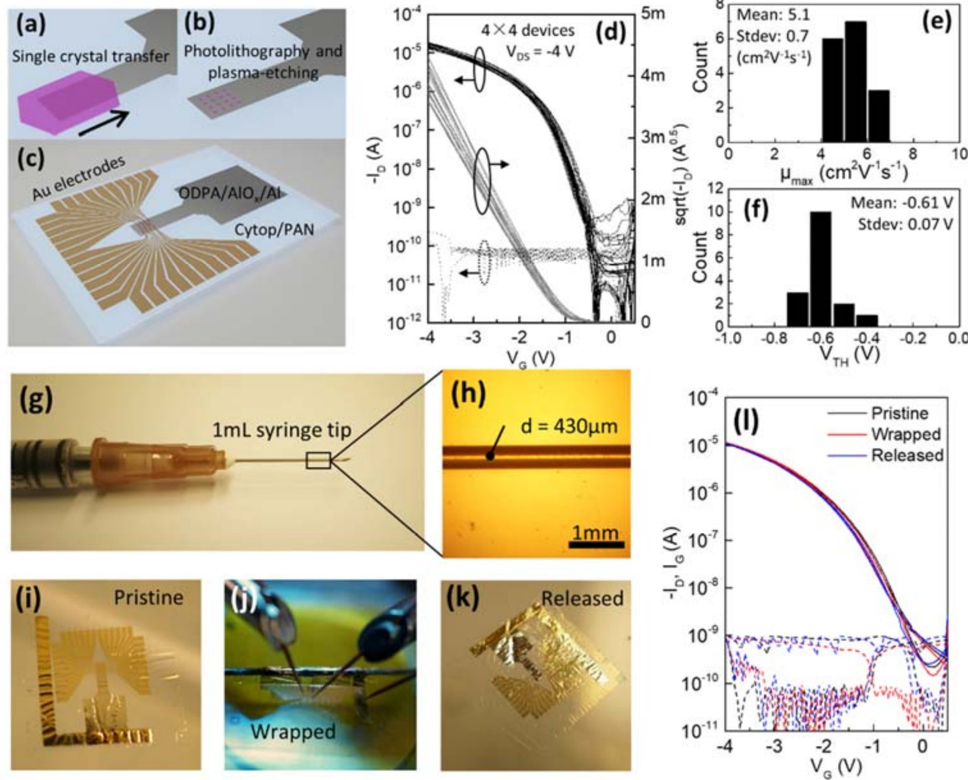


**Figure 6.** a) A $C_{10}$-DNTT bilayer single crystal on the effective area of the dielectric and gate electrode. The black straight arrow denotes the shearing direction during crystal deposition. b) The single crystal after photolithography as the active layers for the 16 pixels. c) The formation of the top-contact source/drain electrodes by photolithography. d) Transfer curves (black lines), square root plot of $I_D$ (grey lines), and averaged leakage current $I_G$ (dotted lines) of all 16 OFET pixels in the array device. Histograms of maximum mobility e) and threshold voltage f) extracted from all 16 OFET pixels in the array device. g) The 1 mL syringe tip ultilized for wrapping test. h) Optical microscopy image of the syring tip. The tested array device (i) before (j) during, and (k) after the wrapping test. l) The trasnfer curves (solid lines) and leakage current (dotted lines) of one pixel beofre, during, and after the wrapping test. The $V_{DS}$ was -4 V. The channel width and length for the array device were 80 µm and 40 µm.

**Keywords: low-voltage OFET, single crystal, bias-stress stability, array, ultra-flexible**

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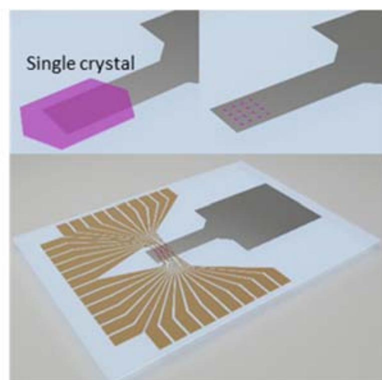
**A transfer method for organic semiconductor towards high-mobility, bias-stable, and flexible electronics**



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# Supporting Information

**A transfer method for organic semiconductor towards high-mobility, bias-stable, and flexible electronics**

*Boyu Peng, Xudong Ji, Xuechen Jiao, Ming Chu, Jinyu Liu, Yang Li, Ming Chen, Zhiwen Zhou, Cuiping Zhang, Qian Miao, Huanli Dong, Baoling Huang, Wenping Hu, Shien-Ping Feng, Wendi Li and Paddy K. L. Chan**

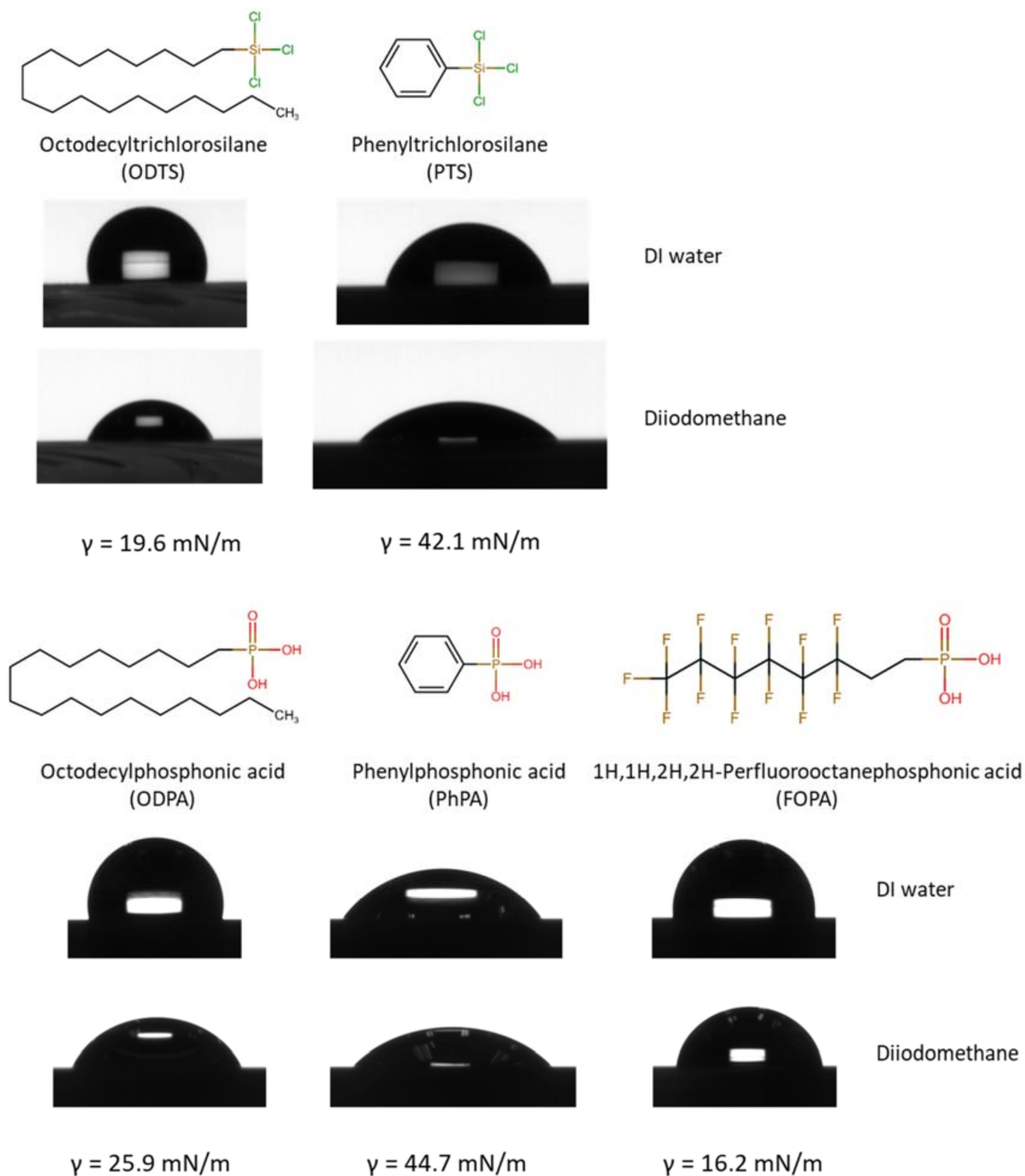


**Figure S1.** The SAM-treated surfaces used in the current work. The chemical structures, abbreviations, contact angle measurement from DI water and diiodomethane, and corresponding surface energy calculations are shown.

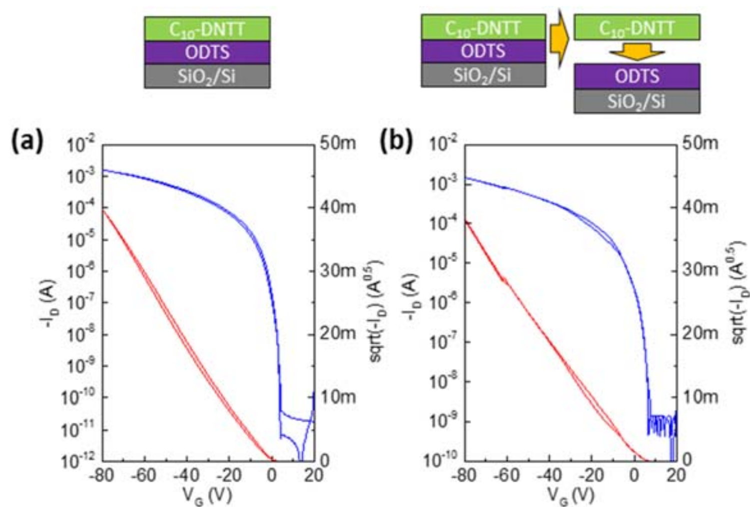


**Figure S2.** a) The transfer curves (blue lines) and $I_{DS}$ square-root plot (red lines) of the bottom-gate top-contact OFET based on the as-grown $C_{10}$-DNTT thin film on ODTS/$SiO_2$. b) The transfer curves (blue lines) and $I_{DS}$ square-root plot (red lines) of the device with transfered $C_{10}$-DNTT thin film onto ODTS/$SiO_2$.

**Table S1. Electrical performance of OFETs based on different semiconductor and dielectric layers.**

| Substrate | Active layer[1] | Fabrication method[2] | $\mu_{peak}$ (σ)[3] | $V_{TH}$ (σ)[4] | *Hys.* (σ)[5] | *SS* (σ)[6] | $N_{trap}$ ($cm^{-2}eV^{-1}$) | Current decay[8] |
|---|---|---|---|---|---|---|---|---|
| ODTS-$SiO_2$ | Thin film | As-grown | 8.05 (0.17) | 1.67 (0.11) | 1.34 (0.09) | 0.91 (0.08) | $1.03 \times 10^{12}$ | 35% |
| ODPA-$AlO_x$ | Thin film | Transferred | 5.40 (0.15) | -1.11 (0.23) | 45 (7.9) $\times 10^{-3}$ | 108 (18) $\times 10^{-3}$ | $1.59 \times 10^{12}$ | 6% |
| PhPA-$AlO_x$ | Thin film | Transferred | 4.65 (0.18) | -1.12 (0.29) | 61 (11.5) $\times 10^{-3}$ | 127 (26) $\times 10^{-3}$ | $2.47 \times 10^{12}$ | 19% |
| FOPA-$AlO_x$ | Thin film | Transferred | 4.95 (0.13) | -0.75 (0.17) | 20 (5.1) $\times 10^{-3}$ | 106 (17) $\times 10^{-3}$ | $1.58 \times 10^{12}$ | 2% |
| PTS-$SiO_2$ | Bilayer crystal | As-grown | 10.0 (0.95) | -4.72 (1.78) | 5.28 (1.08) | 1.45 (0.21) | $1.69 \times 10^{12}$ | 77% |
| ODPA-$AlO_x$ | Bilayer crystal | Transferred | 11.57 (0.78) | -1.11 (0.10) | 12.4 (4.1) $\times 10^{-3}$ | 131 (41) $\times 10^{-3}$ | $2.34 \times 10^{12}$ | 27% |

1. 30 devices are measured for thin film-based devices, 15 devices are measured for bilayer crystal-based devices.
2. As-grown means the growth substrates are used for dielectric in OFETs. Transferred means the semiconductor is first grown on ODTS-$SiO_2$ (thin film) or PTS-$SiO_2$ (bilayer crystal) and transferred.
3. Highest value in mobility-$V_{GS}$ plot of the forward ($V_{GS}$ from positive to negative) scan transfer curves. σ stands for the standard deviation. Unit: $cm^2V^{-1}s^{-1}$.
4. Threshold voltage. Acquired from forward scan of transfer curves. Unit: V.
5. Hysteresis window. The difference in $V_{TH}$ of the transfer curves during forward and reverse ($V_{GS}$ from negative to positive) scan. Unit: V.
6. Subthreshold swing. Acquired from forward scan of transfer curves. Unit: V/decade.
7. As calculated from equation based on the *SS* values:
   $$SS = \frac{kT\ln 10}{e}\left(1 + \frac{e^2}{C_i}N_{trap}\right)$$
8. Defined as the drain current decay after the 20,000 s bias-stress test. Acquired from the device with highest mobility value.

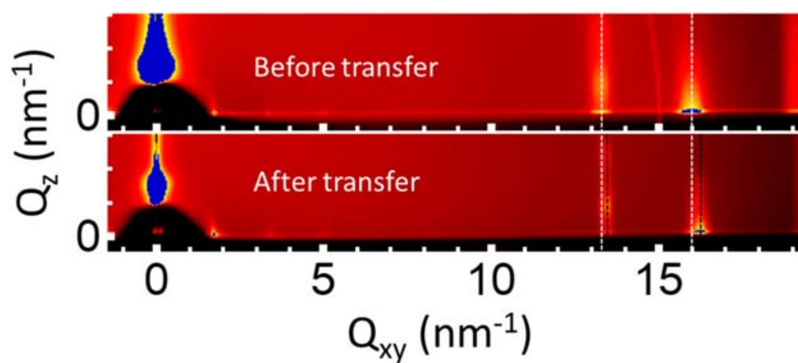


**Figure S3.** Magnified GIWAXS results close to $Q_{xy}$ axes of Figure 3a and d. White dotted lines represent the $Q_{xy}$ of (11L) and (02L) peaks of the $C_{10}$-DNTT film before transfer. Black dotted lines correspond to $Q_{xy}$ of (11L) and (02L) peaks of the $C_{10}$-DNTT film after transfer.

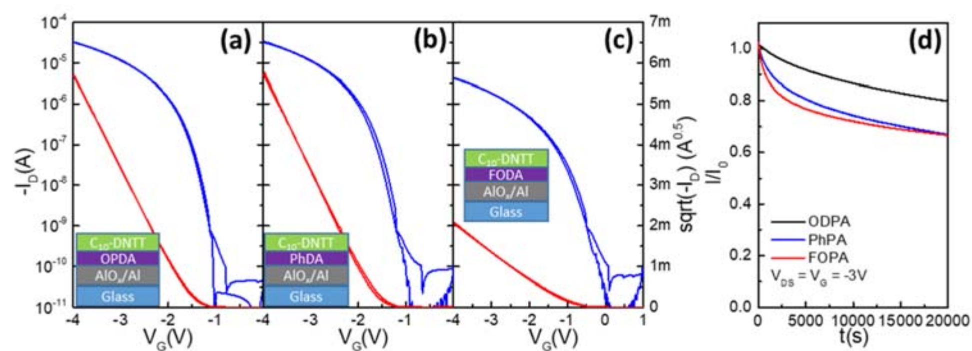


**Figure S4.** Low voltage OFETs performance with room temperature sublimated 30-nm-thick $C_{10}$-DNTT layers as the active layers and a) ODPA, b) PhPA, and c) FOPA-treated $AlO_x$ as the dielectric interfaces. The $V_{DS}$ in (a-c) is -4 V. The channel width and length are 480 μm and 80 μm. d) The 20,000 s continuous bias stress test on devices in (a-c).

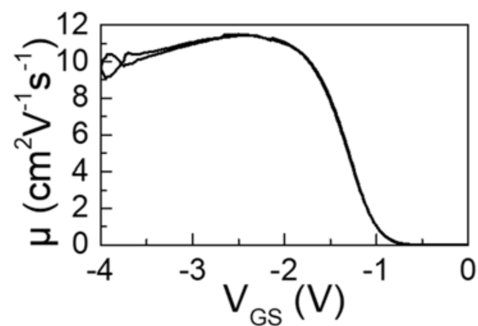


**Figure S5.** Apparent mobility vs. $V_{GS}$ plot of the low-voltage device based on transferred bilayer $C_{10}$-DNTT crystals in Figure 4h.

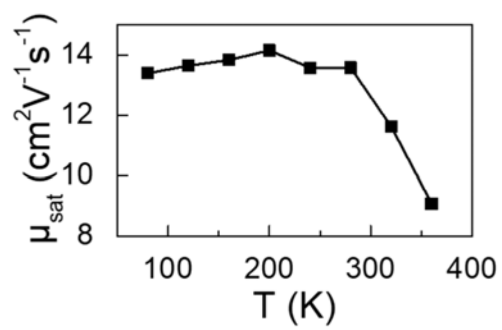


**Figure S6.** Saturation mobility vs. testing temperature of the device in Figure 4h.

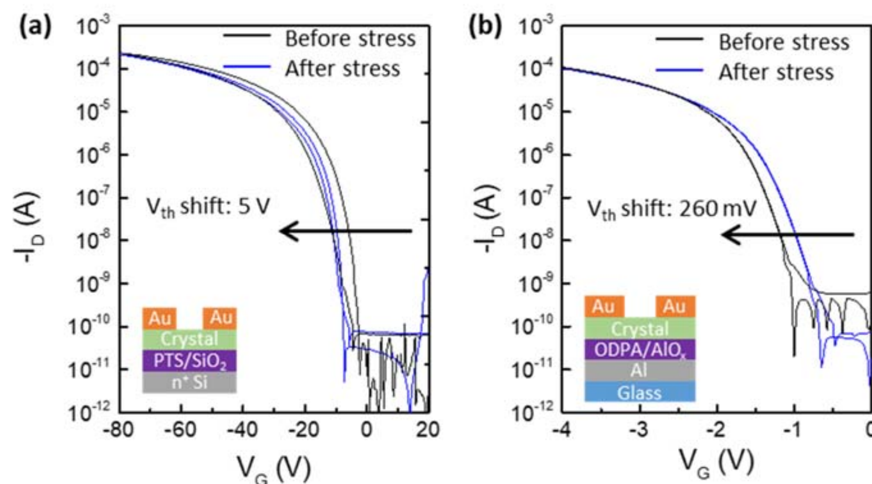


**Figure S7.** a) Transfer curves of solution-processed $C_{10}$-DNTT crystal grown on PTS treated $SiO_2$ before and after stress. The bias condition is $V_{GS} = V_{DS} = -60$ V for 20,000s. Inset illustrates the device structure. b) Transfer curves of solution-processed $C_{10}$-DNTT crystals transferred onto ODPA/$AlO_x$ before and after stress. The bias condition is $V_{GS} = V_{DS} = -3$ V for 20,000s. Inset illustrates the device structure. The source drain electrodes were formed by 50-nm-thick Au through a metal shadow mask. The channel width and length were 480μm and 60 μm.

**Table S2.** Representative low-voltage OFETs in literature with mobility higher than 1 $cm^2V^{-1}s^{-1}$ and operating voltage smaller than 5 V.

| Method | Semiconductor | Device Structure | Dielectric | Carrier Mobility [$cm^2V^{-1}s^{-1}$] | Operating Voltage [V] | Ref. |
|---|---|---|---|---|---|---|
| Vacuum-processed | C60 | BGTC | pV3D3 | 1.83 | 3 | [1] |
| Solution-processed | FS111 | BGTC | HfO2 | 1.0 | 2 | [2] |
| Vacuum-processed | C60 | BGTC | AlOx | 2.17 | 3 | [3] |
| Vacuum-processed | pentacene | BGTC | PVP/YOx | 1.74 | 5 | [4] |
| Vacuum-processed | pentacene | BGTC | (PhO-19-PA) SAM/AlOx | 1.1 | 2 | [5] |
| Vacuum-processed | DNTT | BGTC | SAM/AlOx | 3.0 | 5 | [6] |
| Vacuum-processed | pentacene | BGTC | SAM/AlOx | 1 | 3 | [7] |
| Vacuum-processed | DNTT | BGTC | SAM/AlOx | 2.96 | 3 | [8] |
| Vaccum-processed | C10-DNTT | BGTC | SAM/AlOx | 4.43 | 3 | [9] |
| | DPh-DNTT | | | 5.29 | | |
| | DPh-BBTNDT | | | 4.16 | | |
| Vacuum-processed | DNTT | BGTC | BST | 1.51 | 2 | [10] |
| | pentacene | | | 1.12 | | |
| Vacuum-processed | DNTT | BGTC | SAM/AlOx | 2.11 | 4 | [11] |
| Vacuum-processed | C60 | BGTC | SAM/AlOy/TiOx | 5.1 | 3 | [12] |
| Solution-processed | TIPS-TAP | | | 5.0 | | |
| Solution-processed | C10-DNTT | BGTC | SAM/BST | 4.2 | 4 | [13] |
| Solution-processed | C8-BTBT | BGTC | AlOx | 9.8 | 4 | [14] |
| Solution-processed | C10-DNTT | BGTC | SAM/AlOx | 11.6 | 4 | **This work** |

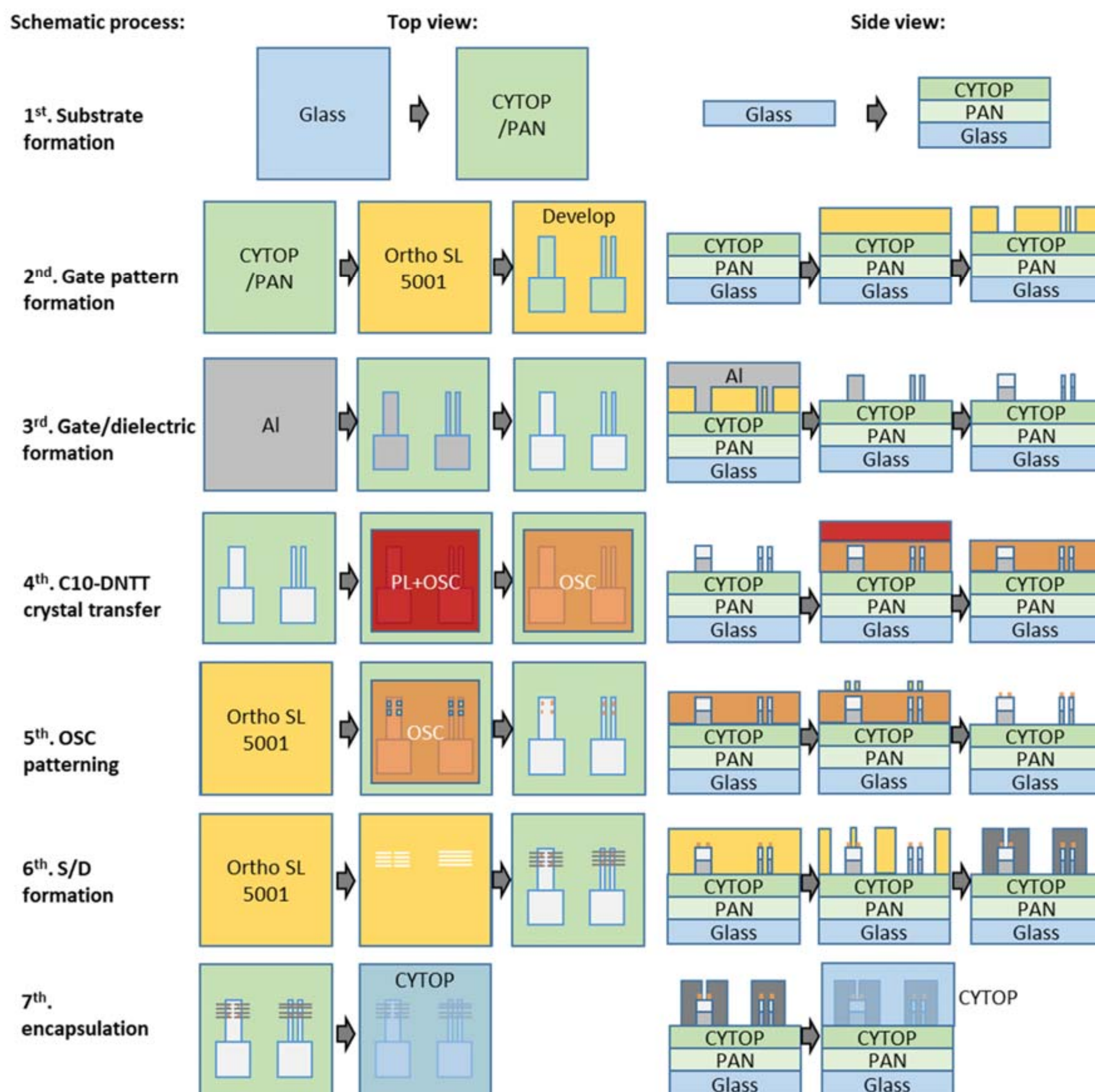


**Figure S8.** Schematic of fabrication procedures of the single-crystalline ultra-flexible array.

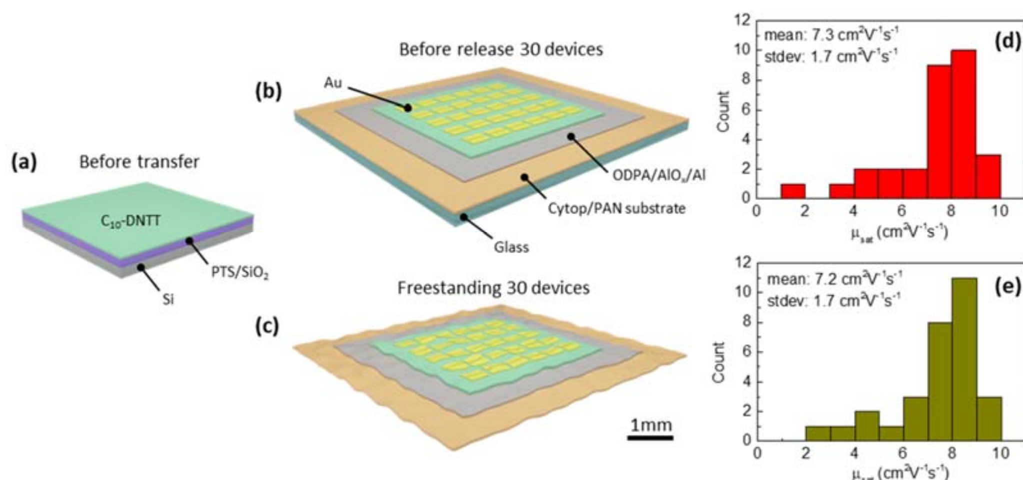


**Figure S9.** a) Schematic of as-grown $C_{10}$-DNTT bi-layer crystals on PTS/$SiO_2$ substrate. b) The crystals in (a) was transfered onto ODPA/$AlO_x$/Al on Cytop/PAN substrate to constructure ultra-flexible devices. 30 pairs of source/drain Au electrodes were thermally evaporated to form 30 OFET devices. The ultra-flexible substrate was still on rigid glass substrate. c) The ultra-flexible substrate was released from glass substrate as ultra-flexible OFET devices. d) The saturation mobility (extracted from $V_G$ range from -80 V to -10 V) distribution of 30 devices in (b). e) The saturation mobility (extracted from $V_G$ range from -80 V to -10 V) distribution of 30 devices in (c).

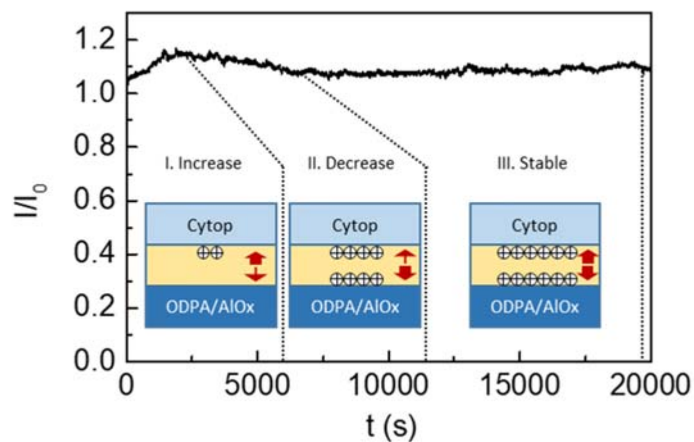


**Figure S10.** The 20,000 s continuous bias stress test conducted in ambient condition on the ultra-flexible device, which is based on transferred $C_{10}$-DNTT crystals and PAN/Cytop double layer substrate. At regime I, the trapping rate at Cytop/OSC interface is faster. At regime II, the trapping rate at ODPA/OSC interface is fast. While at regime III, the trapping rate at the two interfaces are similar. The $V_{GS}$ and $V_{DS}$ are both at -3 V.

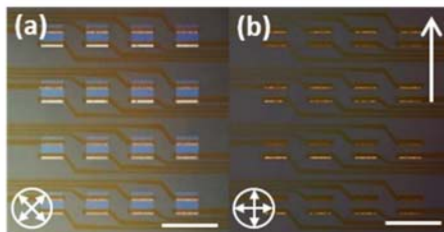


**Figure S12.** a, b) CPOM image of the 4 × 4 OFET pixels in the center region of the array. The crossed white arrows denote the directions of polarizer and analyzer. The scale bars represent 200 μm. The white straight arrow shows the shearing direction of the transferred single crystal of $C_{10}$-DNTT.

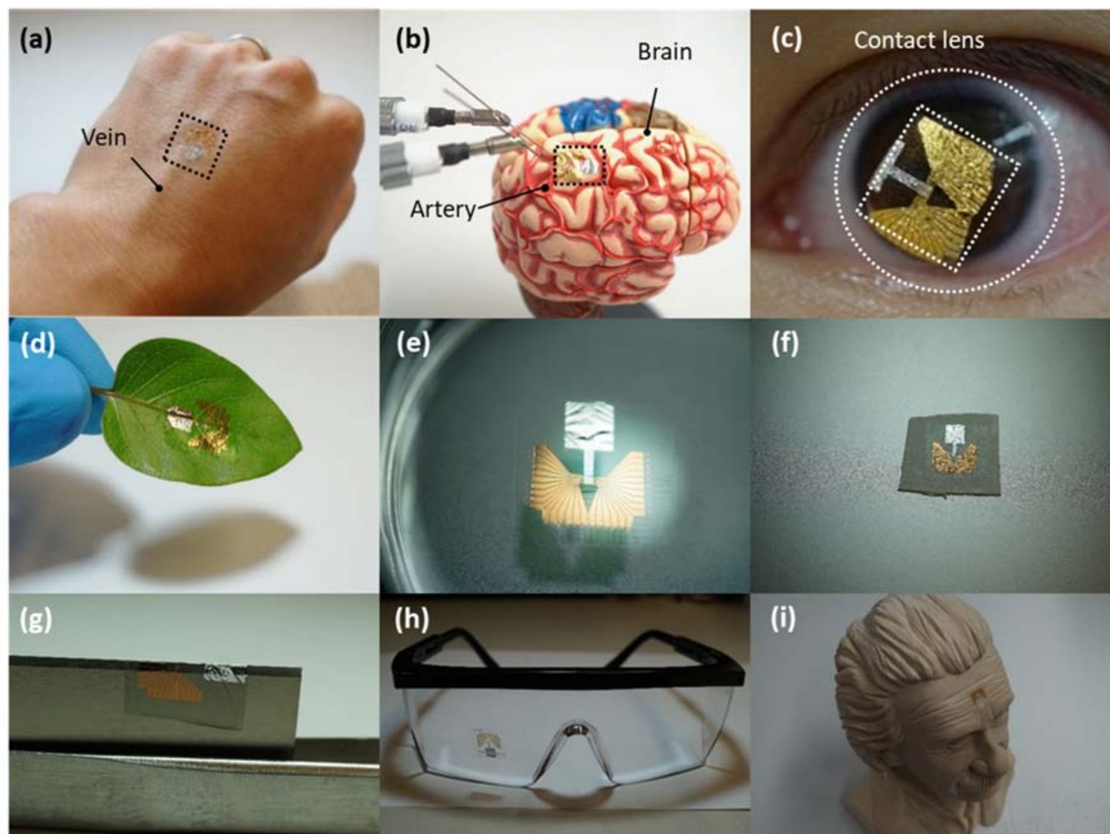


**Figure S13.** Optical images of the single-crystalline ultra-flexible array devices transferred on a) skin surface, b) a human brain model, c) a contact lens worn in an eye, d) a leaf, e) wafer surface, f) a piece of cloth, g) a razor blade, h) a goggle, and i) a statue of Albert Einstein.

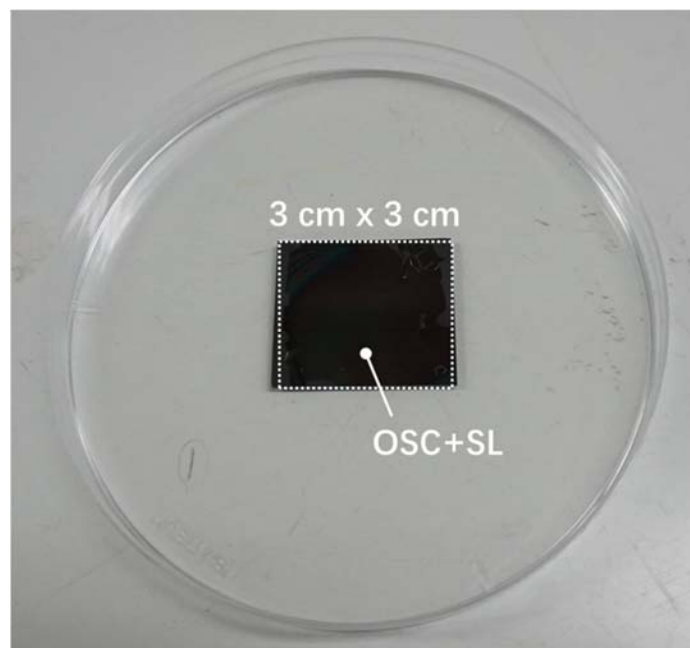


**Figure S14.** Optical image of the large-area (3 cm × 3 cm) transferred film ($C_{10}$-DNTT layer + sacrificial layer) onto ODPA-treated $AlO_x$ on silicon wafer. The transfer process is shown in **Supporting Video S2**.

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