



PAPER

Effects of annealing temperature of NbLaO gate dielectric on electrical properties of ZnO thin-film transistor

OPEN ACCESS

RECEIVED
5 May 2017REVISED
1 August 2017ACCEPTED FOR PUBLICATION
6 September 2017PUBLISHED
17 October 2017

Original content from this work may be used under the terms of the [Creative Commons Attribution 3.0 licence](#).

Any further distribution of this work must maintain attribution to the author(s) and the title of the work, journal citation and DOI.

Y R Liu^{1,4}, H Huang¹, P T Lai^{2,4}, W J Wu³ and R S Chen¹ ¹ School of Electronic and Information Engineering, South China University of Technology, Guangzhou 510640, People's Republic of China² Department of Electrical and Electronic Engineering, the University of Hong Kong, Pokfulam Rd., Hong Kong, People's Republic of China³ The State Key Laboratory of Luminescent Materials and Devices, South China University of Technology, Guangzhou, 510640, People's Republic of China⁴ Authors to whom any correspondence should be addressed.E-mail: phlyr@scut.edu.cn and laip@eee.hku.hk

Keywords: thin film transistors, zinc oxide, NbLaO gate dielectric, annealing

Abstract

A bottom-gate zinc-oxide thin-film transistor (ZnO TFT) with high-*k* NbLaO as gate dielectric was fabricated on indium tin oxide-coated glass substrate by radio frequency sputtering. The NbLaO gate dielectric was annealed in N₂ at different temperatures (200 °C, 300 °C, and 400 °C) for 30 min to investigate the effects of the annealing temperature on the electrical properties of the device. It is demonstrated that the ZnO TFT annealed at 300 °C exhibits the relatively good electrical performance with mobility of 20.5 cm² V⁻¹ s⁻¹, off-state current of 3.4 pA, subthreshold slope of 0.18 V/decade, on/off current ratio of 6.25 × 10⁷ and small hysteresis, which are due to reduction of deep traps in the high-*k* film or at gate-dielectric/semiconductor interface as supported by using a low-frequency noise analysis.

1. Introduction

Zinc oxide (ZnO) thin film transistors (TFTs) have been extensively studied due to the desirable properties of ZnO, including large band gap, low processing temperature, and high transparency in the visible range [1–4]. ZnO TFTs have been reported using many techniques such as magnetron sputtering [5, 6], atomic layer deposition [7, 8], pulsed laser deposition [9, 10], and solution processing [11, 12]. High-performance TFTs with high carrier mobility and low operating voltage are required to achieve low power consumption in applications like next generation transparent and flexible electronics [13, 14]. In TFT devices, the gate dielectric plays an important role in controlling device performance as well as the semiconductor active layer [15, 16]. It is known that conventional gate dielectrics such as silicon oxide (SiO₂) and aluminum oxide (Al₂O₃) cannot meet these requirements because of their low dielectric constant, despite some advantages such as good quality interface with the semiconductor and low leakage current due to the large band gap of Al₂O₃ [16, 17]. To further improve the performance of ZnO TFT, various high-*k* materials have been adopted as the gate dielectric to reduce the operating voltage of the devices and increase carrier mobility. Adamopoulos *et al* [11] reported that ZnO TFTs with HfO₂ gate dielectric fabricated by spray pyrolysis technique exhibits a low operating voltage of 6 V and electron mobility of 40 cm² V⁻¹ s⁻¹. Song *et al* [18] used Ta₂O₅ gate dielectric, and mobility over 50 cm² V⁻¹ s⁻¹ and low operating voltage of 4 V were achieved in ZnO TFTs fabricated by radio-frequency magnetron sputtering. Su *et al* [19] fabricated ZnO TFTs with HfLaO gate dielectric, which resulted in a low operating voltage <3 V and a carrier mobility of 3.5 cm² V⁻¹ s⁻¹. Subramanian *et al* [20] explored solution-processed ZrO₂ gate dielectric and demonstrated a mobility of 20 cm² V⁻¹ s⁻¹ and a low operating voltage <3 V in ZnO TFTs. However, there are several potential disadvantages associated with using high-*k* gate dielectric in TFTs. For example, defects in high-*k* dielectrics could lead to defect-assisted current transport such as the Poole–Frenkel effect, which increases the leakage current of the devices.

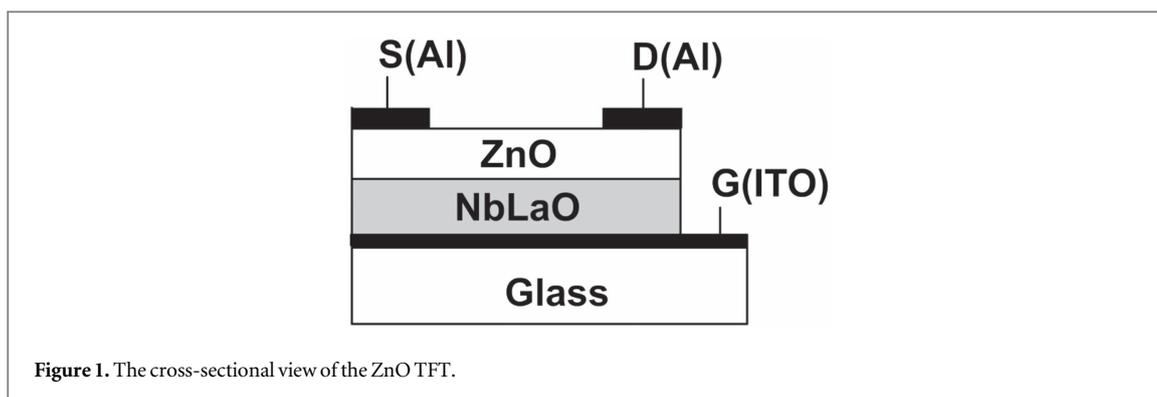


Figure 1. The cross-sectional view of the ZnO TFT.

Nb_2O_5 , with a high k value (>40), was used as the dielectric layer in metal–insulator–metal capacitor to achieve a high capacitance density of $1.76 \text{ fF } \mu\text{m}^{-2}$ with acceptable breakdown voltage [21], demonstrating its great potential to reduce the operating voltage of TFT. However, Nb_2O_5 film has high polarizability, small bandgap (3.4 eV) and high defect concentration (10^{19} – 10^{21} cm^{-3}) [22], which induces strong Coulomb scattering on charge carriers and high leakage current. Fortunately, it was reported that La incorporation in Nb_2O_5 gate dielectric could decrease its surface roughness and passivate the defect states at/near the dielectric/InGaZnO interface [23]. On the other hand, Park *et al* [24] reported that the performance of ZnO TFTs with SiO_2 gate insulators was improved by rapid thermal annealing. Kim *et al* [25] reported that the characteristics of ZnO TFT with low-temperature oxide gate insulator were improved by low-temperature annealing. Therefore, the annealing temperature can greatly influence the electrical performance of the ZnO TFTs, but the related reports, especially about the effects of annealing temperature of NbLaO gate insulator on the electrical performance of ZnO TFTs, are still very limited. So, in this work, ZnO TFTs with low-temperature-annealed NbLaO gate dielectric are fabricated on indium tin oxide (ITO)-coated glass substrate by RF magnetron sputtering, and the influence of the annealing temperature on the electrical properties of ZnO-TFTs is investigated.

2. Experimental details

Figure 1 shows the cross-sectional view of the ZnO TFT with NbLaO gate dielectric. ITO-coated glass substrates (ITO acting as the gate electrode) was used to make ZnO TFTs with a bottom-gate top-contact configuration. Initially, ITO coated glass was ultrasonically cleaned in acetone and methanol and then in de-ionized water for 15 min each. After having been dried by N_2 gas, the cleaned substrate was transferred immediately to a sputtering system, and then a NbLaO film acting as the gate dielectric was deposited on the ITO films (six samples) by co-sputtering of Nb metal target and La_2O_3 ceramic target in an Ar/O_2 (24/6 sccm) mixed ambient. During this process, the direct current/RF power for the Nb/ La_2O_3 targets were set as 0.02 A/ 45 W respectively. After that, all the samples were divided into three groups which were annealed at different temperatures (200 °C, 300 °C, and 400 °C) in a N_2 ambient for 30 min. Subsequently, a 65 nm ZnO film acting as the active layer was deposited on the gate insulator by RF sputtering of a ZnO ceramic target (99.99% in purity). The ZnO film was prepared at a sputtering power of 50 W in an Ar/O_2 (24/1 sccm) mixed ambient. Al source/drain (S/D) electrodes were deposited by thermal evaporation through a shadow mask. Finally, the devices were annealed at 200 °C for 30 min in N_2 to reduce the contact resistance of the source/drain electrodes. Except the annealing processes, all the other processes were carried out at room temperature. In addition, Al/NbLaO/ITO (MIM) capacitors were also prepared to monitor the gate oxide capacitance per unit area (C_{ox}) of the TFTs annealed at different temperatures. The channel width (W) and channel length (L) of the device were 350 μm and 100 μm respectively.

The physical thicknesses of the NbLaO and ZnO films were measured by spectroscopic reflectometer (Ocean Optics, NanoCalc-2000). The electrical characteristics of the TFTs and the 1 MHz capacitance–voltage (C – V) characteristics of the capacitors were measured using a HP 4156 C semiconductor parameter analyzer and a HP 4284 A precision LCR meter, respectively. For the output characteristic (I_{D} – V_{DS}) of the TFTs, the drain-to-source voltage (V_{DS}) was increased from 0 to 10 V with a voltage step of 0.2 V, while the gate-to-source voltage (V_{GS}) was increased from 1 to 5 V with a voltage step of 1 V. For the transfer characteristics (I_{D} – V_{GS}) of the TFTs, V_{GS} was increased from -5 to 12 V with a voltage step of 0.2 V, while V_{DS} was fixed at 6 V. All the electrical characterizations and C – V measurements were conducted at room temperature under a light-tight, electrically-shielded condition.

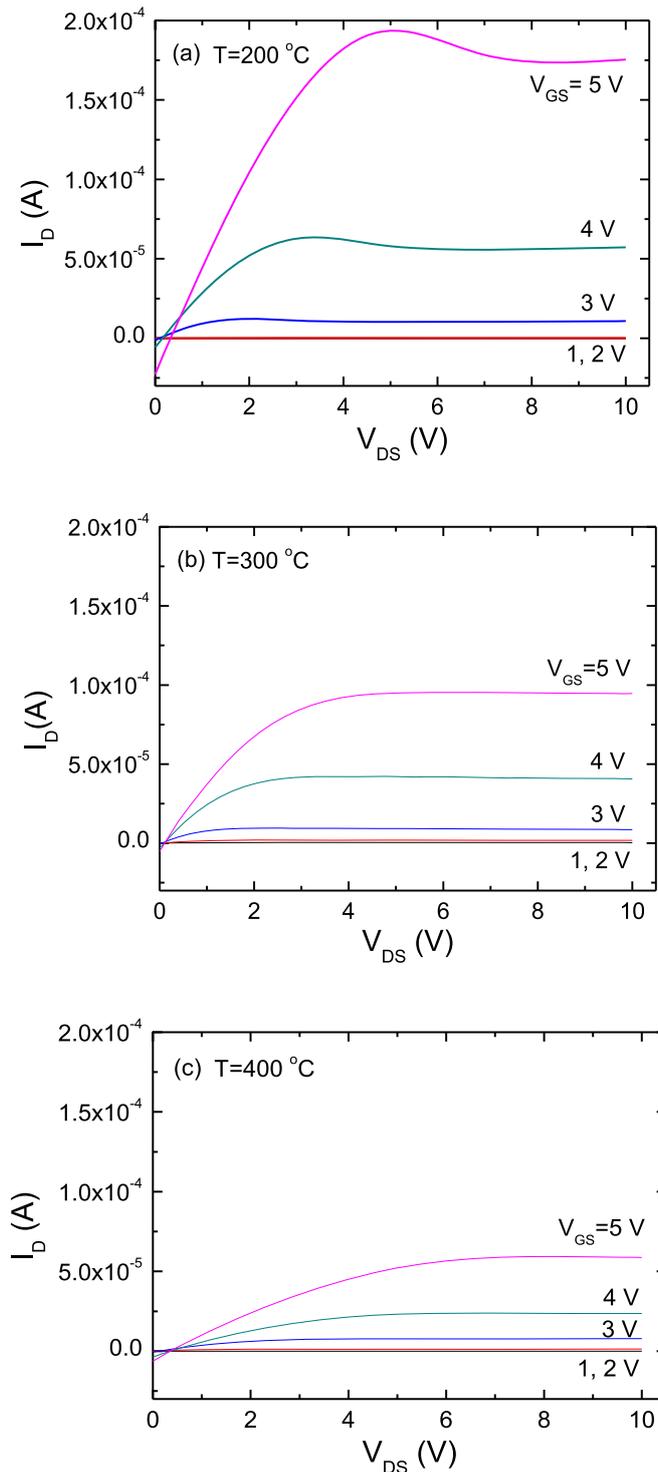


Figure 2. Output characteristics curves (I_D - V_{DS}) of the ZnO TFT with the NbLaO gate dielectric annealed at different temperatures. (a) 200 °C, (b) 300 °C, (c) 400 °C.

3. Results and discussion

Figure 2 shows the output characteristics (I_D - V_{DS}) of the ZnO TFTs with different annealing temperatures for the NbLaO gate dielectric. It can be seen that all the samples have good ohmic contact at the Al/channel interface because no current crowding at low V_{DS} is found. The ZnO TFTs show a typical behavior of a TFT device with an n-type semiconductor as active channel layer, in which the drain current increases with positive gate voltage (a positive gate-to-source voltage induces electron accumulation in the channel). The ZnO TFTs exhibit an excellent saturation behavior at high V_{DS} for the two annealing temperatures of 300 °C and 400 °C. But for the annealing temperature of 200 °C, after V_{DS} increases to the pinch-off voltage, the drain current decreases firstly

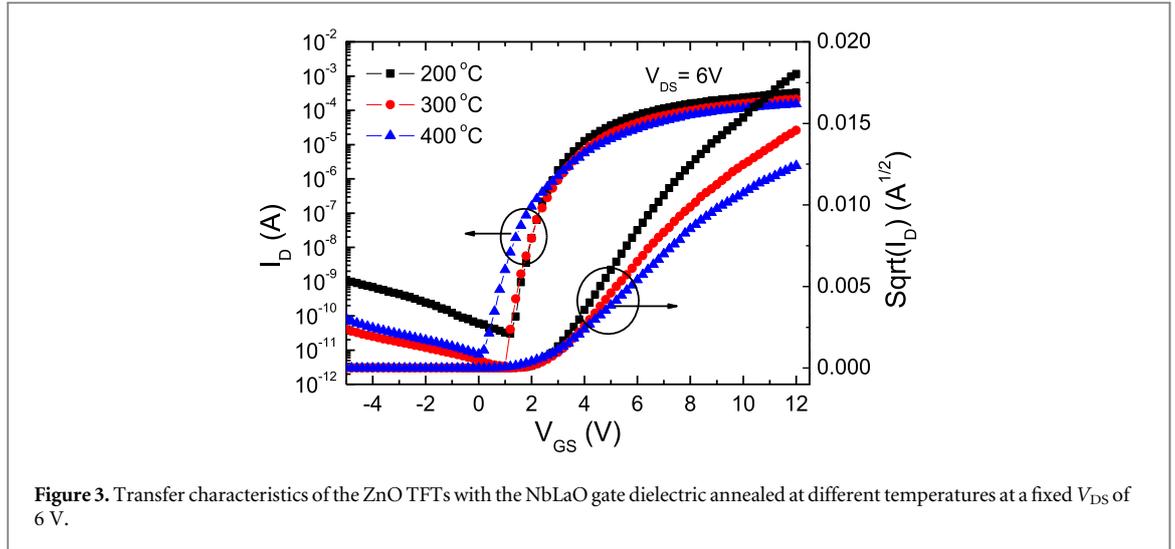


Figure 3. Transfer characteristics of the ZnO TFTs with the NbLaO gate dielectric annealed at different temperatures at a fixed V_{DS} of 6 V.

with increasing V_{DS} , and then remains unchanged. This unusual saturation behavior can be explained as follows. When the device is in on-state and V_{DS} is smaller than the pinch-off voltage, the channel is in a strong accumulation condition, the donor-like interface traps at the NbLaO/ZnO interface are filled with electrons from the channel because the trap level is below the Fermi level at the surface of ZnO, and so the drain current increases linearly with the increasing V_{DS} due to increasing channel field. But when V_{DS} increases up to the pinch-off voltage, the channel region near the drain is in depletion condition, the donor-like interface traps above the Fermi level is positively charged and so able to capture electrons injected from the source, and thus resulting in a reduction of the drain current. However, when V_{DS} continues to increase to a certain value, the donor-like interface traps above the Fermi level are all basically filled with electrons and do not continue to increase with increasing drain voltage due to the Fermi level pinning effect, and so the drain current remains unchanged for further increase in V_{DS} . In addition, it can be also noted that the sample annealed at 300 °C exhibits a smallest gate-leakage current according to the negative drain current at zero V_{DS} under the same V_{GS} . The above analysis indicates that the annealing at an appropriate temperature (e.g. 300 °C) can reduce deep traps in the gate dielectric or at/near the NbLaO/ZnO interface. This may be because the densification of the NbLaO film annealed at 300 °C is improved to reduce oxide charge, and unsaturated bonds in the NbLaO gate dielectric.

Figure 3 depicts the transfer characteristics (I_D - V_{GS}) of the ZnO TFTs with different NbLaO annealing temperatures measured at a V_{DS} of 6 V, exhibiting quite different electrical properties. The threshold voltage (V_{th}) and saturation carrier mobility (μ_{sat}) are calculated from the plot of $I_D^{1/2}$ versus V_{GS} , based on the I - V equation of FET operating in the saturation region

$$I_D = \frac{W}{2L} \mu_{sat} C_i (V_{GS} - V_{th})^2, \quad (1)$$

where C_i is the capacitance per unit area of the gate insulator. The subthreshold swing (SS), defined as the gate-voltage change that makes the drain current increase by a factor of 10. From the I_D - V_{GS} curve, SS can be calculated

$$SS = \left(\frac{d \log(I_D)}{dV_{GS}} \right)^{-1}. \quad (2)$$

Based the SS value, the trap density (N_{it}) at/near the gate dielectric/ZnO interface can be calculated from

$$N_{it} = \left[\frac{SS \log(e)}{kT/q} - 1 \right] \frac{C_i}{q}, \quad (3)$$

where k is the Boltzmann's constant, T the temperature in Kelvin, and q the electron charge. Therefore, the electrical parameters of the devices can be readily extracted from the transfer curves and summarized in table 1. The sample with the annealing temperature of 200 °C shows higher saturation carrier mobility ($39.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) than those of the samples annealed at 300 °C and 400 °C, which are 20.5 and $10.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ respectively. One possible reason is that large amount of negative oxide charge in the NbLaO gate dielectric with low annealing temperature (as supported by larger V_{th}) can form a strong electric field to cause repel the electrons in the channel away from the NbLaO surface, thus resulting in weaker surface-roughness scattering for the electrons. Another possible explanation is that for no annealing or low annealing effect, the traps are uniformly distributed in the NbLaO gate dielectric and so have a small scattering effect

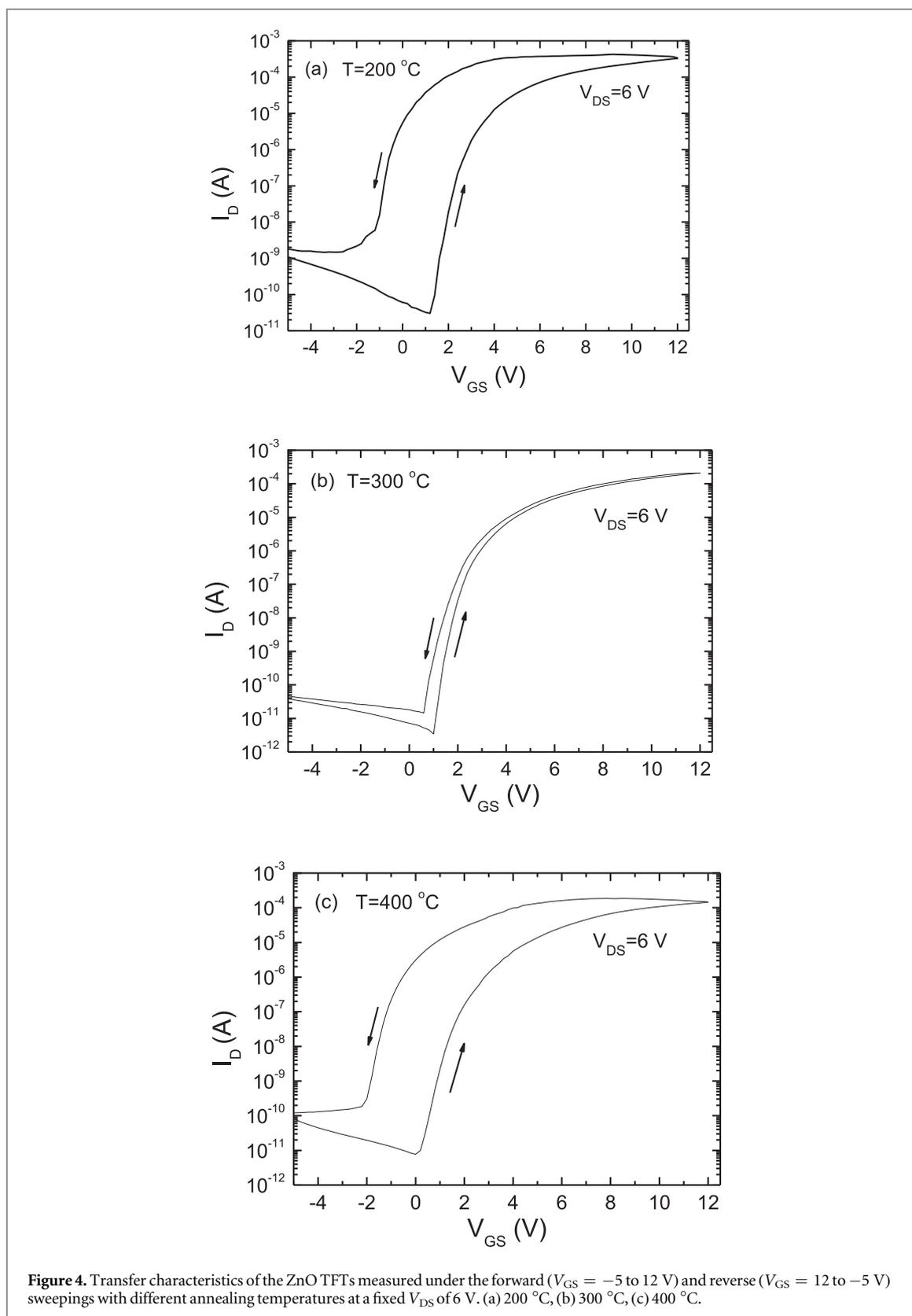
Table 1. Electrical parameters of the ZnO TFTs with NbLaO gate dielectric annealed at different temperatures.

Annealing temperature (°C)	200	300	400
μ_{sat} (cm ² V ⁻¹ s ⁻¹)	39.7	20.5	15.4
V_{th} (V)	2.7	2.5	2.4
SS (V/decade)	0.28	0.18	0.44
$I_{\text{on}}/I_{\text{off}}$ ($\times 10^7$)	1.08	6.25	1.34
I_{of} (pA)	30.3	3.4	7.6
C_{ox} (nF cm ⁻²)	85.7	98.5	91.6
t_{ox} (nm)	70	67	65
N_{it} ($\times 10^{12}$ cm ⁻²)	1.9	1.2	3.6
ΔV_{th} (V)	-2.95	-0.48	-2.72

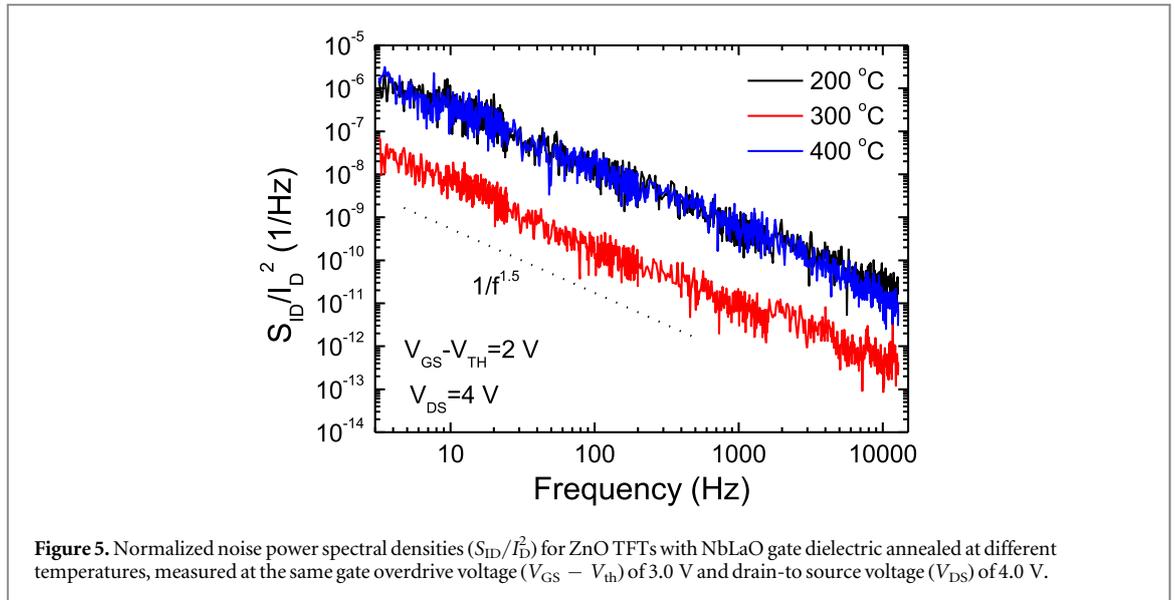
on the carriers in the channel. However, for relatively high annealing temperature, the traps are more concentrated at the NbLaO/ZnO interface, thus causing a decrease in carrier mobility due to more severe Coulomb scattering on the channel carriers [26]. On the other hand, V_{th} decreases weakly from 2.7 to 2.4 V with increasing annealing temperature from 200 °C to 400 °C, which is possibly due to two factors: one is the increase of C_i due to stronger densification of the NbLaO film during the annealing as listed in table 1; the other is that the negative oxide charges in the gate dielectric that can be reduced by annealing at higher temperature. In addition, the ZnO TFT annealed at 300 °C exhibits a smaller subthreshold slope (~ 0.18 V/decade) and a higher on/off current ratio ($\sim 6.25 \times 10^7$) than the other two samples. The high on/off current ratio is mainly originated from a low off-state current of 3.4 pA, which is an order of magnitude less than that of the sample annealed at 200 °C, and is two times lower than that of the sample annealed at 400 °C. The trap density at/near the gate-dielectric/ZnO interface can be estimated by equation (3) to be 1.6×10^{12} , 1.2×10^{12} and 3.6×10^{12} cm⁻² for the annealing temperature of 200 °C, 300 °C and 400 °C, respectively, indicating that the relatively good electrical performance of the ZnO-TFT with the annealing temperature of 300 °C is mainly attributed to the low trap density at/near the gate-dielectric/ZnO interface. In addition, the devices for the three annealing temperatures exhibit a low voltage operation (< 8 V), which is close to the results reported using Al₂O₃ and Ta₂O₅ gate dielectrics [11, 27], but is higher than that of HfLaO and ZrO₂ gate dielectrics [19, 20], implying that the electrical performances of the device need to be further optimized for the requirement of low power application in flexible and wearable electronics.

Figure 4 exhibits the hysteresis behavior of transfer characteristics under forward and reverse V_{GS} sweeps, and the threshold-voltage shifts ($\Delta V_{\text{th}} = V_{\text{th-reverse}} - V_{\text{th-forward}}$) of the samples with different NbLaO annealing temperatures are listed in table 1. It can be seen from figure 4 that there is an anticlockwise hysteresis phenomenon for the three samples, implying that there are donor-like deep traps at/near the NbLaO/ZnO interface of the three samples. During the forward V_{GS} sweep, the donor-like deep traps start to capture holes (i.e. minority carriers for ZnO channel) in the subthreshold region, thus generating a built-in electric field to enhance the external electric field and so accumulate more electrons in the channel during the reverse sweep. As a result, V_{th} is shifted in the negative direction to produce an anticlockwise hysteresis. However, it is notable that ΔV_{th} of the sample annealed at 300 °C (-0.48 V) is much smaller than those of the other two samples (-2.95 and -2.72 V) and close to or less than that of the ZnO TFTs with Al₂O₃ or Ta₂O₅ as gate dielectrics [27, 28]. The large ΔV_{th} of the sample annealed at 200 °C should be due to the stronger moisture absorption of the looser NbLaO film annealed at lower temperature [22]. The densification of the NbLaO film is improved with increasing annealing temperature to reduce the deep traps, oxide charge, and unsaturated bonds in the NbLaO gate dielectric. Therefore, the hysteresis phenomenon is effectively suppressed, together with smallest SS. However, for the annealing temperature of 400 °C, the hysteresis phenomenon becomes significant again. It indicates that, compared with the sample annealed at 300 °C, there are more donor-like deep traps near and at the NbLaO/ZnO interface which are likely originated from more indium diffused into the NbLaO gate dielectric from the ITO during annealing at a higher temperature, thus leading to the increases of I_{off} , SS and ΔV_{th} .

For further investigation on the interface properties of the TFTs, low frequency noise (LFN) measurements are performed. Figure 5 shows the normalized noise spectral density ($S_{\text{ID}}/I_{\text{D}}^2$) for the drain current of the samples, measured at the same gate overdrive voltage ($V_{\text{GS}} - V_{\text{th}}$) of 3.0 V and V_{DS} of 3.0 V. All the spectra show a monotonic decrease as frequency increases from 3.5 Hz to 100 kHz, and the LFN follows the $1/f^\gamma$ behavior for all three devices. However, the frequency exponent γ values are about 1.5, much larger than 1. Moreover, the normalized noise of the sample annealed at 300 °C is about two orders of magnitude lower than that those of the other two samples. It is well known that the exponent of $1/f^\gamma$ behavior in the noise spectral density is closely related to location of the Fermi level, trap distribution, and available energy states within the bandgap of the semiconductor. Christensson *et al* explained that the power spectral density shows exact $1/f$ behavior only for dominant oxide traps with uniform distributions over space and energy because only traps around the Fermi



level are involved in the noise generation process and traps with different lifetimes are equally distributed [29]. However, if the distribution of traps is not uniform, the spectral density will deviate from the ideal $1/f$ behavior. Based on this, the results here can be explained as following. When the ZnO TFTs operate in the saturation mode, the channel region near the drain is in depletion due to the high drain bias, and so the Fermi level near the drain region is located near mid-gap. Since the traps near the Fermi level are the only active traps for noise generation, only deep traps participate in the fluctuation of carrier number. Since trapping and detrapping by deep traps require longer time than that by shallow traps, carriers trapping and detrapping correlated with



longer lifetime becomes more dominant, and thus the noise level in the low frequency region increases, resulting in the frequency exponent γ values larger than 1.

According to the McWhorter model for the $1/f$ noise of MOSFETs, the trap density can be estimated as [30]

$$N_t = S_V \frac{fWLC_i^2}{\lambda kTq^2}, \quad (4)$$

where T is absolute temperature, λ the tunneling parameter conventionally assumed to be 0.1 nm, N_t the trap density, and $S_V = S_{ID}/g_m^2$, with g_m the transconductance. Furthermore, N_t can be calculated from figures 3 and 5 to be $6.9 \times 10^{22} \text{ cm}^{-3} \text{ eV}^{-1}$, $1.2 \times 10^{21} \text{ cm}^{-3} \text{ eV}^{-1}$, and $8.8 \times 10^{22} \text{ cm}^{-3} \text{ eV}^{-1}$ at a frequency of 100 Hz for the samples annealed at 200 °C, 300 °C and 400 °C, respectively. Therefore, this further supports that the relatively good electrical properties of the sample annealed at 300 °C are mainly attributed to the reduction of deep traps in the high- k gate dielectric and at the gate-dielectric/semiconductor interface.

4. Conclusions

The electrical characteristics of ZnO-TFTs with NbLaO gate dielectric annealed at different temperatures (200 °C, 300 °C and 400 °C) are investigated. The sample annealed at 300 °C exhibits the relatively better electrical properties. The mobility, on/off ratio, subthreshold slope, off-state current and interface-state density are $20.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, 6.25×10^7 , 180 mV dec⁻¹, 3.4 pA and $1.2 \times 10^{12} \text{ cm}^{-2}$, respectively, and there is a slight hysteresis phenomenon in the transfer characteristics. The optimized performance is mainly attributed to reduced deep traps in the high- k gate dielectric or at gate-dielectric/semiconductor interface. The optimized device is suitable for low power applications such as flexible and wearable electronics.

Acknowledgments

This work is supported by the Natural Science Foundation of Guangdong province (Project No. 2016A030313474), the National Natural Science Foundation of China (Project No. 61604057), Science and Technology Program of Guangdong Province (Project No. 2016B090906002), and the Research Grants Council, Hong Kong (Project No. HKU 17203814).

ORCID iDs

R S Chen  <https://orcid.org/0000-0002-7247-8420>

References

- [1] Fortunato E, Barquinha P and Martins R 2012 *Adv. Mater.* **24** 2945
- [2] Liu X X, Wegener M, Polster S, Jank M P M, Roosen A and Frey L 2016 *J. Disp. Technol.* **12** 214

- [3] Nayak P K, Wang Z and Alshareef H N 2016 *Adv. Mater.* **28** 7736
- [4] Fortunato E, Barquinha P, Pimentel A, Gonçalves A, Marques A, Martins R and Pereira L 2004 *Appl. Phys. Lett.* **85** 2541
- [5] Wang B S, Li Y S and Cheng I C 2016 *IEEE Trans. Electron Devices* **63** 1545
- [6] Chen R S, Zhou W, Zhang M and Kwok H S 2012 *Thin Solid Films* **520** 6681
- [7] Oh B Y, Kim Y H, Lee H J, Kim B Y, Park H G, Han J W, Heo G S, Kim T W, Kim K Y and Seo D S 2011 *Semicond. Sci. Technol.* **26** 085007
- [8] Hwang C S, Park S H K, Oh H, Ryu M K, Cho K I and Yoon S M 2014 *IEEE Electron Device Lett.* **35** 360
- [9] Bayraktaroglu B, Leedy K and Neidhard R 2008 *IEEE Electron Device Lett.* **29** 1024
- [10] Yoshida T, Tachibana T, Maemoto T, Sasa S and Inoue M 2010 *Appl. Phys. A* **101** 685
- [11] Esro M, Vourlias G, Somerton C, Milne W I and Adamopoulos G 2015 *Adv. Funct. Mater.* **25** 134
- [12] Hwang J, Park J and Kim H 2014 *Semicond. Sci. Technol.* **29** 095019
- [13] Han D D, Chen Z F, Cong Y Y, Yu W, Zhang X and Wang Y 2016 *IEEE Trans. Electron Devices* **63** 3360
- [14] Ji L W, Wu C Z, Fang T H, Hsiao Y J, Meen T H, Water W, Chiu Z W and Lam K T 2013 *IEEE. Sens. J.* **13** 4940
- [15] Nayak P K, Jang J, Lee C and Hong Y 2010 *J. Soc. Inf. Disp.* **18** 552
- [16] Alshammari F H, Nayak P K, Wang Z W and Alshareef H N 2016 *ACS Appl. Mater. Interfaces* **8** 22751
- [17] Wang Y H, Ma Q, Zheng L L, Liu W J, Ding S J, Lu H L and Zhang D W 2016 *IEEE Trans. Electron Devices* **23** 1893
- [18] Brox-Nilsen C, Jin J, Luo Y, Bao P and Song A 2013 *IEEE Trans. Electron Devices* **60** 3424
- [19] Su N C, Wang S J and Chin A 2010 *Electrochem. Solid-State Lett.* **13** H8
- [20] Zeumault A and Subramanian V 2016 *Adv. Funct. Mater.* **26** 955
- [21] Kim S J, Cho B J, Bin Yu M, Li M F, Xiong Y Z, Zhu C X, Chin A and Kwong D L 2005 *IEEE Electron Device Lett.* **26** 625
- [22] Kukli K, Ritala M and Leskelä M 2001 *J. Electrochem. Soc.* **148** F35
- [23] Song J Q, Han C Y and Lai P T 2016 *IEEE Trans. Electron Devices* **63** 1928
- [24] Park C J, Kim Y W, Cho Y J, Bobade S M, Choi D K and Lee S B 2009 *J. Korean Phys. Soc.* **55** 1925
- [25] Kim J J, Lee J H, Bak J Y, Kim H S, Jang N W, Lee W J and Cho C R 2010 *J. Korean Phys. Soc.* **56** 404
- [26] Sah C T, Ning T H and Tschopp L L 1972 *Surf. Sci.* **32** 561
- [27] Zhang L, Li J, Zhang X W, Yu D B, Jiang X Y and Zhang Z L 2010 *Phys. Status Solidi a* **207** 1815
- [28] Alshammari F H, Nayak P K, Wang Z W and Alshareef H N 2016 *ACS Appl. Mater. Interfaces* **8** 22751
- [29] Christensson S, Lundström I and Svensson C 1968 *Solid-State Electron.* **11** 797
- [30] Rumyantsev S L, Jiang C L, Samnakay R, Shur M S and Balandin A A 2015 *IEEE Electron Devices Lett.* **36** 517