# Effects of thermal annealing on $La_2O_3$ gate dielectric of InGaZnO thin-film transistor

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**Abstract:** The effects of thermal annealing on $La_2O_3$ gate dielectric of InGaZnO thin-film transistor (TFT) are investigated by varying annealing temperature. Due to densification and enhanced moisture resistance of the $La_2O_3$ film, its surface roughness and interface with InGaZnO are improved by the thermal annealing, thus leading to significant improvement in the TFT electrical performance. However, higher-temperature (450 $^oC$) annealing deteriorates the dielectric roughness and induces more traps associated with grain boundaries in the $La_2O_3$ film. The TFT with an appropriate annealing (350 $^oC$) shows the best performance with smallest sub-threshold swing (0.276 V/dec), lowest threshold voltage (3.01 V), highest field-effect mobility (23.2 $cm^2/V.s$) and largest on-off current ratio ($3.52\times10^8$).

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Compared with conventional Si-based thin-film transistors (TFT), InGaZnO TFTs have advantages including low processing temperature, high field-effect mobility as well as good uniformity, and thus have received intensive attention over the last decade. [1] Recently, high-*k* dielectrics, such as $Ta_2O_5$, $HfO_2$, $ZrO_2$, AlZrO and $Lu_2O_3$, have been widely investigated to replace $SiO_2$ or $Si_3N_4$ as gate dielectrics in InGaZnO TFTs for improving their driving ability and reducing their operating voltage and power consumption. [2-6] Among various high-*k* materials, $La_2O_3$ displays high dielectric constant (~ 30), large band gap (~ 6.0 eV) and good thermodynamic stability with InGaZnO, and thus should be a promising candidate as the gate dielectrics of InGaZnO TFTs. [7,8] It has been demonstrated that Ta incorporated in $La_2O_3$ (LaTaO) can further improve the TFT performance by suppressing moisture absorption of the $La_2O_3$ film; however, the TFT performance is quite sensitive to Ta content in the LaTaO film, thus leading to uniformity issues. [8] It must be noted that not only the dielectric itself but also the thermal treatment plays a key role in the device performance. Therefore, this work aims to study the thermal and electrical characteristics of InGaZnO TFTs with $La_2O_3$ gate dielectric prepared at different annealing temperatures.

TFT devices with bottom-gate top-contact configuration were fabricated on heavily p-type Si substrate. The substrate was cleaned by a standard RCA cleaning: firstly, the substrate was submerged in solution I ($H_2O$:$H_2O_2$:$NH_4OH$=5:1:1) at 80 $^oC$ for 10 min to remove organics and particles; then, the substrate was cleaned in solution II ($H_2O$:$H_2O_2$:HCl=5:1:1) at 80 $^oC$ for 10 min to remove metallic contaminants; finally, the substrate was dipped in 2% hydrofluoric acid for 1 min to remove native oxide. After the cleaning, 40-nm $La_2O_3$ was deposited on the substrate by radio-frequency sputterer using a $La_2O_3$ target in an Ar/$O_2$ ambient. Then, the samples were divided into four groups: two of the groups went through post-deposition annealing (PDA) in $N_2$ at 350 $^oC$ and 450 $^oC$ for 10 min respectively, denoted as LaO_350 and LaO_450 samples; the third and fourth groups did not receive PDA，denoted as the as_deposited and control samples respectively. Following that, a 60-nm IGZO active layer was deposited by sputterer using an InGaZnO target in an Ar/$O_2$ ambient. Then, source/drain (S/D) electrodes consisting of 20-nm Ti/80-nm Au were formed by electron-beam evaporation combined with lift-off technique, where Ti was used to enhance the electrode adhesion and also reduce the barrier height between the electrodes and InGaZnO. The channel width (*W*) and length (*L*) were 100 μm and 20 μm

respectively. Finally, the LaO_350, LaO_450 and control samples received a post-metallization annealing (PMA) in forming gas ($H_2/O_2$=5%/95%) at 350 $^oC$ for 20 min to improve the electrical contacts. The samples with different annealing conditions are summarized in Table 1.

Fig. 1 shows the X-ray diffraction (XRD) patterns of the samples with various annealing conditions measured under theta-theta mode, where all the samples display a polycrystalline structure and consists of $La_2O_3$ and $La(OH)_3$ in the $La_2O_3$ film. $La(OH)_3$ is formed by the reaction of $La_2O_3$ with moisture due to the hydroscopic nature of $La_2O_3$. [8] For the LaO_350 and LaO_450 samples, the peak (3 1 1) of $La(OH)_3$ decreases significantly relative to that of the sample with no PDA, indicating suppressed formation of $La(OH)_3$ and thus enhanced moisture resistance of $La_2O_3$ by the thermal annealing. In addition, compared with the LaO_350 sample, the intense peak (1 1 0) attributed to $La_2O_3$ component for the LaO_450 sample exhibits stronger intensity and smaller FWHM (full width at half maximum), indicating more crystallized structure with larger grain size and more grain boundaries induced by the higher-temperature annealing. Moreover, compared with the LaO_350 sample, the more grain boundaries in the LaO_450 one facilitate the diffusion of moisture in the dielectric film, thus enhancing the formation of $La(OH)_3$.

Fig. 2 shows the atomic force microscopy (AFM) images of the samples, where the root-mean-square (RMS) roughness is 1.39 nm, 0.90 nm and 1.11 nm for the as_deposited, LaO_350 and LaO_450 samples respectively. Both of the LaO_350 and LaO_450 samples have smoother surface than the as_deposited one because of densification as well as enhanced moisture resistance of the $La_2O_3$ film induced by the thermal annealing, which is helpful to suppress the volume expansion of the $La_2O_3$ film caused by moisture absorption and thus the formation of $La(OH)_3$. [8] Moreover, the rougher surface of the LaO_450 sample than the LaO_350 one is mainly ascribed to larger grain size induced by the higher-temperature annealing.

Fig. 3 shows the transfer characteristics of the devices. The sub-threshold swing *SS*, saturation carrier mobility $\mu_{sat}$, threshold voltage $V_{th}$, on-current $I_{on}$ (defined as $I_D$ at $V_G$ = 10 V and $V_D$ = 5 V) and on-off current ratio $I_{on}/I_{off}$ of the devices are extracted from Fig. 3 and summarized in Table 2. In terms of the parameters listed in Table 2, the control sample shows better performance than the as_deposited one mainly due to the improved electrical contacts and InGaZnO film by PMA. Moreover, the LaO_350 and LaO_450 samples exhibit much better performance than the control one, suggesting that PDA plays a key role in the device performance.

The smaller *SS* of the LaO_350 and LaO_450 samples (LaO_350 ~ 0.276 V/dec; LaO_450 ~ 0. 411V/dec) than the control one (~ 2.11 V/dec) suggests fewer interface states at the dielectric/semiconductor interface, demonstrating that the thermal annealing can effectively improve the interface quality by densifying the dielectric film and improving the interface roughness. Additionally, for the LaO_350 and LaO_450 samples, the better dielectric /semiconductor interface with fewer interface states can suppress the trapping of charge carriers and the trap-related scattering of charge carriers in the conduction channel, thus resulting in lower $V_{th}$ (LaO_350 ~ 3.01 V; LaO_450 ~ 4.01 V; control ~ 5.00 V) and higher $\mu_{sat}$ (LaO_350 ~ 23.2 $cm^2$/V.s; LaO_450 ~ 5.63 $cm^2$/V.s; control ~ 2.11 $cm^2$/V.s) than the control one. Moreover, it is known that the by-product $La(OH)_3$ formed by the reaction of $La_2O_3$ with moisture increases the negative charge in the dielectric film due to $OH^-$ replacing $O^{2-}$. [9] This increased negative charge density in the dielectric film screens the electric field from the gate, and thus larger gate voltage is required to induce a conduction channel; also, the increased charge density can induce Coulombic scattering on the charge carriers, thus degrading $\mu_{sat}$. Consequently, the suppressed formation of $La(OH)_3$ for the LaO_350 and LaO_450 samples further contributes to their lower $V_{th}$ and higher $\mu_{sat}$. Owing to the lower $V_{th}$ and higher $\mu_{sat}$, the LaO_350 and LaO_450 samples achieve much higher $I_{on}$ (LaO_350 ~ 495 μA; LaO_450 ~ 118 μA) than that of the control one (~ 24.7 μA). Moreover, the higher $I_{on}$ and suppressed off-state leakage path by thermal annealing of the LaO_350 and LaO_450 samples lead to higher $I_{on}/I_{off}$ ratio (LaO_350 ~ $3.52\times10^8$; LaO_450 ~ $4.29\times10^6$) than the control one (~ $1.72\times10^6$). The control sample displays much larger current under negative $V_G$ than the other samples. For the control sample, the PMA would lead to Ti diffusion in the gate dielectric film, thus degrading the quality of the dielectric film and resulting in large leakage current under negative $V_G$. [10] The as_deposited sample did not receive PMA, thus leading to smaller leakage under negative $V_G$ than the control one. Although the LaO_350 and LaO_450 samples received the same PMA as the control one, the PDA before the PMA could densify the dielectric film, thus suppressing the Ti diffusion in the dielectric film. Therefore, they also have smaller leakage than the control one. The above analysis needs to be further confirmed. Compared with the LaO_350 sample, the LaO_450 one with higher annealing temperature displays worse performance mainly due to larger grains formed in the dielectric at higher annealing temperature, resulting in more traps along the grain boundaries as well as degraded

dielectric/semiconductor interface associated with rougher dielectric film (shown in AFM results in Fig. 2). [7] Therefore, it is believed that the superior performance of the LaO_350 sample is mainly ascribed to the high quality of both the dielectric bulk itself and its interface with the semiconductor achieved by appropriate annealing temperature. Moreover, the LaO_350 sample displays similar $\mu_{sat}$ (~ 23.2 $cm^2$/V.s) as that (~ 23.4 $cm^2$/V.s) of the TFT with LaTaO gate dielectric, but much higher $I_{on}/I_{off}$ ratio (~ $3.52\times10^8$) than the latter (~ $2.60\times10^7$), demonstrating that the appropriate annealing is an effective way to improve the TFT performance. [8]

Fig. 4(a) shows the $V_{th}$ shift ($\Delta V_{th}$) of the samples as a function of stress time under positive gate-bias stress (PGBS). The $V_{th}$ of the control sample exhibits a positive shift with increasing stress time. However, the LaO_350 sample displays a positive $V_{th}$ shift initially, but then a negative $V_{th}$ shift with the stress time. There are two mechanisms responsible for $V_{th}$ shift under PGBS: electrons move towards the InGaZnO/dielectric interface and are trapped at the interface (denoted as electron trapping), leading to reduced electrons in the InGaZnO film and thus positive $V_{th}$ shift; On the other hand, adsorbed $H_2O$ molecules on the back channel can act as donors (denoted as electron injection), resulting in increased electrons in the InGaZnO film and thus negative $V_{th}$ shift. [11] It is known that $OH^-$ group at dielectric interface usually acts as electron trap. [12] Due to severer moisture absorption of the $La_2O_3$ film for the control sample, it has much more $OH^-$ groups than the LaO_350 one. Therefore, electron trapping at the dielectric/semiconductor interface is dominant over electron injection from the back channel under PGBS for the control sample, thus leading to the continual positive $\Delta V_{th}$ with the stress time and severer $V_{th}$ instability. For the LaO sample, the insertion of a passivation layer between the InGaZnO and ambient should effectively suppress the $V_{th}$ instability by blocking the $H_2O$ adsorption on the back channel. Fig. 4(b) shows the output characteristics of the LaO_350 sample, where a high drain current of 534 μA can be obtained with the device biased at $V_G$ = 10 V and $V_D$ = 6V, demonstrating its strong driving ability for high-speed applications. The current crowding at low $V_D$ should be due to parasitic resistance from the source/drain contacts. [13]

In summary, the impact of thermal annealing on $La_2O_3$ gate dielectric of InGaZnO TFT has been studied. Compared with the TFT with no or higher-temperature (450 $^oC$) PDA, the one with suitable annealing temperature (350 $^oC$) displays better electrical performance mainly due to smoother dielectric/semiconductor interface with fewer interface states as well as higher quality of

the bulk dielectric film with lower charge density and fewer grain boundaries. Therefore, $La_2O_3$ film with appropriate thermal annealing is a promising gate dielectric for high-performance InGaZnO TFT.

Acknowledgments This work was financially supported by the Natural Science Foundation of Jiangsu Province (No. BK20140639), the Fundamental Research Funds for the Central Universities (No. 2242014K10016), RGC of HKSAR, China (No. HKU 17203814) and the University Development Fund (Nanotechnology Research Institute, No. 00600009) of the University of Hong Kong.

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**Captions**

Fig. 1. XRD patterns of the $La_2O_3$ films on the Si substrate with various annealing temperatures, where the diffraction peaks are also indexed (JCPDS No. 40－1281; 06－0588).

Fig. 2. AFM images of the $La_2O_3$ films on the Si substrate with various annealing temperatures: (a) as-depostied, (b) 350 $^oC$ and (c) 450 $^oC$.

Fig. 3. Transfer characteristics of the TFTs with various annealing conditions.

Fig. 4. (a) $\Delta V_{th}$ of the control and LaO_350 samples as a function of stress time under PGBS ($V_{GS}$=+7 V, $V_{DS}$=0 V). (b) Output characteristics of the LaO_350 sample.

Table 1. Comparison of the annealing conditions for each sample

| Sample | As_deposited | Control | LaO_350 | LaO_450 |
|---|---|---|---|---|
| **PDA** | no | no | 350 $^{o}$C, 10 min | 450 $^{o}$C, 10 min |
| **PMA** | no | 350 $^{o}$C, 20 min | 350 $^{o}$C, 20 min | 350 $^{o}$C, 20 min |

Table 2. Key parameters extracted from the transfer characteristics in Fig. 3 for the TFTs.

| **Sample** | **As_deposited** | **Control** | **LaO_350** | **LaO_450** |
|---|---|---|---|---|
| **SS (V/dec)** | 0.456 | 0.454 | 0.276 | 0.411 |
| **$\mu_{sat}$ ($cm^2$/V.s)** | 0.623 | 2.11 | 23.2 | 5.63 |
| **$V_{th}$ (V)** | 5.22 | 5.01 | 3.01 | 4.02 |
| **$I_{on}$ (μA)** | 5.13 | 24.7 | 495 | 118 |
| **$I_{on}/I_{off}$** | $8.44\times10^5$ | $1.72\times10^6$ | $3.52\times10^8$ | $4.29\times10^6$ |

Fig. 1
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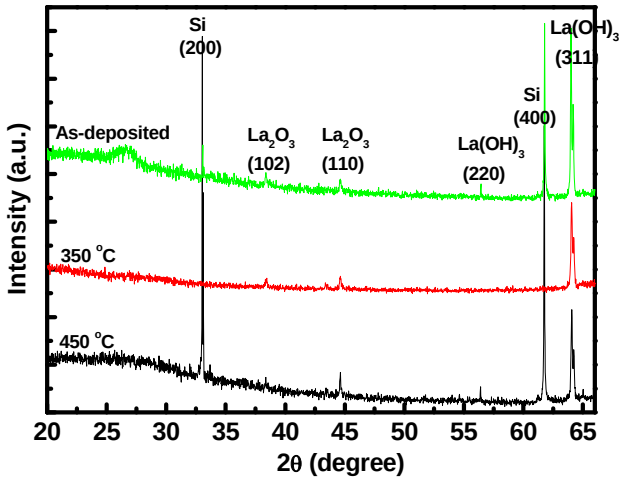

Fig. 2
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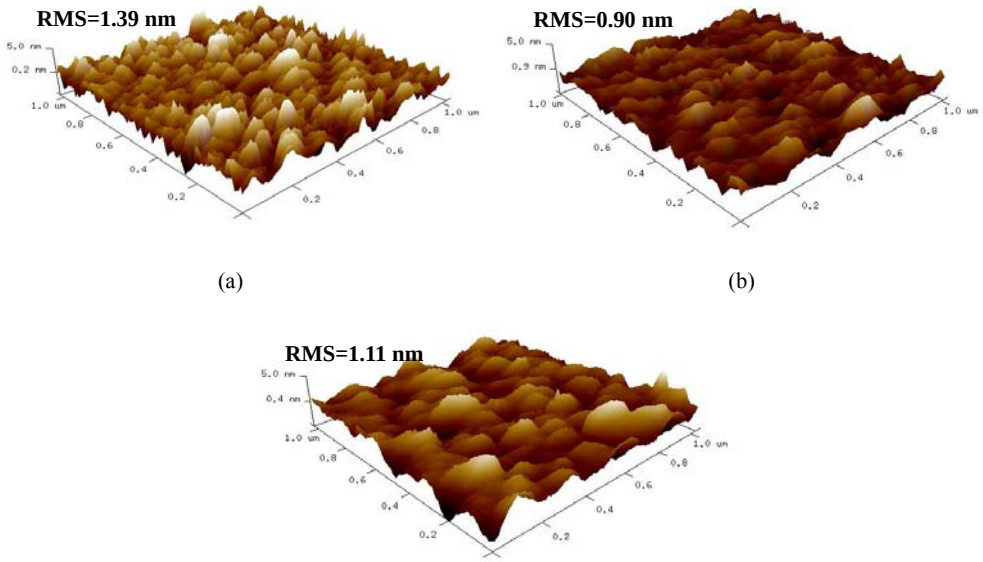


(a) (b)

(c)

Fig. 3
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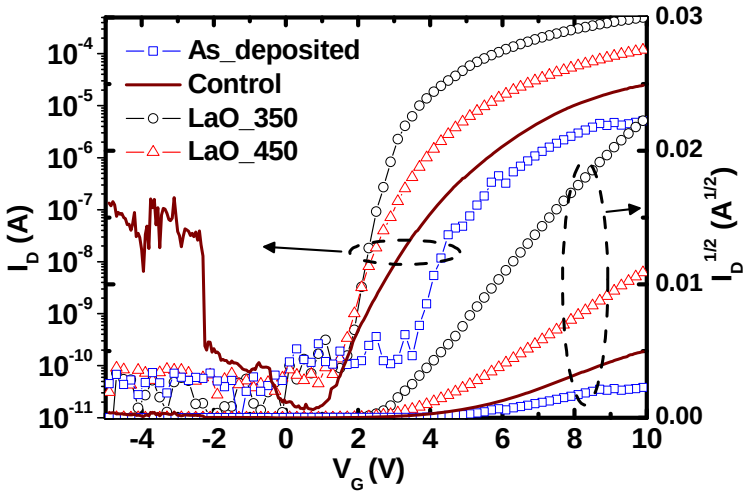

Fig. 4
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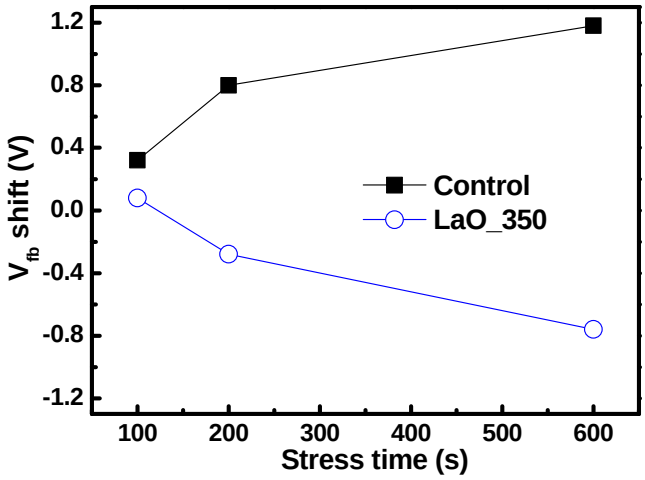
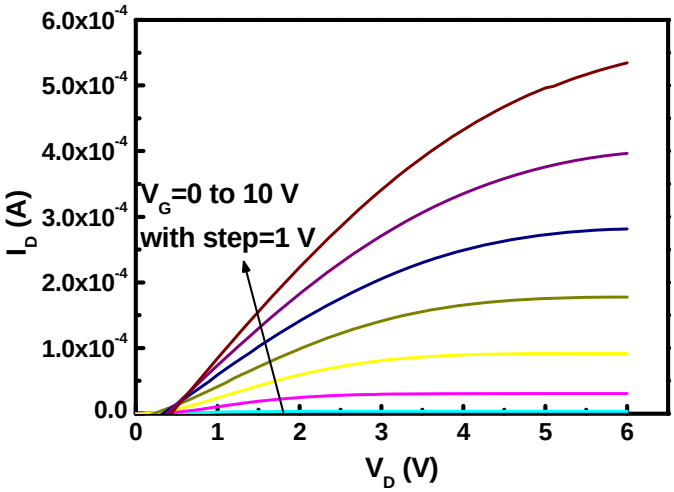



(a)




(b)