Charge-trapping characteristics of fluorinated thin ZrO_2 film for nonvolatile memory applications

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(Received 26 January 2014; accepted 15 April 2014; published online 24 April 2014)

The effects of fluorine treatment on the charge-trapping characteristics of thin ZrO_2 film are investigated by physical and electrical characterization techniques. The formation of silicate interlayer at the ZrO_2/SiO_2 interface is effectively suppressed by fluorine passivation. However, excessive fluorine diffusion into the Si substrate deteriorates the quality of the SiO_2/Si interface. Compared with the ZrO_2-based memory devices with no or excessive fluorine treatment, the one with suitable fluorine-treatment time shows higher operating speed and better retention due to less resistance of built-in electric field (formed by trapped electrons) against electron injection from the substrate and smaller trap-assisted tunneling leakage, resulting from improved ZrO_2/SiO_2 and SiO_2/Si interfaces. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4873388]

Metal-oxide-nitride-oxide-silicon (MONOS)-type nonvolatile memory with discrete traps in the dielectric for charge storage is considered as a promising candidate to replace its floating-gate counterpart due to stronger scaling ability and higher reliability. Recently, high-k dielectrics have been proposed instead of conventional Si_3N_4 as charge-trapping layer (CTL) to achieve lower operating voltage and higher charge-trapping efficiency.[1–8] Among various high-k dielectrics, Hf-based oxides (e.g., HfO_2 and HfON) have been extensively investigated as CTL mainly because of its large conduction-band offset relative to SiO_2 ($\Delta E_c \sim 2.0$ eV), high k value (~22), and compatibility with CMOS processing.[2–4] On the other hand, ZrO_2 shows similar dielectric properties as HfO_2 but has higher k value (~37).[5] Consequently, there is an increasing interest in exploring ZrO_2 as CTL.[5,6] Wu *et al*. studied the charge-trapping characteristics of ZrO_2 with and without nitridation and found that MONOS device with nitrided ZrO_2 showed better performance than that without nitridation due to nitrogen passivation of the ZrO_2 film.[5] Besides nitrogen, fluorine is also an excellent passivant to remove oxide defects and strengthen the dielectric films due to its very high electronegativity.[9] Therefore, fluorination is an effective way to improve the charge-trapping characteristics of dielectrics.[7,8] In this work, based on MONOS capacitors, the charge-trapping characteristics of ZrO_2 with and without fluorine incorporation are studied. Detailed analysis of fluorine treatment on the device performance is also carried out.

MONOS capacitors with $Al/Al_2O_3/ZrO_2/SiO_2/Si$ were fabricated on p-type (100) substrate. After the standard RCA cleaning, 2-nm SiO_2 tunneling oxide was grown on the wafers by thermal dry oxidation. Then 3-nm ZrO_2 was deposited on the SiO_2 by sputtering using a Zr target in an Ar/O_2 (8/1) mixed ambient. Following that, some samples were treated by a $CHF_3 + O_2$ (10 SCCM/1 SCCM) plasma at 20 W for 150 s and 400 s, respectively. The low-concentration O_2 was used to remove the carbon and hydrogen in the plasma.[10] Then, 15-nm Al_2O_3 was deposited by atomic layer deposition using trimethyl-aluminum ($Al(CH3)_3$) and H_2O as precursors at 300 °C. Following that, all the samples went through a post-deposition annealing in N_2 at 900 °C for 30 s. Finally, Al was evaporated and patterned as gate electrodes followed by a forming-gas annealing at 300 °C for 20 min. The sample without fluorine treatment was denoted as ZrO, while the samples with 150-s and 400-s fluorine treatment were denoted as LF-ZrO and HF-ZrO, respectively. In addition, $Al/Al_2O_3/SiO_2/Si$ (denoted as MAOS) and $Al/ZrO_2/SiO_2/Si$ (denoted as MNOS) capacitors were also fabricated by the same process to study the charge-trapping characteristics of the ZrO_2 film. The physical properties of the films with and without fluorine treatment were analyzed by transmission electron microscopy (TEM), secondary ion mass spectroscopy (SIMS), and X-ray photoelectron spectroscopy (XPS). The electrical characteristics of the devices were measured by HP4284A LCR meter and HP4156A semiconductor parameter analyzer.

Fig. 1 shows the cross-sectional TEM image of the MONOS capacitors with and without the fluorine treatment, where the physical thickness remains the same after the fluorine treatment, indicating negligible etching of the ZrO_2 film due to the low energy of the fluorine plasma treatment. Fig. 2(a) displays the SIMS depth profile of the samples with various fluorine-treatment times to evaluate the fluorine distribution. It is clear that fluorine is mainly located in the ZrO_2/SiO_2 stack and decreases rapidly in the Si substrate, indicating strong fluorine passivation in the ZrO_2/SiO_2 stack. Also, the fluorine atoms diffuse more into the Si substrate for longer fluorine-treatment time. This is consistent with the XPS data in Fig. 2(b), where the Si 2p spectrum from the substrate for the HF-ZrO sample shifts to higher binding energy by 0.05 eV relative to those for the ZrO and LF-ZrO samples, implying the formation of Si-F bonds. Fig. 2(c) shows the Zr 3d spectrum combined with curve-fitting lines. For the ZrO sample, the Sr 3d spectrum displays distinct doublet at 184.7 eV (Zr $3d_{3/2}$) and 182.3 eV (Zr $3d_{5/2}$), agreeing with Zr–O bonding in the ZrO_2 film.[11] After the fluorine treatment,

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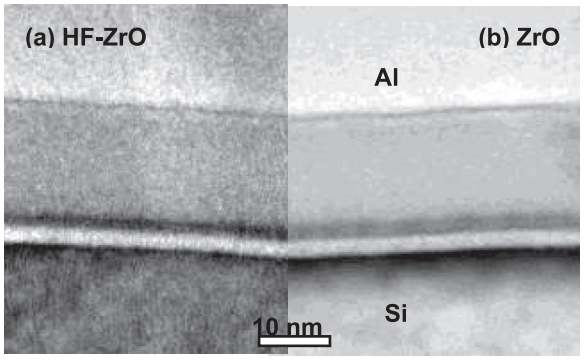

FIG. 1. Cross-sectional TEM image for (a) the HF-ZrO and (b) ZrO MONOS capacitors.

the spectrum shifts to higher binding energy by 0.5 eV, indicating that F is bonded with Zr. Moreover, the Zr spectrum can be decomposed into two components, corresponding to ZrO_2 (182.3 eV for Zr $3d_{5/2}$) and Zr silicate formed by the ZrO_2/SiO_2 interfacial reaction (182.7 eV for Zr $3d_{5/2}$). Compared with the ZrO sample, the much smaller area of the silicate component for the LF-ZrO and HF-ZrO samples indicates negligible formation of the Zr silicate interlayer due to sufficient fluorine passivation. The formation of the interlayer consumes the SiO_2 tunneling oxide, and also it has smaller bandgap (~6.6 eV) and more defects than thermally grown SiO_2 (~8.9 eV).[12,13] Therefore, an abrupt interface without interlayer is desirable for good data retention.[14]

Fig. 3(a) displays the C-V loops under ±8 MV/cm sweeping for the MAOS and MNOS samples. The trapped-charge density (Q_{ox}) in the device can be calculated by the expression below

$$Q_{ox} \approx \frac{\Delta V_{FB} C_{ox}}{q}, \quad (1)$$

where ΔV_{FB} is the memory window from the C-V loops, C_{ox} is the capacitance density of the samples, and q is the electron charge. The Q_{ox} for the MAOS and MNOS samples is about $3.5 \times 10^{10}\,cm^{-2}$ and $1.1 \times 10^{12}\,cm^{-2}$, respectively. The much higher Q_{ox} for the MNOS sample than that for the MAOS one at the same operating condition indicates that the charge-trapping site is mainly in the ZrO_2 layer. In addition, compared with the MAOS sample with counterclockwise hysteresis loop, the MNOS one exhibits a clockwise hysteresis loop, suggesting that charges inject from the Al electrode into the ZrO_2 layer at the forward sweeping (from −8 MV/cm to +8 MV/cm) mainly due to the smaller barrier height at the Al/ZrO_2 interface ($\Delta E_C \sim 1.6$ eV for Al/ZrO_2; ~3.0 eV for Al/Al_2O_3).[15] Fig. 3(b) depicts the 1-MHz C-V hysteresis loops of the MONOS devices, where the memory window for the ZrO, LF-ZrO, and HF-ZrO samples is 4.8 V, 3.8 V, and 5.1 V, respectively. The smaller window for the LF-ZrO sample than the ZrO sample is due to the suppressed formation of interlayer by fluorine passivation,[13] while the largest window for the HF-ZrO sample suggests extra traps generated by excessive fluorine treatment. The C-V curve of the HF-ZrO sample shows more severe stretch-out characteristic than the ZrO and LF-ZrO samples, implying its higher interface-state density (D_{it}) at the SiO_2/Si interface. Using the Terman's method,[16] the HF-ZrO sample has an extracted D_{it} of $7.4 \times 10^{12}\,cm^{-2}$, corresponding to 8.8% and 17.5% higher than the ZrO sample ($6.8 \times 10^{12}\,cm^{-2}$) and the LF-ZrO sample (6.3×10^{12} cm^2), respectively. Appropriate fluorine incorporation can passivate the SiO_2/Si interface,

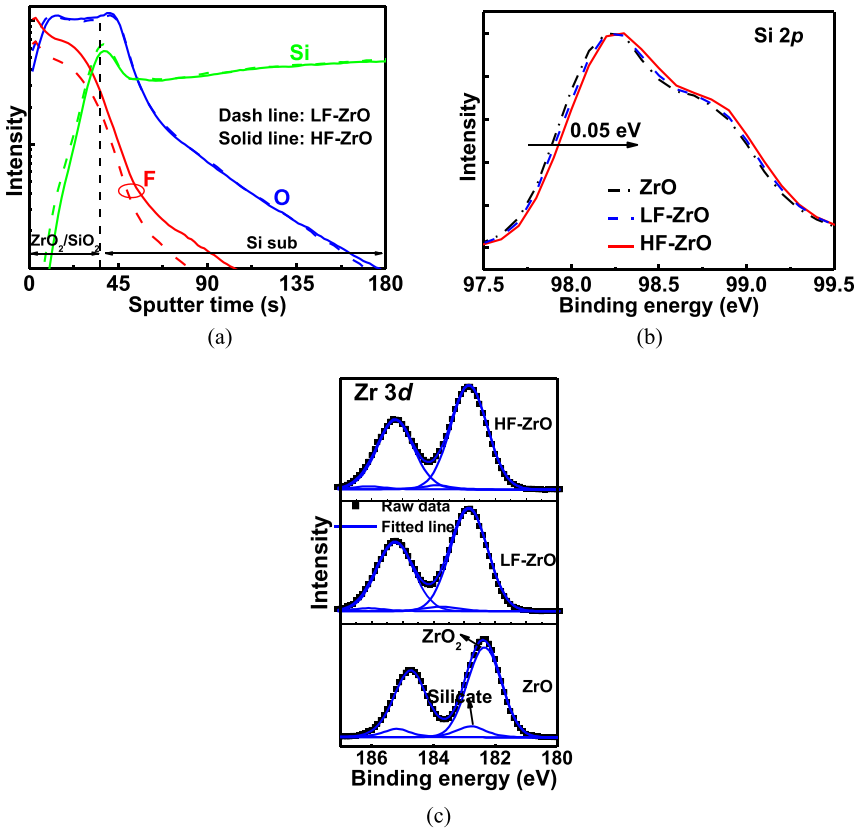

FIG. 2. (a) SIMS depth profile of ZrO_2/SiO_2 on Si substrate with various fluorine treatments. (b) XPS Si 2*p* spectrum and (c) XPS Zr 3*d* spectrum for the samples with and without fluorine treatments.

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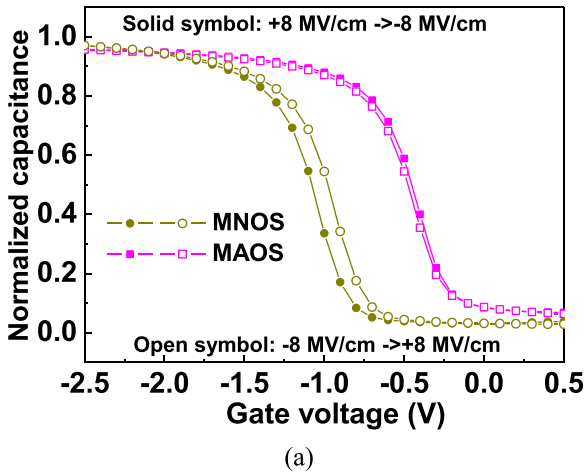

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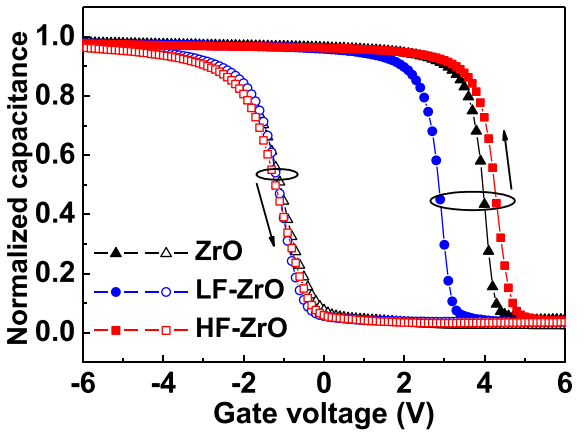
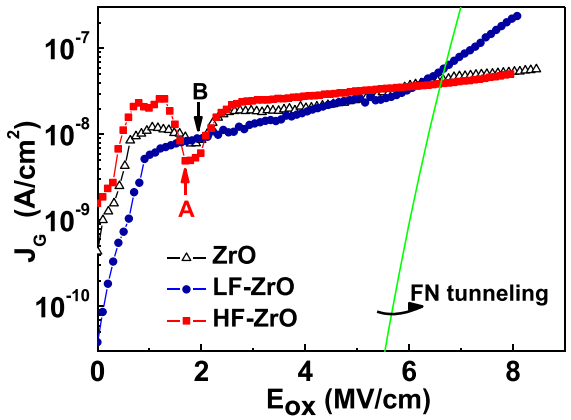


(b)

FIG. 3. (a) 1-MHz C-V loops of the MNOS and MAOS devices under ±8 MV/cm sweeping; (b) 1-MHz C-V loops of the MONOS devices under ±12 V sweeping.



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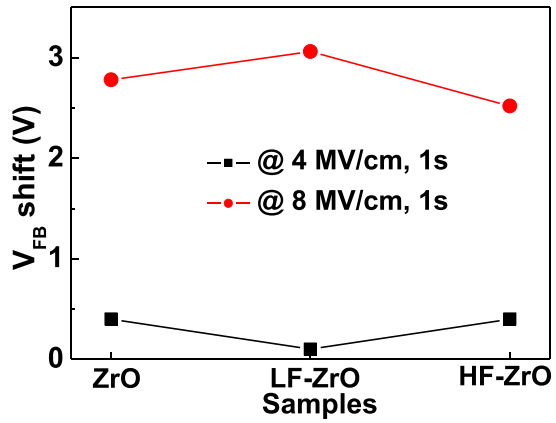

(b)

FIG. 4. (a) J_G as a function of E_{OX} for the MONOS capacitors. The simulated FN tunneling current through SiO_2 tunneling oxide is also shown. (b) V_{FB} shift at low (~4 MV/cm) and high (~8 MV/cm) E_{OX}. V_{FB} shift is defined as $V_{FB} - V_{FB0}$, where V_{FB} is the flat-band voltage under stress, and V_{FB0} is the flat-band voltage of the fresh device.

leading to the smallest D_{it} for the LF-ZrO sample.[9] However, owing to the high electronegativity of fluorine, excessive fluorine can distort and even cleave the Si-Si bonds at the interface to form dangling Si bonds and Si-F bonds (as demonstrated in Fig. 2),[17,18] resulting in the highest D_{it} and thus the largest window for the HF-ZrO sample.

Fig. 4(a) displays the gate leakage (J_G) of the MONOS devices as a function of electric field across SiO_2 (E_{OX}) by applying positive gate voltage (V_G), corresponding to electron injection from the substrate. The LF-ZrO sample has a smaller leakage at low E_{OX} than the ZrO and HF-ZrO samples due to fewer traps at/near its interface and thus reduced trap-assisted tunneling. Moreover, the J_G-E_{OX} curve of the HF-ZrO sample presents an obvious notch (denoted as A), where J_G decreases with E_{OX} and then increases again. This is associated with its high D_{it} at the SiO_2/Si interface. Due to Coulomb repulsion, electrons trapped by interface states can form a built-in electric field (E_{in}) opposite to the external electric field E_{OX} induced by V_G, which is approximately given by

$$E_{in} \approx \frac{1}{4\pi\varepsilon}\frac{Q_{it}}{R^2}, \tag{2}$$

where Q_{it} is the trapped charge; ε is the permittivity of the dielectric that E_{in} passes through; and R represents the distance between the trapped-charge centroid and the substrate. E_{in} tends to block the electron injection and also electrons filled in the shallow traps near the interface would flow back into the substrate due to E_{in}, both of which can offset the electron injection from the substrate. With increasing E_{OX} and establishing a balance between electron trapping and de-trapping, J_G increases with E_{OX} again. A similar notch (denoted as B) is also observed for the ZrO sample due to high trap density at the ZrO_2/SiO_2 interlayer and high D_{it} at the SiO_2/Si interface. On the contrary, no notch in the J_G-E_{OX} curve for the LF-ZrO sample suggests that its E_{in} is weak and has little effect on electron injection, resulting from the suppressed formation of interlayer at the ZrO_2/SiO_2 interface by the fluorine passivation as well as low D_{it} at the SiO_2/Si interface by avoiding excessive fluorine diffusion to the Si substrate. For the ZrO and HF-ZrO samples, the traps generated by the Zr-silicate interlayer and high interface states lead to larger V_{FB} shift (thus larger Q_{it}) at low electric field as shown in Fig. 4(b). Moreover, these trapped charges at the ZrO_2/SiO_2 and SiO_2/Si interfaces make the trapped-charge centroid closer to the substrate compared with those located in the ZrO_2 film, thus resulting in stronger E_{in} against electron injection according to Eq. (2). This is consistent with the phenomenon that the J_G of the LF-ZrO

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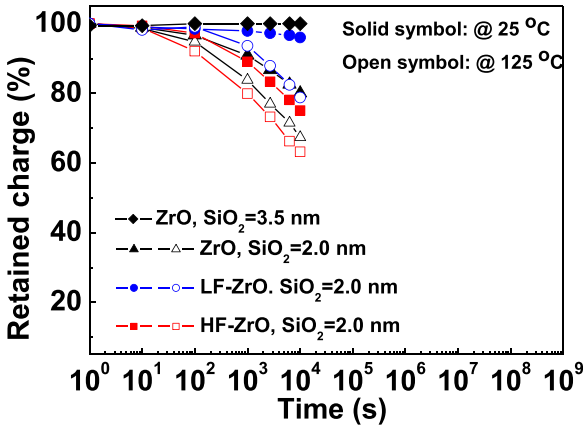
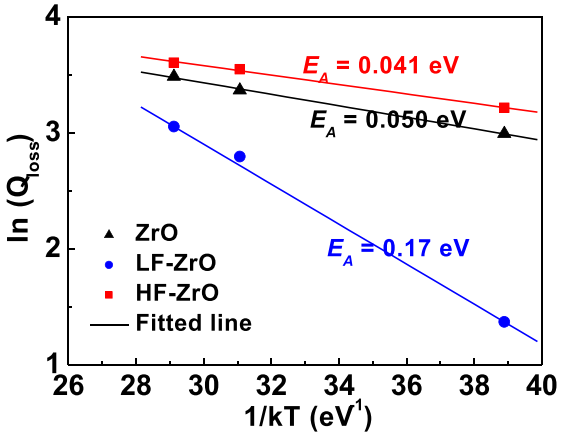
sample increases more rapidly with E_{OX} than those of the ZrO and HF-ZrO samples, which becomes more obvious as the Fowler-Nordheim (FN) tunneling current dominates J_G (FN current is exponentially proportional to electric field of E_{OX}-E_{in}).[19] It should be noted that the little impact of E_{in} on electron injection from the substrate is beneficial to supplying sufficient electrons for the memory device, thus contributing to the larger V_{FB} shift (~3.1 V versus 2.8 V for ZrO, 2.5 V for HF-ZrO) at high electric field for the LF-ZrO sample in Fig. 4(b). On the other hand, small leakage at low electric field normally indicates suppressed trap-assisted tunneling under retention mode and thus is beneficial for data retention. Therefore, the steeper J_G-E_{OX} characteristic of the LF-ZrO sample is desirable for memory device to achieve high operating speed as well as good data retention.

Fig. 5(a) displays the retention characteristics of the MONOS capacitors, and the retention data for the ZrO sample with thicker SiO_2 tunneling layer (SiO_2 ~ 3.5 nm) are also measured to study charge-loss paths under the retention mode. The ZrO sample with thicker SiO_2 shows excellent data retention with no charge loss even after 10^4 s suggests that no charge loss happens through the Al_2O_3 blocking layer mainly due to its high quality with negligible traps. Moreover, compared with the ZrO sample with thicker SiO_2, the ZrO one with thinner SiO_2 (~2.0 nm) shows worse data retention, indicating that the charge loss is mainly determined by the tunneling SiO_2 layer. As the operating temperature is raised from 25 °C to 125 °C, the charge-loss rate after 10^4 s (Q_{loss}) increases from 3.9% to 21.2% for the LF-ZrO sample; For comparison, the corresponding Q_{loss} increases from 19.9% to 32.6% and from 24.9% to 36.8% for the ZrO and HF-ZrO samples, respectively. The lower Q_{loss} of the LF-ZrO sample demonstrates its better data retention. The activation energy E_A of the charge loss is also extracted from the Arrhenius plot of the retention property in Fig. 5(b) to gain more insight on the charge-loss mechanism. The much smaller E_A of the ZrO sample (0.041 eV) and HF-ZrO sample (0.050 eV) indicates that the charge-loss mechanism is mainly based on tunneling process. which hardly depends on temperature.[20] For the ZrO and HF-ZrO samples, the electrons trapped at the ZrO_2/SiO_2 or SiO_2/Si interface are close to the substrate, thus easily escaping back to the substrate, because the tunneling probability increases exponentially with decreasing barrier height and tunneling distance between the trapped electrons and the substrate. Also, the traps at the ZrO_2/SiO_2 and SiO_2/Si interfaces can act as a medium to facilitate the escaping of electrons from the CTL to the substrate by trap-assisted tunneling. On the contrary, the trapped electrons in the LF-ZrO sample cannot move easily by tunneling but have to be thermally activated to the conduction band of the CTL before tunneling to the substrate (due to the larger distance of the trapped charges in the ZrO_2 film from the substrate as well as high-quality ZrO_2/SiO_2 and SiO_2/Si interfaces), thus resulting in larger E_A (~0.17 eV) and better data retention.



(a)



(b)

FIG. 5. (a) Data retention for the MONOS capacitors with an initial V_{FB} shift of 3.2 V. (b) Arrhenius plot of the retention property.

In summary, the effects of fluorine treatment on the charge-trapping characteristics of thin ZrO_2 film are investigated. Compared with the memory devices with no or excessive fluorine treatment, the one with suitable fluorine treatment time shows better characteristics due to suppressed interlayer growth by fluorine passivation of the ZrO_2/SiO_2 interface and also fewer interface states by avoiding excessive fluorine diffusion to the substrate. Therefore, ZrO_2 film with appropriate fluorine incorporation is a promising candidate as CTL for high-performance nonvolatile memory applications.

This work was financially supported by the CRCG Small Project Funding (No. 201209176095) of the University of Hong Kong.

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