# Improved Charge-Trapping Performance of Hf-doped SrTiO<sub>3</sub> for Nonvolatile Memory Applications

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The charge-trapping characteristics of Hf-doped SrTiO<sub>3</sub> have been studied based on Al/Al<sub>2</sub>O<sub>3</sub>/Hf-doped SrTiO<sub>3</sub>/SiO<sub>2</sub>/Si capacitors. The thermodynamic stability of the SrTiO<sub>3</sub> film is significantly improved by Hf incorporation, thus resulting in negligible formation of an interlayer at the Hf-doped SrTiO<sub>3</sub>/SiO<sub>2</sub> interface, as confirmed by X-ray photoelectron spectroscopy and transmission electron microscopy. The memory device with Hf-doped SrTiO<sub>3</sub> as charge-trapping layer displays high speed at low operating voltage (a  $V_{FB}$  shift of 1.9 V at +6 V, 100  $\mu$ s) and good data retention (charge loss of 12.7% after 10<sup>4</sup> s). Therefore, the Hf-doped SrTiO<sub>3</sub> film is a promising material as charge-trapping layer for high-performance nonvolatile memory applications.

### Introduction

Metal-oxide-nitride-oxide-silicon (MONOS) nonvolatile memories with traps distributed in the dielectrics for charge storage have been considered as a better candidate than their conventional floating-gate counterpart due to their localized charge-storage and couplingfree properties. Intensive researches have been carried out to study high-k dielectrics for substituting Si<sub>3</sub>N<sub>4</sub> as charge-trapping layer (CTL) mainly due to the stronger scaling ability, lower operating voltage and higher charge-trapping efficiency. In our previous work. SrTiO3 was demonstrated to be a promising CTL for low-voltage MONOS memory applications due to its high-k value as well as large band offset with respect to the SiO<sub>2</sub> tunneling oxide (1). However, this memory device with SrTiO<sub>3</sub> as CTL displayed severe charge loss mainly due to its poor thermodynamic stability with SiO<sub>2</sub>, which resulted in a thick non-stoichiometric interlayer at the SrTiO<sub>3</sub>/SiO<sub>2</sub> interface. It was also found that this interlayer could be significantly suppressed by inserting HfON between SrTiO<sub>3</sub> and SiO<sub>2</sub> leading to better data retention (2). However, the insertion of HfON increases the processing complexity of the memory device. Additionally, the operating speed and operating voltage of the devices mentioned above need to be further improved (1)(2). Therefore, in order to achieve excellent performance for the SrTiO<sub>3</sub>based memory device with good retention as well as high speed at low operating voltage, this work aims to investigate the charge-trapping characteristics of Hf-doped SrTiO<sub>3</sub> made by co-sputtering technique.

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## **Experiment**

MONOS capacitor with an Al/Al<sub>2</sub>O<sub>3</sub>/Hf-doped SrTiO<sub>3</sub>/SiO<sub>2</sub>/Si structure was fabricated. SiO<sub>2</sub> as tunneling layer (TL) was grown on the p-type Si by thermal oxidation. Then, Hf-doped SrTiO<sub>3</sub> film as CTL was prepared by co-sputtering of Hf and SrTiO<sub>3</sub> targets in an Ar/O<sub>2</sub> mixed ambient. Following that, Al<sub>2</sub>O<sub>3</sub> as blocking layer (BL) was deposited by atomic layer deposition using Al(CH<sub>3</sub>)<sub>3</sub> and H<sub>2</sub>O as precursors at 300 °C. Finally Al was evaporated and patterned as gate electrode, followed by forming-gas annealing at 300 °C for 20 min. The cross-sectional transmission electron microscopy (TEM) image of the completed MONOS device is shown in Figure 1(a).

#### **Results and Discussion**

Figures 1(b) and 1(c) show the Si 2p spectrum as well as the curve-fitting lines for Hf-doped SrTiO<sub>3</sub>/SiO<sub>2</sub> and SrTiO<sub>3</sub>/SiO<sub>2</sub> on Si substrate by X-ray photoelectron spectroscopy (XPS). Each curve-fitting line is assumed to follow the general shape of Lorentzian—Gaussian function. Both of the Si 2p spectra can be decomposed into two components, and correspond to SiO<sub>2</sub> tunneling oxide (103.6 eV) and Ti silicate (102.3 eV) at the CTL/TL interface formed by chemical reaction respectively (3)(4). Note that the area ratio of Si component corresponding to SiO<sub>2</sub> and silicate is 36 for the sample with Hf-doped SrTiO<sub>3</sub>, which is much larger than that for the sample with pure SrTiO<sub>3</sub> (5.0), suggesting a much thinner interlayer at the interface achieved by Hf doping due to the good thermodynamic stability of hafnium oxide contacted with SiO<sub>2</sub>(5). This observation can be further confirmed by the TEM image in Figure 1(a) with no interlayer observed at the CTL/TL interface. Therefore, Hf incorporation can effectively improve the thermodynamic stability of SrTiO<sub>3</sub>.

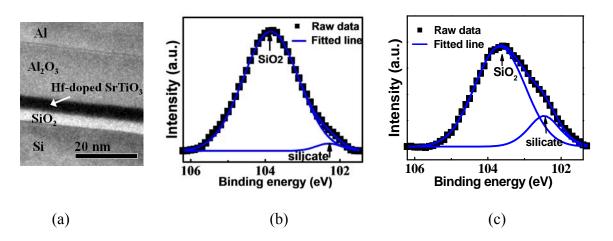


Figure 1. (a) TEM image of the MONOS device, and the thickness of BL/CTL/TL is 15.7 nm/4.3 nm/2.8 nm. (b) Si 2*p* spectrum of the Hf-doped SrTiO<sub>3</sub>/SiO<sub>2</sub> on the Si substrate. (c) Si 2*p* spectrum of the SrTiO<sub>3</sub>/SiO<sub>2</sub> on the Si substrate.

Fig. 2 shows the program/erase (P/E) transient characteristics of the MONOS device with Hf-doped SrTiO<sub>3</sub> as CTL. As the operating voltage  $V_G$  increases from +6 V to +10 V with a pulse width of 1 ms, the  $V_{FB}$  shift ( $\Delta V_{FB}$ ) increases from 2.2 V to 5.3 V. The device shows higher  $\Delta V_{FB}$  (5.3 V at  $V_G$  = 10 V, 1 ms) than the device with SrTiO<sub>3</sub> ( $\Delta V_{FB}$ 

= 3.2 V at  $V_G$  = 10 V, 1 ms) or SrTiO<sub>3</sub>/HfON ( $\Delta V_{FB}$  = 2.9 V at  $V_G$  = 10 V, 1 ms) as CTL under the same operating conditions, even though the former has a thicker TL (2.8 nm) than the latter (2.0 nm) (2). This should be due to the better interfaces of the dielectric stack and more traps in the CTL induced by Hf incorporation in SrTiO<sub>3</sub>, thus resulting in higher charge-trapping efficiency for the device with Hf-doped SrTiO<sub>3</sub>. Moreover, the proposed device presents a high  $\Delta V_{FB}$  of 1.9 V even at a low  $V_G$  of +6 V for 100  $\mu$ s under program state and a high  $\Delta V_{FB}$  of 3.6 V at  $V_G$  of -8 V for 100  $\mu$ s under erase state, demonstrating its high P/E speeds with low-voltage operating ability.

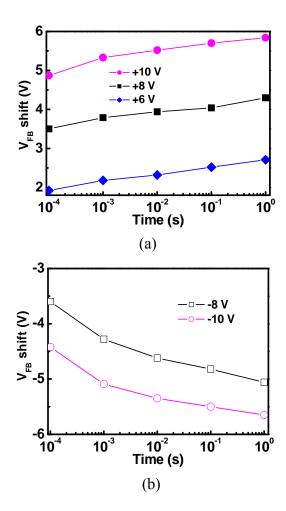


Figure 2. (a) Program and (b) erase transient characteristics of the memory device with Hf-doped SrTiO<sub>3</sub> at various gate voltages.

Figure 3 exhibits the retention characteristics of the device with Hf-doped SrTiO<sub>3</sub> as CTL, which shows good data retention with low charge-loss rate (the charge loss rate  $Q_{loss}$  after  $10^4$  s is 12.7%). As shown in the inset of Figure 3, the device with Hf-doped SrTiO<sub>3</sub> exhibits similar  $Q_{loss}$  as the one with SrTiO<sub>3</sub>/HfON ( $Q_{loss} = 12.3\%$ ), and both devices exhibit much better data retention than the one with SrTiO<sub>3</sub> ( $Q_{loss} = 50.2\%$ ) (2). This should be mainly due to the suppressed formation of interlayer at the CTL/TL interface because the interlayer consumes part of the SiO<sub>2</sub> tunneling oxide (thus shortening the leakage path from the CTL to the substrate) and also traps in the non-stoichiometric interlayer usually facilitate charge loss via trap-assisted tunneling.

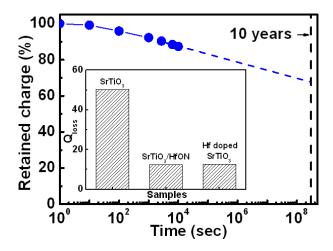


Figure 4. Retention characteristic of the MONOS device with Hf-doped SrTiO<sub>3</sub> as CTL measured at room temperature. The inset shows the Q<sub>loss</sub> of the SrTiO<sub>3</sub>-based devices.

#### **Conclusion**

The charge-trapping characteristics of Hf-doped SrTiO<sub>3</sub> have been studied. The thermodynamic stability of the SrTiO<sub>3</sub> film can be improved by Hf incorporation. The memory device with Hf-doped SrTiO<sub>3</sub> as CTL displays high P/E speeds at low operating voltage and good data retention. Therefore, the Hf-doped SrTiO<sub>3</sub> film is a promising material as CTL for MONOS-type memory applications.

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#### References

- 1. X. D. Huang, P. T. Lai, L. Liu and J. P. Xu, Appl. Phys. Lett., 98, 242905 (2011).
- 2. X. D. Huang, P. T. Lai and Johnny K.O. Sin, Microeletron. Reliab., 52, 2527 (2012).
- 3. D. Brassard, D. K. Sarkar, M. A. El Khakani and L. Ouellet, *Appl.Phys. Lett.*, 84, 2304 (2004).
- 4. D. K. Sarkar, E. Desbiens and M. A. El Khakani, Appl. Phys. Lett., 80, 294 (2002).
- 5. M. Copel, N. Bojarczuk, L. F. Edge and S. Guha, *Appl. Phys. Lett.*, **97**, 182901 (2010).