Charge-Trapping Characteristics of $BaTiO_3$ with and without Nitridation for Nonvolatile Memory Applications

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Abstract: The charge-trapping characteristics of $BaTiO_3$ with and without nitrogen incorporation were investigated based on $Al/Al_2O_3/BaTiO_3/SiO_2/Si$ (MONOS) capacitors. The physical properties of the high-*k* films were analyzed by transmission electron microscopy and X-ray photoelectron spectroscopy. Compared with the MONOS capacitor with $BaTiO_3$ as charge-trapping layer, the one with nitrided $BaTiO_3$ showed higher program speed even at lower operating voltage (4.3 V at +8 V for 100 μs), better endurance property and smaller charge loss (charge loss of 10.6 % after 10^4 s at 85 ^oC), due to the nitrided $BaTiO_3$ film exhibiting higher charge-trapping efficiency caused by nitrogen incorporation and suppressed leakage induced by nitrogen passivation.

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1. Introduction

Metal-oxide-nitride-oxide-silicon (MONOS)-type flash memories with discrete traps in dielectric for charge storage are regarded as a promising candidate for next-generation nonvolatile memories, mainly due to their stronger scaling ability and higher reliability than their floating-gate counterparts. Si_3N_4 was the first dielectric used as the charge-trapping layer (CTL). The main shortcomings of Si_3N_4 as CTL lie in its low dielectric constant ($k \sim 7$) [1], which limits continually down-scaling of cell size; and poor data retention due to the small conduction-band offset ($\Delta E_c = 1.1$ eV) between Si_3N_4 and SiO_2 [2]. Recently, extensive researches have been carried out to study high-k dielectrics instead of Si_3N_4 as CTL mainly due to their higher charge-trapping efficiency and stronger scaling ability, e.g. Gd_2O_3 ($k \sim 14$) [3], Y_2O_3 ($k \sim 18$) [4], HfON ($k \sim 22$) [5, 6], and ZrO_2 ($k \sim 37$) [7]. Among various high-k dielectrics, perovskite-type dielectrics (e.g. $SrTiO_3$, $BaTiO_3$) are regarded as a promising material as charge-trapping layer [8, 9], mainly due to their high dielectric constant ($k > 100$ for $SrTiO_3$) [10, 11], which can enhance the electric field across the SiO_2 tunneling layer, thus improving program/erase (P/E) speeds at low operating voltage; as well as large ΔE_c (~ 3.2 eV for $SrTiO_3$) with respect to SiO_2 [1], which is desirable for data retention because the tunneling probability of electrons from the CTL to the substrate is inversely exponential to the barrier height under retention mode. Compared with $SrTiO_3$, $BaTiO_3$ even displays a larger ΔE_c (~ 3.6 eV) [1], which is helpful to further improve the retention performance. Moreover, nitrogen incorporation also has a profound impact on the charge-trapping characteristics of dielectrics because it can induce more deep-level traps in the band-gap [5][7, 8]. Also, nitrogen incorporation can improve the thermal stability of dielectrics and suppress the inter-diffusion of elements in the dielectric stacks [1][8]. Therefore, based on MONOS capacitors, this

work aims to study the charge-trapping characteristics of nitrided $BaTiO_3$ by comparing with pure $BaTiO_3$.

2. Experiment

MONOS capacitors with $Al/Al_2O_3/BaTiO_3/SiO_2/Si$ were fabricated on p-type silicon substrate. After the standard RCA (Radio Corporation of America, a standard clean procedure) cleaning, 2-nm SiO_2 as tunneling layer (TL) was grown on the wafers by thermal dry oxidation. Then 10-nm $BaTiO_3$ was deposited on the SiO_2 by reactive sputtering using a $BaTiO_3$ target in mixed Ar/N_2 or Ar/O_2 ambient, and the corresponding MONOS capacitors were denoted as the nitrided $BaTiO_3$ sample and the $BaTiO_3$ sample respectively. Next, 15-nm Al_2O_3 as blocking layer (BL) was deposited by atomic layer deposition using trimethyl-aluminum ($Al(CH_3)_3$) and H_2O as precursors at 300 ^oC. Finally Al was evaporated and patterned as gate electrodes by wet etching, followed by forming-gas annealing at 300 ^oC for 20 min. The electrical characteristics were measured by HP4284A LCR meter and HP4156A semiconductor parameter analyzer. Their flatband voltage (V_{FB}) was extracted from their measured capacitance-voltage curve at the capacitance equal to the calculated flatband capacitance.

3. Results and Discussion

Fig. 1(a) shows the Ti 2*p* XPS (X-ray photoelectron spectroscopy) spectrum for the samples with and without nitrogen incorporation. Compared with the $BaTiO_3$ sample, the Ti 2*p* spectrum for the nitrided $BaTiO_3$ sample shifts to lower binding energy by 0.2 eV due to nitrogen incorporation [7]. The nitrogen content is calculated to be 3.3 % from XPS analysis as shown in the inset of Fig. 1(a). Fig. 1(b) shows the

Si 2*p* spectrum for the samples with and without nitrogen incorporation, which presents two intense peaks located at 99.7 eV and 103.2 eV, corresponding to the Si substrate and SiO_2 tunneling oxide respectively. Moreover, compared with the nitrided $BaTiO_3$ sample, the $BaTiO_3$ sample displays an obvious shoulder at 101.6 eV which agrees with the value for Ti silicate [12]. Fig. 2 shows the cross-sectional TEM (transmission electron microscopy) images of the samples. The nitrided $BaTiO_3$ sample displays a negligible interlayer at the CTL/SiO_2 interface compared with the $BaTiO_3$ sample due to nitrogen passivation, which is consistent with the XPS observation.

Fig. 3(a) shows the program transient characteristics of the MONOS capacitors with and without nitrogen incorporation at various operating voltages. It is noted that the nitrided $BaTiO_3$ sample has a similar equivalent oxide thickness (EOT, 11.6 nm) as the $BaTiO_3$ sample (12.2 nm), which suggests a similar electric field across the SiO_2 tunneling layer of both samples under the same operating voltage. As the operating voltage increases from +8 V to +12 V with a fixed pulse-width of 100 μs, the V_{FB} shift (ΔV_{FB}, defined as $\Delta V_{FB} = V_{FB} - V_{FB0}$, where V_{FB} is the flatband voltage under stress, and V_{FB0} is the neutral flat-band voltage of the fresh device) increases from 2.22 V/4.33V to 4.55 V/7.16 V for the $BaTiO_3$ and nitrided $BaTiO_3$ samples respectively. It is worth mentioning that the nitrided $BaTiO_3$ sample shows a similar ΔV_{FB} (~ 4.33 V) even at a smaller gate voltage of +8 V as the $BaTiO_3$ sample (~ 4.55 V) at +12 V for the same stress time of 100 μs, further supporting its much higher program speed. To gain more insight on this phenomenon, the gate leakage as a function of positive gate voltage (I-V_G) is also shown in Fig. 3(b), which corresponds to electron injection from the substrate toward the gate electrode. The injected electrons from the substrate can be divided into two parts: one part flows

through the dielectrics to the gate electrode, resulting in gate leakage; the other part is trapped in the dielectric, leading to V_{FB} shift of the device. The higher gate leakage of the $BaTiO_3$ sample indicates more electrons flowing from the substrate to the gate electrode rather than being trapped in the charge-trapping layer. This is consistent with its smaller ΔV_{FB} (~ 5.12 V) after V_G sweeping than that of the nitrided $BaTiO_3$ sample (~ 7.17 V). Therefore, it is believed that the higher program speed of the nitrided $BaTiO_3$ sample should be mainly due to its higher charge-trapping efficiency resulting from more deep-level traps induced by nitrogen incorporation [5][7, 8]. Moreover, unlike resistive random access memories (RRAM) [13], the I-V_G curves in Fig. 3(b) for both samples show no switching phenomenon. This should be due to high quality of the SiO_2 tunneling layer and the Al_2O_3 blocking layer with few traps as shown in the inset of Fig. 3(b), which blocks the formation of conductive filaments between the Al electrode and Si substrate. Fig. 3(c) shows the erase transient characteristics of the samples with and without nitrogen incorporation, where both samples are prepared with the same ΔV_{FB} = +8 V for fair comparison before erasing. Both samples (especially the nitrided $BaTiO_3$ sample) cannot return the fresh state and have no over-erase phenomenon even operated at high gate voltage (-14 V), suggesting that hole trapping is negligible and electron de-trapping is dominant under the erase operation. The nitrided $BaTiO_3$ sample exhibits lower erase speed than the $BaTiO_3$ sample under the same operating conditions, and needs higher operating voltage to achieve a similar ΔV_{FB} (~ -7.3 V at -14 V, 1 s) as the latter (~ -7.2 V at -12 V, 1 s). This should be due to more deep-level traps (thus higher ratio of deep-level traps and shallow-level traps) in the nitrided $BaTiO_3$ film; therefore, electrons trapped in these deep traps are more difficult to de-trap from the CTL to the substrate than

those trapped in the shallow-level traps [6]. This inference can be further confirmed later by the retention property shown in Fig. 4.

Fig. 4 displays the retention characteristics of the MONOS capacitors with and without nitrogen incorporation measured at 85 ^{o}C. For fair comparison, both samples are programmed/erased to achieve a similar initial P/E memory window (5.2 V ~ 5.3 V). The V_{FB} degrades with time during the retention mode, which is mainly due to the loss of charge stored in the charge-trapping layer via tunneling back to the substrate and gate electrode. The decay rate of the nitrided $BaTiO_3$ sample is 117.5 mV/dec and 20.0 mV/dec under the program and erase states respectively. For comparison, the corresponding decay rate of the $BaTiO_3$ sample is 310.0 mV/dec and 60.0 mV/dec. Also, as shown in the inset of Fig. 4, the normalized retained charge after 10 years is evaluated by extrapolation to be 56.3 % and 24.0 % for the samples with and without nitrogen incorporation respectively. The superior data retention of the nitrided $BaTiO_3$ sample should be ascribed to more deep-level traps in the nitrided $BaTiO_3$ film induced by nitrogen incorporation [5][7, 8]. In addition, nitrogen incorporation can block elemental inter-diffusion, thus leading to an excellent CTL/SiO_2 interface with negligible formation of non-stoichiometric interlayer (see Fig. 2) [1][8]. This also contributes to better data retention of the nitrided $BaTiO_3$ sample because the charge-loss path via defects located at the CTL/SiO_2 interface by trap-assisted tunneling can be suppressed. This inference can be further confirmed by the I-V characteristics shown in Fig. 3(b), where the nitrided $BaTiO_3$ sample displays lower gate leakage than the $BaTiO_3$ one in the low-voltage range corresponding to the retention mode.

Fig. 5 shows the endurance characteristics of the MONOS capacitors with and without nitrogen incorporation, where P/E stressing conditions are chosen to achieve a similar initial P/E memory window for fair comparison. The initial P/E window of the

nitrided $BaTiO_3$ and $BaTiO_3$ samples is 3.79 V and 3.94 V respectively. After a 10^5-cycle P/E stressing, the P/E window decreases to 3.65 V and 3.52 V, corresponding to a degradation of 3.7 % and 10.7 % for the nitrided $BaTiO_3$ and $BaTiO_3$ samples respectively. The better endurance of the nitrided $BaTiO_3$ sample should be mainly ascribed to its higher P/E speeds at lower operating voltages resulting from the higher charge-trapping efficiency caused by nitrogen incorporation.

4. Conclusion

In summary, the charge-trapping characteristics of $BaTiO_3$ film with and without nitrogen incorporation are investigated based on MONOS-type capacitors. The MONOS capacitor with nitrided $BaTiO_3$ as CTL shows better electrical characteristics in terms of higher program speed, better endurance and smaller charge loss than the one without nitridation, because the nitrided $BaTiO_3$ film exhibits higher charge-trapping efficiency induced by nitrogen incorporation and suppressed leakage through nitrogen passivation. Therefore, the nitrided $BaTiO_3$ film is a promising charge-trapping layer for high-performance nonvolatile memory applications.

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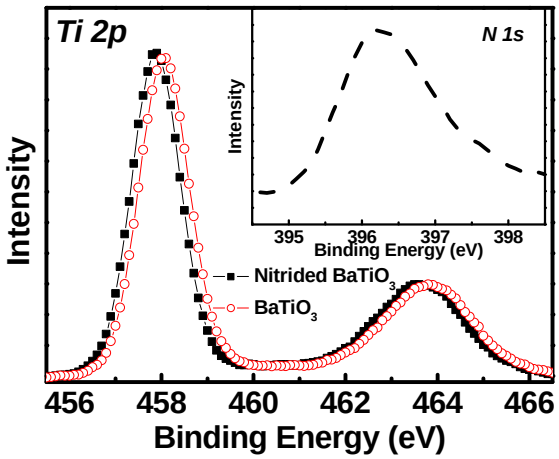
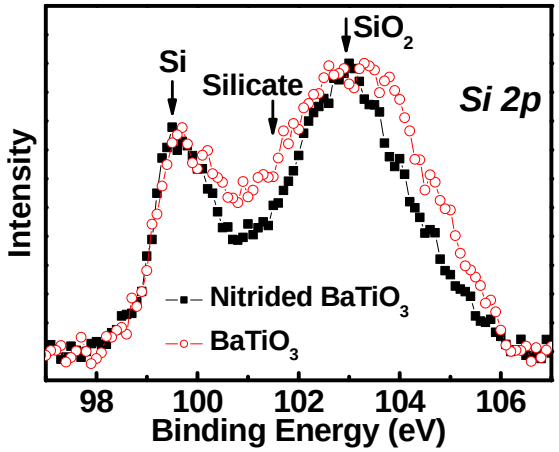
Fig. 1. XPS spectra for the samples with and without nitrogen incorporation: (a) Ti 2*p* spectrum and (b) Si 2*p* spectrum. The inset of (a) is the N 1*s* spectrum.



(a)



(b)

Fig. 2. Cross-sectional TEM images of the MONOS capacitors (a) with and (b) without nitrogen incorporation, where the factual thickness of the charge-trapping layer is 11.5 nm and 10.2 nm for the nitrided $BaTiO_3$ and $BaTiO_3$ samples respectively.

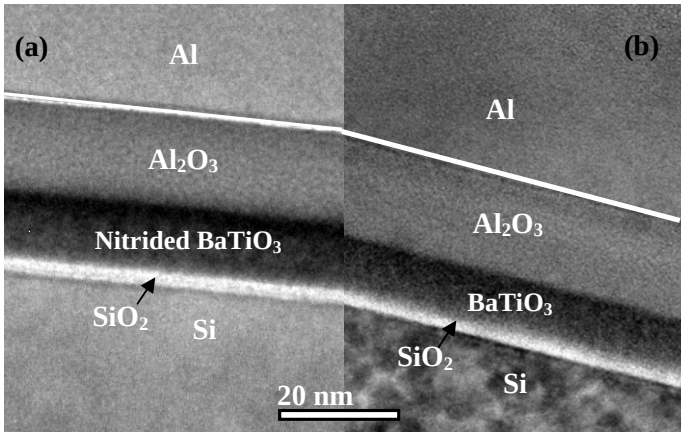
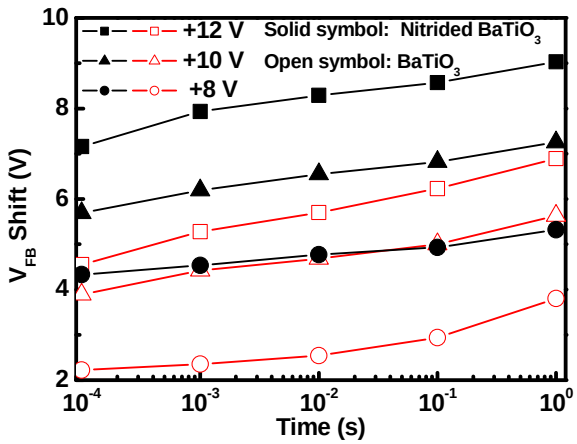
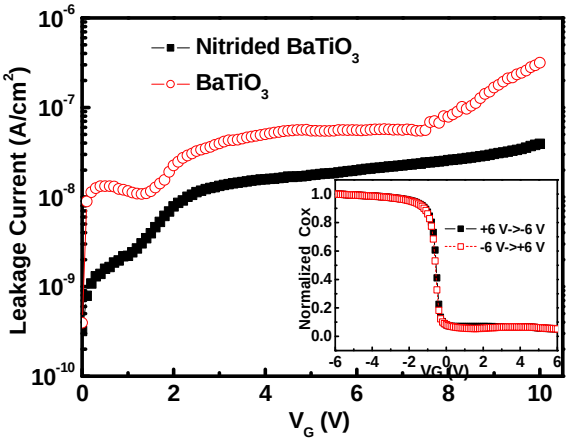


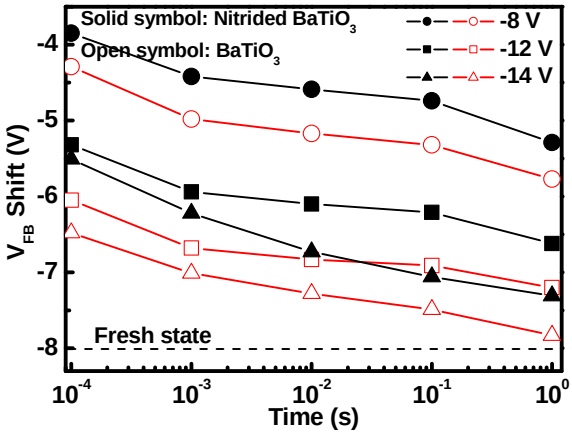
Fig. 3. (a) Program transient characteristics of the MONOS capacitors with and without nitrogen incorporation as a function of pulse width at various gate voltages. (b) Gate leakage current as a function of positive gate voltage corresponding to electron injection from the substrate. The inset shows the capacitance-voltage (C_{ox}-V_G) hysteresis loops for the Al/Al_2O_3/SiO_2/Si sample under ±6 sweeping voltage, and no hysteresis memory window indicates few traps in the SiO_2 and Al_2O_3 layers. (c) Erase transient characteristics of the samples with and without nitrogen incorporation. The samples are programmed to be with the same ΔV_{FB} = +8 V firstly before erase test.



(a)



(b)


Solid symbol: Nitrided BaTiO3
Open symbol: BaTiO3
-8 V
-12 V
-14 V
Fresh state
V FB Shift (V)
-4
-5
-6
-7
-8
10-4
10-3
10-2
10-1
100
Time (s)

(c)

Fig. 4. Retention characteristics of the MONOS capacitors with and without nitrogen incorporation measured at 85 °C. The inset shows normalized retained charges for the P/E states as a function of time.

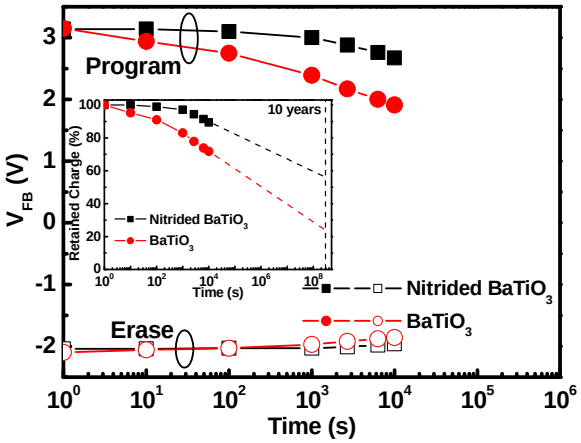


Fig. 5. Endurance characteristics of the MONOS capacitors measured at room temperature. To achieve a similar initial P/E memory window, the P/E stress is +8 V, 100 μs/-8 V, 1 ms for the nitrided $BaTiO_3$ sample, and +10 V, 100 μs/-10 V, 100 μs for the $BaTiO_3$ sample respectively.