Improved Performance by using $TaON/SiO_2$ as Dual Tunnel Layer in Charge-Trapping Nonvolatile Memory

J. X. Chen[a], J. P. Xu[a]* , L. Liu[a], X. D. Huang[b], P. T. Lai[b]*

[a] School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan 430074, P. R. China
[b] Department of Electrical & Electronic Engineering, the University of Hong Kong, Pokfulam Road, Hong Kong

Abstract

Tunneling-barrier engineered stacks with different high-κ dielectrics are investigated by fabricating the stacked structures of $Al/Al_2O_3/HfLaON/(TaON/SiO_2)/Si$ and $Al/Al_2O_3/HfLaON/(HfON/SiO_2)/Si$. As compared to the device with $HfON/SiO_2$ dual tunnel layer (DTL), the one with $TaON/SiO_2$ DTL shows larger memory window (3.85 V at ±13 V/1 s), higher program/erase speeds (1.85 V/-2.00 V at +/-12 V/100 μs), better endurance (window narrowing rate of 5.7% after 10^5 cycles). The main mechanisms involved lie in (1) the higher dielectric constant of TaON which induces high electric field in the SiO_2 layer, (2) the smaller conduction/valence-band offsets between TaON and the Si substrate, and (3) better interface quality with SiO_2. Furthermore, compared with SiO_2 single tunnel layer, better retention characteristics can be achieved for the $TaON/SiO_2$ DTL due to its larger thickness.

Keywords: Flash memory; MONOS; dual tunnel layer (DTL); high-κ dielectric

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*Corresponding authors.
E-mail address: jpxu@mail.hust.edu.cn, fax: +86-27-87544406 (J. P. Xu),
E-mail address: laip@eee.hku.hk, fax: +852-25598738 (P. T. Lai)

1, Introduction

In recent years, metal-oxide-nitride-oxide-silicon (MONOS) charge-trapping flash memory has attracted a lot of attention due to its advantages of low operating voltage, feasibility of scaling, and simple fabrication process. The basic challenge of the charge-trapping flash memory is how to achieve a tradeoff between program/erase (P/E) efficiency and data retention [1]. The variable oxide thickness (VARIOT) concept [2], consisting of at least two dielectric layers with different dielectric constants κ (i.e., low-κ/high-κ stack), is a promising solution for the compromise due to the enhanced sensitivity of tunneling current to electric field. Over the past years, Si_3N_4, Al_2O_3, HfO_2, HfAlO, and Ti-silicate have been investigated as the high-κ material in the SiO_2/high-κ stack [3-7], and improvements in the relevant memory performances have been demonstrated by using the low-κ/high-κ stack as dual tunnel layer (DTL). On the other hand, nitrogen incorporation in high-κ dielectric films can results in beneficial characteristics, including excellent resistance to interdiffusion of elements between different layers, improved thermodynamic stability, and enhanced immunity to damage induced by high-field stress [8, 9], all of which are highly desirable for the tunneling-barrier engineering applications. However, a combination of the VARIOT concept with the nitrided high-κ oxide film was rarely reported. With a high dielectric constant (κ ~ 22) and good thermodynamic stability

on SiO_2, the low-trap-density HfON is believed to be a promising candidate for the barrier-engineered tunnel dielectric in NAND flash memory applications [10-12]. In addition, TaON was also proposed to replace the conventional SiO_2 due to its high dielectric constant ($\kappa \sim 34$) as well as good thermal stability [13, 14], and its small conduction/valence-band offsets to the Si substrate makes it very beneficial for electrons/holes tunneling through the barrier and thus improving P/E performance of the memory devices [15, 16]. Therefore, a new MONOS flash memory structure with TaON/SiO_2 or HfON/SiO_2 as DTL can be proposed by combining the VARIOT concept with the nitrided high-κ oxide film.

In this work, MONOS devices with TaON/SiO_2 or HfON/SiO_2 as DTL, HfLaON as charge storage layer (CSL) and Al_2O_3 as blocking layer (BL) were fabricated, and their memory performances are extensively compared. Experimental results reveal that the memory device with TaON/SiO_2 DTL can achieve larger memory window, higher P/E speeds, and better endurance than the device with HfON/SiO_2 DTL. Also, the retention characteristics of both devices with DTL are improved as compared with the control device with SiO_2 as single tunnel layer.

2, Experimental details

MONOS capacitors were fabricated on p-type silicon wafers with a resistivity of 1 ~ 10 Ω•cm. After the standard RCA cleaning, 4-nm SiO_2 was grown by thermal oxidation at 900 ^{0}C. Then, 4-nm TaON was deposited on SiO_2 by sputtering a Ta target in an $Ar/O_2/N_2$ (12/3/15) ambient, followed by rapid thermal annealing in N_2 at 800 ^{0}C for 30 s to form TaON/SiO_2 DTL (denoted as TaON sample). For comparison, HfON was also prepared on SiO_2 by sputtering a Hf target in the same deposition and annealing conditions to form HfON/SiO_2 DTL (denoted as HfON sample). Next, 10-nm HfLaON layer as CSL was deposited by RF-sputtering of HfLa target in an $Ar/O_2/N_2$ (24/3/6) ambient, followed by rapid thermal annealing in N_2 at 500 ^{0}C for 30 s. Then, 13-nm Al_2O_3 as blocking layer was deposited by ALD method at 300 ^{0}C. Finally, Al was evaporated and patterned as gate electrode and also as back electrode, followed by forming-gas annealing in H_2/N_2 (5% H_2) at 300 ^{0}C for 20 min. In order to investigate the qualities of the TaON/SiO_2 and HfON/SiO_2 interfaces, MIS capacitors with Al/TaON/SiO_2/Si and Al/HfON/SiO_2/Si structures were fabricated by the same processing conditions.

The dielectric film thickness was measured by multi-wavelength ellipsometry. The electrical characteristics of the devices were measured at room temperature using HP4284A precision LCR meter and HP4156A precision semiconductor parameter analyzer. The flat-band voltage (V_{FB})

of the samples was extracted by assuming C_{FB}/C_{OX} = 0.5 (C_{FB} and C_{OX} are the flat-band and oxide capacitances respectively, determined from 1-MHz high-frequency C-V curve). All measurements were carried out under light-tight and electrically-shielded condition.

3, Results and discussion

Fig. 1 shows the C-V curves of the MIS capacitors swept in forward and backward directions under +/-4 V sweeping voltages. Little hysteresis is observed for the two devices, indicating the high-quality bulk and interfacial properties of the high-k dielectric layers. Furthermore, the slope of the C-V curve for the Al/TaON/SiO_2/Si MIS capacitor is steeper than that of the Al/HfON/SiO_2/Si MIS capacitor, implying better interface quality for the TaON/SiO_2 than the HfON/SiO_2 [17]. In addition, based on the dielectric constants of TaON and HfON [10,14] as well as a low-κ/high-κ thickness of 4 nm/4 nm, the accumulation capacitance for the MIS capacitors with Al/TaON (or HfON) /SiO_2/Si structures and gate area of 7.85×10^{-5} cm^2 can be calculated to be 60.7 pF and 57.5 pF respectively, which are larger than the ones extracted from the measured C-V curves of the two samples (53.6 pF and 50.8 pF, respectively). The difference should be attributed to the fact that the κ values of the deposited dielectrics are slightly smaller than those in the literature, probably due to the difference in elemental composition and the interface

between the high-κ/low-κ layers [17].

Fig. 2 shows the memory window of the two samples under different P/E voltages for 1 s. It can be observed that the TaON sample presents larger flatband voltage shift (ΔV_{FB}) than the HfON observed sample. Furthermore, their difference increases as the P/E voltage increases. This could be attributed to the fact that TaON has a larger dielectric constant (κ ~ 34) [14] than HfON (κ ~ 22) [10], which induces higher electric field in the SiO_2 layer, thus leading to a larger bending of energy band. Also, as shown in Fig. 3, the conduction-band offset of TaON to the Si substrate is 0.3 eV [15, 16], much smaller than the 2.0 eV [10] of HfON conduction-band offset to the Si substrate. Therefore, the electron tunneling distance is shorter in the TaON sample than the HfON sample at the same gate bias.

As shown in Fig. 4, the P/E transient performances are characterized in terms of ΔV_{FB} as a function of time under P/E voltages of ±12 V. Obviously, higher P/E speeds can be attained for the TaON sample than the HfON sample. After initial 100-μs P/E voltages of +/-12 V, the flatband voltage shift is 1.85 V/-2.00 V for the TaON sample, and 1.55 V/-1.15 V for the HfON sample. Furthermore, the TaON sample then exhibits a larger change of ΔV_{FB}. Since the CSL and BL are the same for the two devices, the above differences in performances should be mainly attributed to the difference in their stacked tunneling dielectrics. As

mentioned above, the conduction-band offset of TaON to the Si substrate is much smaller than that of HfON, and so the barrier height of the TaON layer is much smaller than that of the HfON layer. On the other hand, the larger dielectric constant of TaON (than that of HfON) results in a higher electric field in the SiO_2 layer of the TaON sample than the HfON sample due to the redistribution of the applied bias over the high-κ/low-κ layers [19]. Consequently, as shown in Fig. 3 (c) and (d), the TaON/SiO_2 DTL exhibits shorter tunneling distance than the HfON/SiO_2 DTL under the same bias, and electrons/holes can tunnel through the TaON/SiO_2 barrier more easily, thus resulting in significantly better P/E performances for the TaON/SiO_2 DTL than the HfON/SiO_2 DTL.

Fig. 5 shows the endurance characteristics of the two devices. The P/E cycle is performed at +/-12 V with a pulse width of 100 μs/100 μs, and then the V_{FB} shift is extracted by measuring the C-V curve after 1, 10^1, 10^2, 10^3, 10^4, and 10^5 P/E cycles. As can be seen in Fig. 5, the memory window is initially 2.65 V and 1.60 V for the TaON and HfON samples respectively and becomes 2.50 V and 1.50 V after 10^5 cycles. The lower loss rate of memory window for the TaON sample (5.7%) than the HfON sample (6.3%) could be attributed to the better interface quality of the former, as confirmed in Fig. 1. Besides, the memory-window narrowing of the two devices is not severe, but the flatband voltage presents negative shift for both program and erase states. The negative

V_{FB} shift for the erase state implies that some holes are probably trapped at/near the CSL/TaON (or HfON) interface during the P/E cycling, and the almost unchanged memory window indicates that the amount of electrons captured from the programming tunneling current basically remains the same [19].

Fig. 6 is the retention characteristics of the two samples measured at room temperature after removing the program or erase voltage of +12 V or -12 V for 1 s. The V_{FB} change is extracted by measuring the C-V curves at successive times from 1 s to 10000 s. In order to clarify the impact of the DTL on data retention, another device with only 4-nm SiO_2 as tunnel layer and the same CSL and BL as the TaON and HfON samples is also fabricated (denoted as SiO2 sample). It can be seen that the extrapolated 10-year memory window is 2.04 V, 1.41 V, and 1.92 V for the TaON, HfON and SiO2 samples, respectively (the initial window is 2.60 V, 1.75 V, and 2.90 V, respectively), corresponding to a charge-loss rate of 21.5%, 19.4%, and 33.8%, respectively. Although the TaON sample shows a slightly larger charge leakage than the HfON sample, it is still much smaller than that of the SiO2 sample, indicating that the larger physical thickness of the DTL can effectively improve the charge retention. Since TaON has better interface quality with SiO_2 than HfON (mentioned above), the slightly higher charge-loss rate for the TaON sample than the HfON sample should be mainly attributed to the band

offsets between the high-κ dielectric layer and the silicon substrate, as presented in Fig. 7. Since the conduction band of TaON/HfON is below/above that of HfLaON respectively, the TaON/ SiO_2 barrier exhibits slightly poorer ability in blocking electrons than the HfON/SiO_2 barrier. On the other hand, since more electrons are trapped in the CSL of the TaON sample, a slightly higher electric field is induced in the SiO_2 layer and thus slightly larger bending of energy band occurs during retention (see Fig. 7), which can further enhance the discharge of electrons from the CSL. However, in view of the large memory window, high P/E speeds and good endurance property, the stacked dielectric of TaON/SiO_2 is still a good choice for the DTL application.

4, Conclusion

In summary, high-κ/low-κ dielectric stacks (TaON/SiO_2 and HfON/SiO_2) as DTL have been investigated based on MONOS capacitors. As compared with the MONOS capacitor with HfON/SiO_2 DTL, the MONOS capacitor with TaON/SiO_2 DTL shows larger memory window, higher P/E speeds, and better endurance. The involved mechanisms are that TaON has larger dielectric constant and smaller band offset to the Si substrate than HfON, thus greatly enhancing charge injection from the Si substrate to the CSL. In addition, the better interface quality for the TaON/SiO_2 DTL than the HfON/SiO_2 DTL is responsible for the better endurance of the former. Furthermore, compared with the device using

only SiO_2 as tunneling layer, both devices with DTL can achieve improved retention characteristics due to the larger physical thickness of the tunnel layer. Therefore, the TaON/SiO_2 stack is a potential alternative as the DTL for MONOS charge-trapping flash memory applications.

Acknowledgments

This work is financially supported by the National Natural Science Foundation of China (Grant no. 60976091) and the University Development Fund (Nanotechnology Research Institute, 00600009) of the University of Hong Kong.

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Captions:

Fig. 1 C-V curves of the MIS capacitors with Al/TaON/SiO_2/Si and Al/HfON/SiO_2/Si structures swept in bi-directions under +/-4 V sweeping voltages.

Fig. 2 Memory window of the two samples under different P/E voltages for 1 s.

Fig. 3 Energy band diagrams of TaON sample (a) and HfON sample (b) under flat band conditions, and TaON sample (c) and HfON sample (d) under programming states.

Fig. 4 The P/E transient performances of the two samples in terms of ΔV_{FB} as a function of time at P/E voltages of ± 12 V: (a) program state and (b) erase state.

Fig. 5 Endurance characteristics of the two devices, with the P/E cycle performed at +/-12 V for 100 μs /100 μs, respectively.

Fig. 6 Retention characteristics of the three samples measured at room temperature after removing 1-s P/E voltages at +/-12 V.

Fig. 7 Energy band diagram of TaON and HfON samples under retention mode.

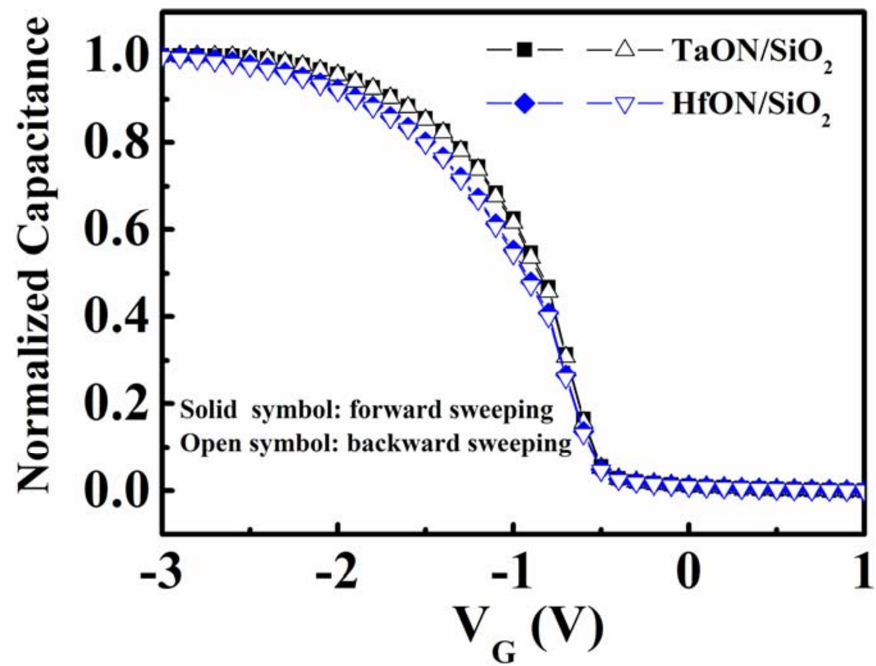

Fig. 1

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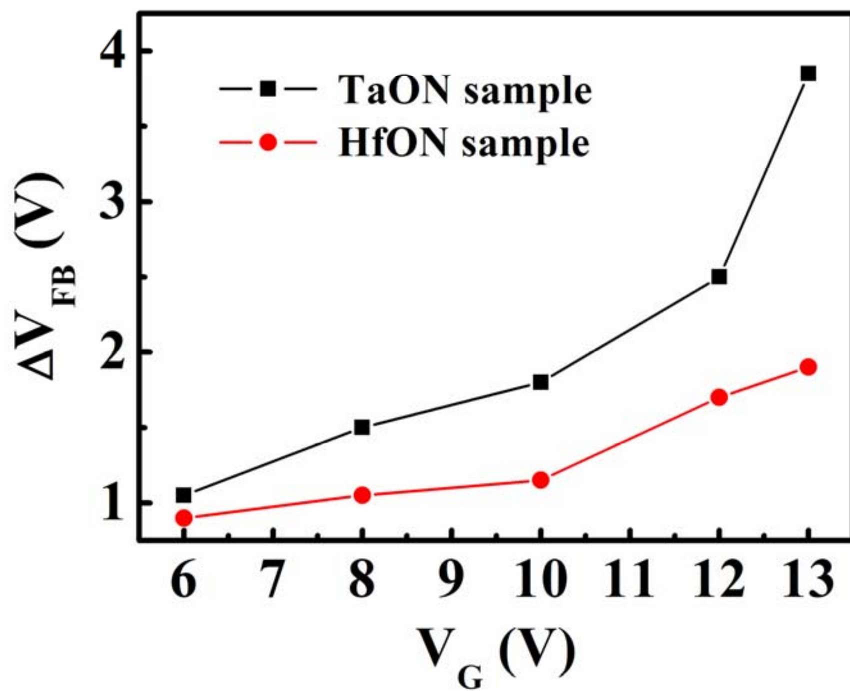

Fig. 2
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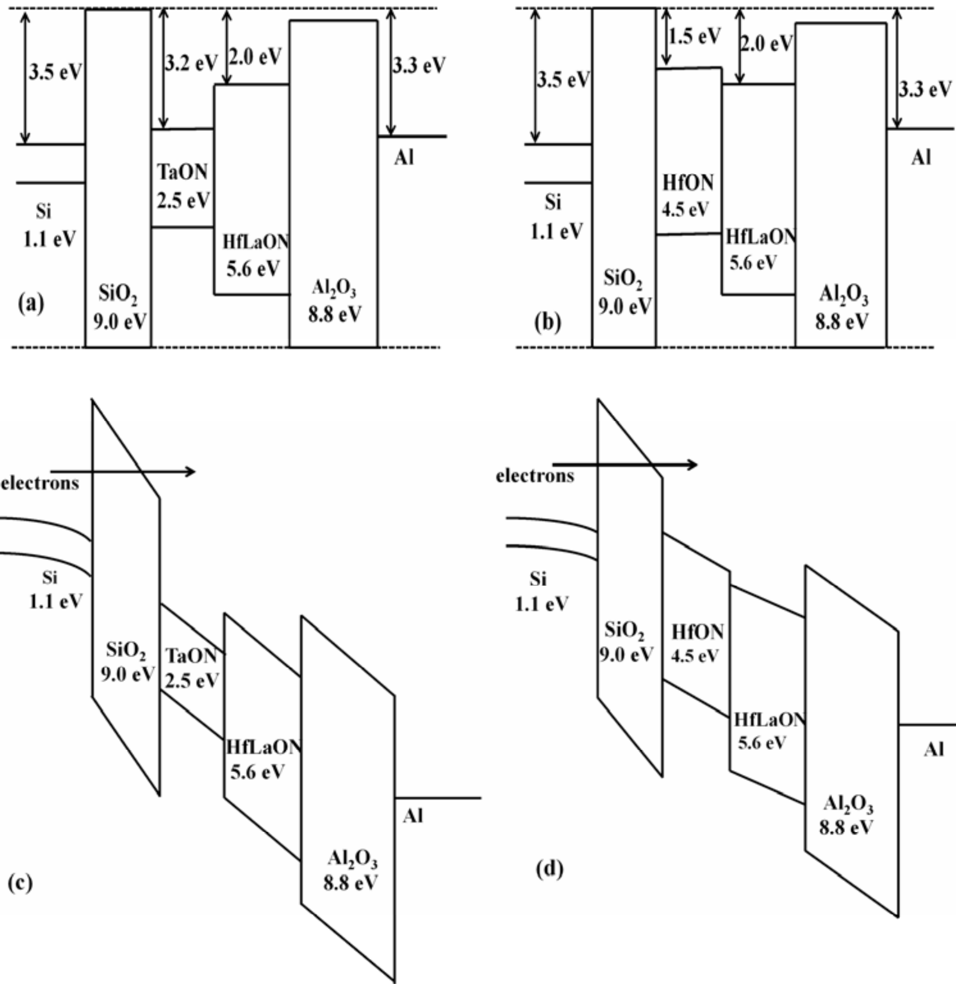

Fig. 3
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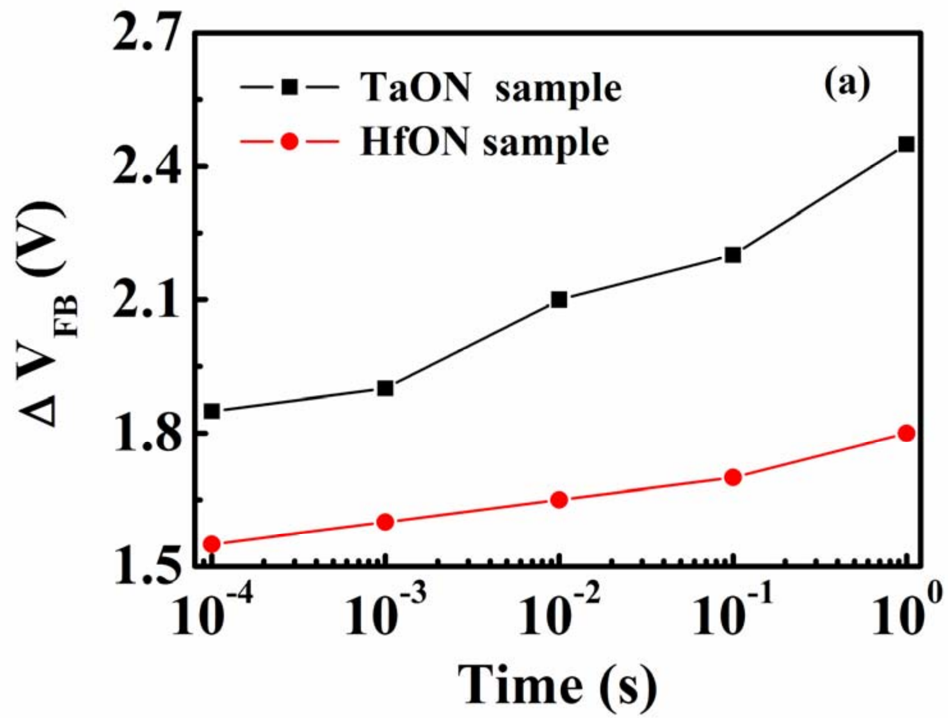

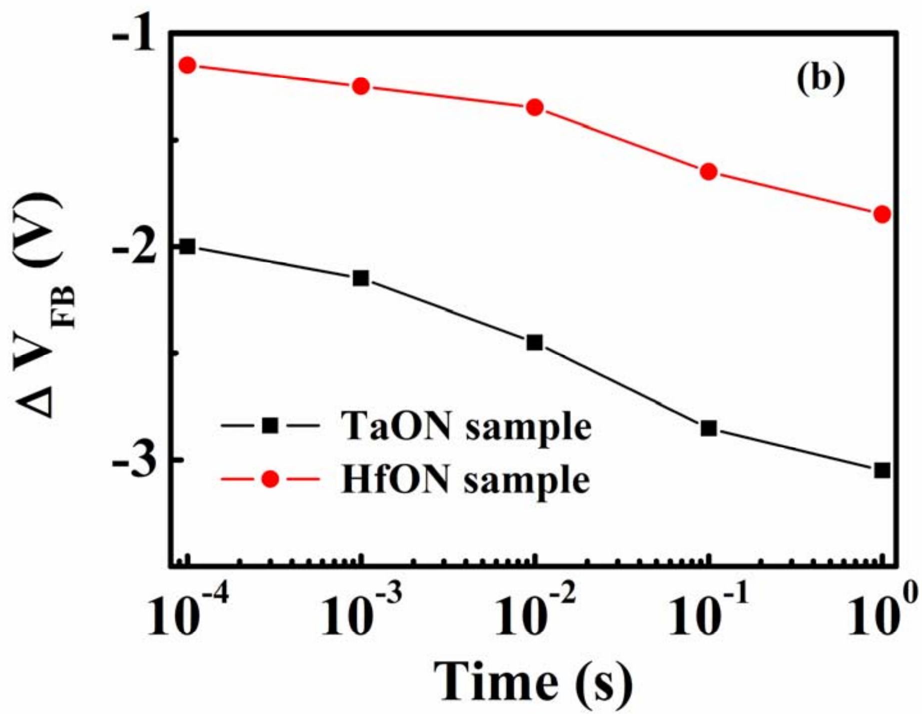

Fig. 4
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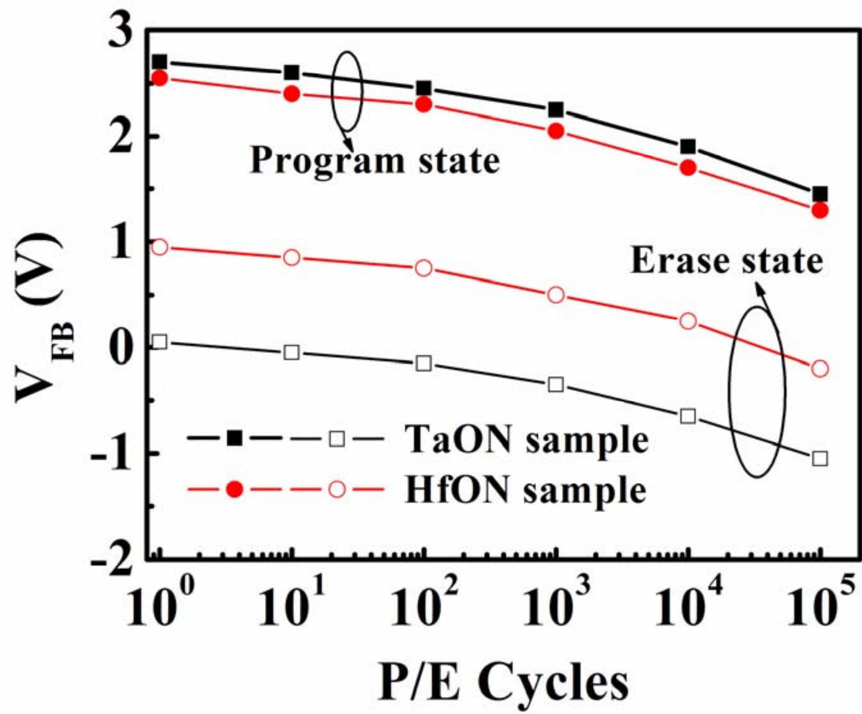

Fig. 5
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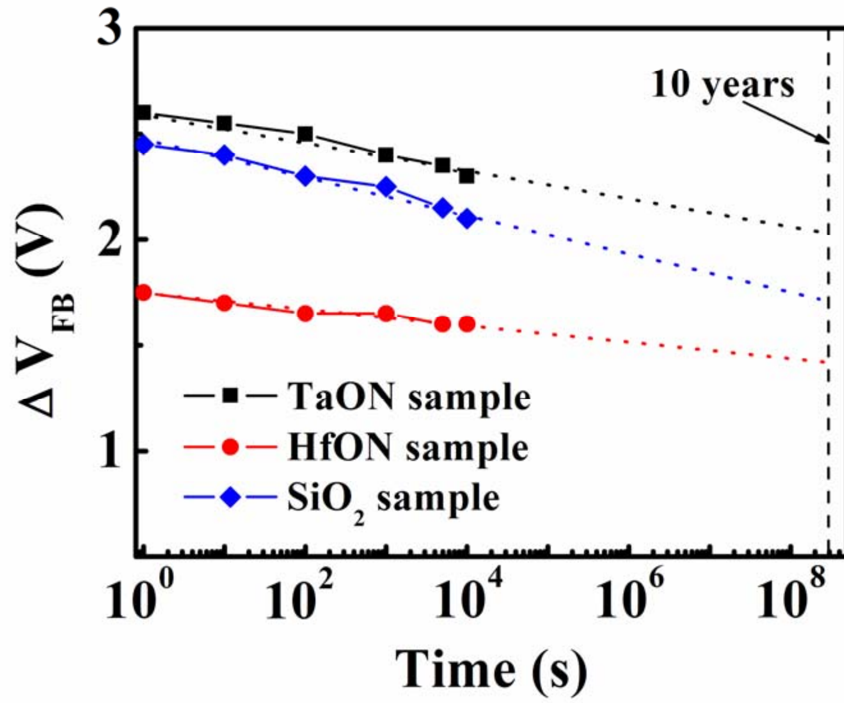

Fig. 6
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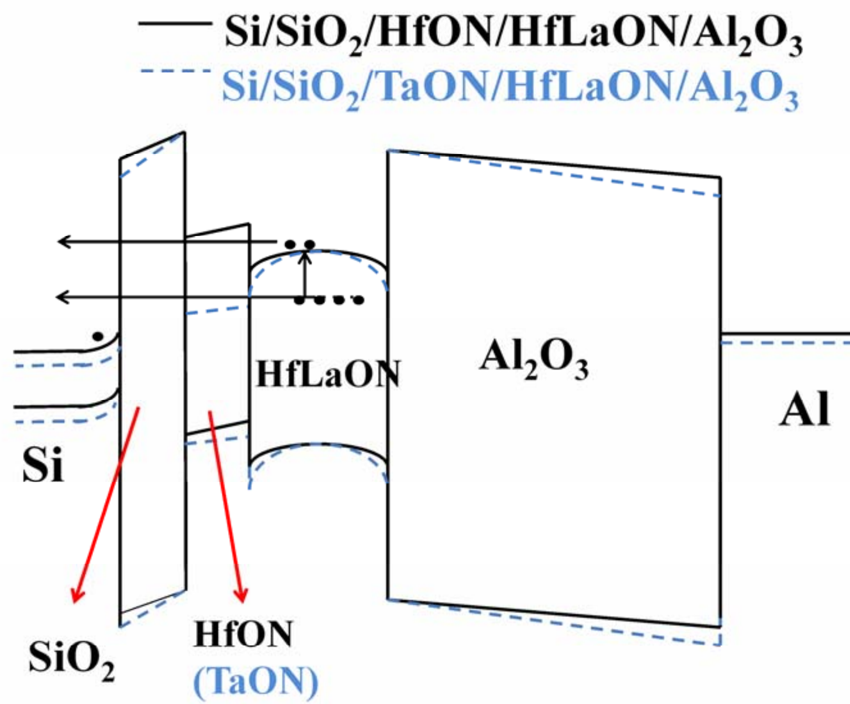

Fig. 7
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