Flexible transistor active matrix array with all screen-printed electrodes

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ABSTRACT

Flexible transistor active matrix array is fabricated on PEN substrate using all screen-printed gate, source and drain electrodes. Parylene-C and DNTT act as gate dielectric layer and semiconductor, respectively. The transistor possesses high mobility (0.33 $cm^2V^{-1}s^{-1}$), large on/off ratio (> 10^6) and low leakage current (~10 pA). Active matrix array consists of 10×10 transistors were demonstrated. Transistors exhibited average mobility of 0.29 $cm^2V^{-1}s^{-1}$ and on/off ratio larger than 10^4 in array form. In the transistor array, we achieve 75μm channel length and a size of 2 mm × 2 mm for each element in the array which indicates the current screen-printing method has large potential in large-area circuits and display applications.

Keyword: screen-printing, active matrix array, room temperature, parylene-C, DNTT

1. INTRODUCTION

Organic thin film transistors (OTFTs) have unique advantages such as mechanical flexibility, large-area production and low-cost fabrication processes [1-3]. To realize real large-area production, vapor deposition methods like PVD or CVD cannot fulfill this demand, as these methods require high vacuum or high temperature which makes them energy and time consuming. Spin coating [4] and drop casting [5] methods have been widely used in deposition semiconductors and dielectric layers in OTFT fabrication. But for electrodes deposition, these methods need to be combined with lithography or chemical etching methods to create patterned gate, source and drain electrodes. Solution processed electrodes towards all solution processed OTFT have drawn people's attention in the last decade. Ink-jet printing is a well-developed method for electrode deposition in OTFT fabrication [6, 7]. Someya *et al*. even reported to get 1 um channel length using this method [8]. However, the operating speed of the system is limited by the programmable nozzle control and thus the printing area is limited. To overcome these shortcomings, we present screen-printing method for electrodes deposition in OTFT fabrication which can realize fast, large-area and low temperature fabrication.

Screen-printing methods has been widely used in cloth and painting industry. This method was also adopted by researchers to form thick ceramic films (thicker than 1 μm) in ceramic capacitor fabrication and electrical connections [9, 10]. In the screen-printing, usually more viscous paste can offer high pattern resolution but at the same time the thickness can be larger, which makes it hard to use this method for electrode printing in OTFT fabrication especially for gate electrode printing. Song *et al*. reported a printing technology combining screen-printing with a wet-etching process to fabricate gate electrode of OTFT [11].

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In the current screen-printing field, the screen mesh has mesh number (mesh per inch) over 500 which is capable of define patterns thinner than 100 μm. At the same time, precise control on emulsion layer thickness can decrease the thickness of printed film to ~5 μm. These technical breakthroughs make it possible to use screen-printing method for all electrodes deposition in OTFT fabrication.

2. EXPERIMENTAL

The 125 μm thick poly(ethylenenaphthalate) (PEN) (Goodfellow) was employed as the substrate. Before the deposition, it was cleaned by ultrasonic bath in detergent, DI water and isopropanol. Fig. 1 hows the via hole printing process for double side printing of the substrate. The 50 μm thick Kapton tape was carefully stuck onto PEN surface without any bubbles in between. Via hole drilling was completed by CO_2 laser (Universal Laser System, VLS 2.30), wavelength of CO_2 laser is 10.6 μm. Kapton tape and PEN were penetrated at the same time, so for next step of via hole printing, Kapton tape acted as a protective shadow mask. Conductive via holes were made by doctor blading high viscosity screen-printing silver paste (RAFS 089, TOYOCHEM) across Kapton tape surface and then uncovered the protective tape.

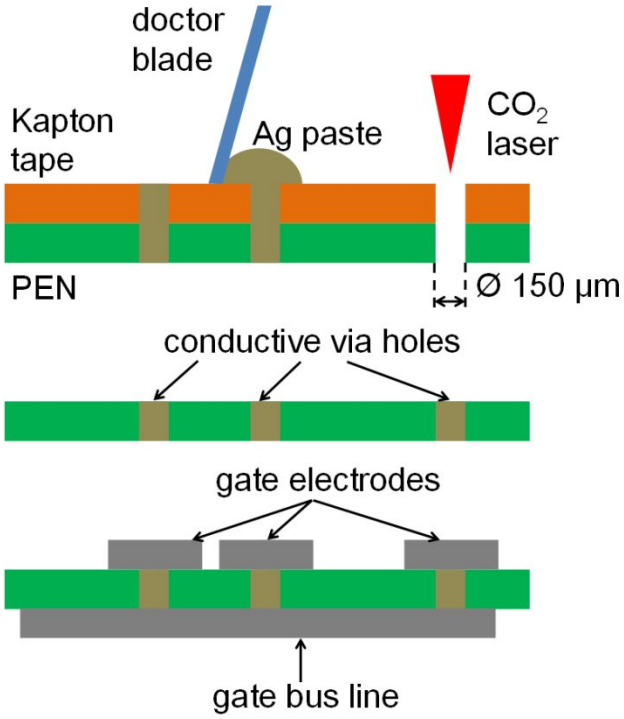

Figure 1. Via hole printing process for double side conductivity.

Screen-printing processes for gate electrodes and gate bus lines on both sides of PEN were completed by a home-made screen-printing stage through a screen with pre-defined pattern (ELECHEM TCHNOLOGY). After gate electrode deposition, the paste was naturally dried in ambient air for 2 hours to obtain good conductivity. Then para-chloroxylylene (parylene-C) was chosen as gate dielectric layer to offer good step coverage on gate electrodes. For single transistor fabrication, parylene-C layer thickness was set to 375 nm. For active matrix array fabrication, in order to

ensure a good successful yield, thickness of parylene-C layer was increased to 680 nm. The deposition process was performed by Labcoater PDS 2010 system (Specialty Coating Systems) and the thickness (measured by KLA Tencor P10 stylus profiler) was controlled by parylene-C dimer mass. The relationship between dimer mass and parylene-C layer thickness is in Fig. 2a. 300 mg, 600 mg, and 900 mg parylene-C dimer was added in the furnace, resulting parylene-C thickness of 70 nm, 375 nm and 680 nm, which showed perfect linear relationship between dimer mass and layer thickness. Capacitance measurement of parylene-C layer was done by Agilent 4294A Precision Impedance Analyzer, capacitance data can be found in Fig. 2b. In frequency range from 1 kHz to 1 MHz, capacitance relaxation is not obvious. Capacitance at 1 kHz was used for calculating transistor's mobility. The calculated dielectric constant for the parylene-C layer is 3.15.

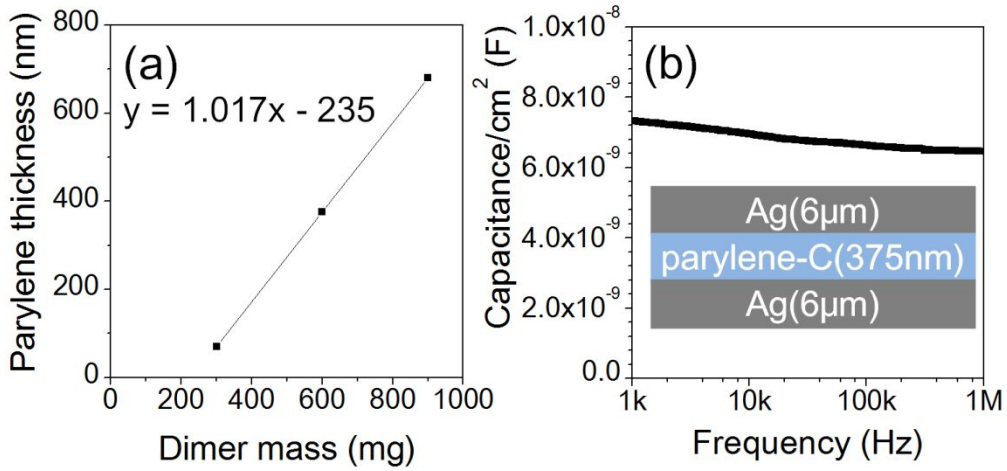

Figure 2. (a) Capacitance measurement of 375 nm thick parylene-C layer.

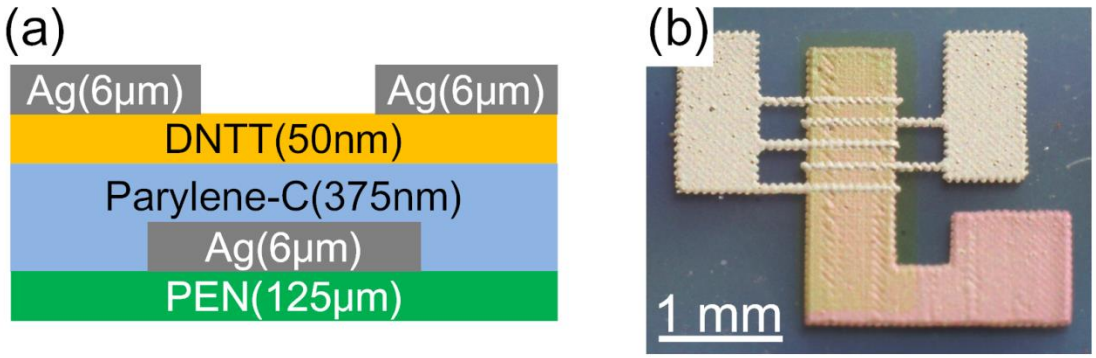

Figure 3. (a) Schematic drawing and (b) optical image of a transistor with all screen-printed electrodes, channel length and width are 150 μm and 3 mm, respectively.

After dielectric deposition, 50 nm dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) (Lumtec, Taiwan) was evaporated in thermal evaporation chamber (MiniBox, MOORFIELD) at base pressure below 10^{-6} torr. For first 5 nm

DNTT, evaporation speed was below 0.02 nm/s; and for next 45 nm, evaporation speed was 0.05-0.1 nm/s. Source and drain electrodes of OTFT were formed by another screen-printing process. Symmetric structure and optical image of a single OTFT can be found in Fig. 3. After fabrication process, the devices were dried by putting into vacuum vessel of glove box for at least 2 hours before characterizations. Current-voltage (I-V) curves were measured using Keithley 2636A and 2400 source meters. Electrical characterization was performed in Glove box (MBRAUN) with water and oxygen contents less than 0.1 ppm.

3. RESULTS AND DISCUSSION

The transfer and output curves of a representative transistor are shown in Fig. 4. The screen-printed transistor has a high mobility of 0.33 $cm^2V^{-1}s^{-1}$ and an on/off ratio larger than 10^6. At the same time, gate leakage current is as low as around 10 pA, corresponding to leakage current density of 8.55×10^{-9} A/cm^2 at electric field of 0.78 MV/cm. The leakage current density of parylene-C layer is lower than those of PMMA dielectric formed by spin-coating (9.8×10^{-7} A/cm^2) [12] and Al_2O_3 dielectric formed by atomic layer deposition (2×10^{-8} A/cm2) [13]. We believe electrical conductivity of printed electrodes and dielectric strength of parylene-C dielectric enhance the electrical performance of the transistors.

Fig. 5 shows volume resistivity of screen-printed Ag after 1 hour annealing in different annealing temperature. Results indicate that even just dried in room temperature, the volume resistivity of screen-printed silver is 60 times larger than bulk silver (1.6 μΩ cm) [2]. Consider the thickness ratio between screen-printed Ag and thermal evaporated Ag (6 μm to 50 nm), the overall conductance of screen-printed Ag electrode is at least 2 times better than that of 50 nm thermally evaporated Ag electrode.

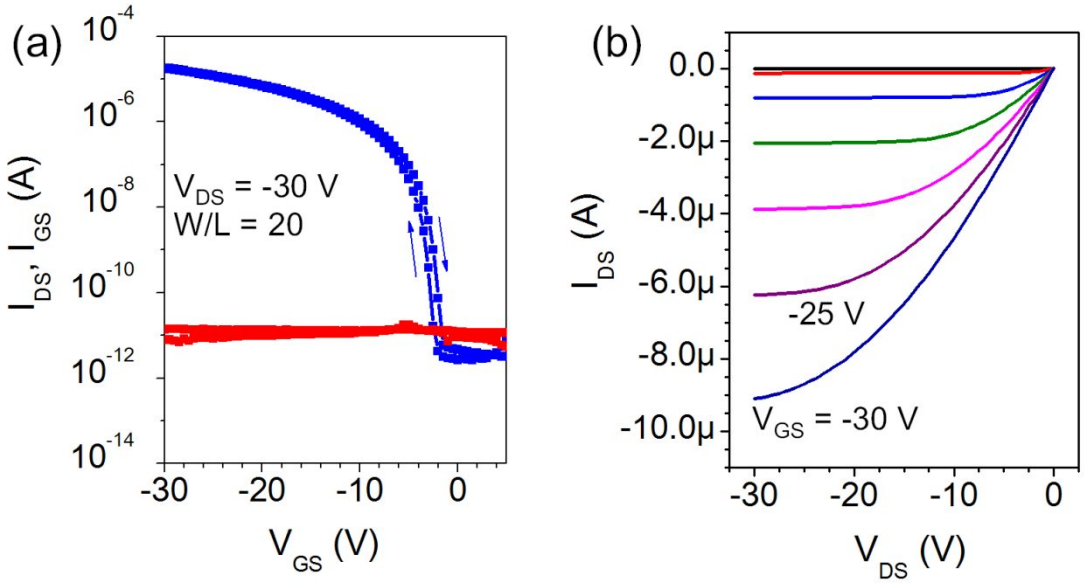

Figure 4. (a) Transfer curve of a single transistor. Blue line is drain to source current, mobility is 0.33 $cm^2V^{-1}s^{-1}$ and threshold voltage (V_{th}) is -3.2 V. Red line is gate to source leakage current. (b) Output curve of a single transistor, step size is -5 V

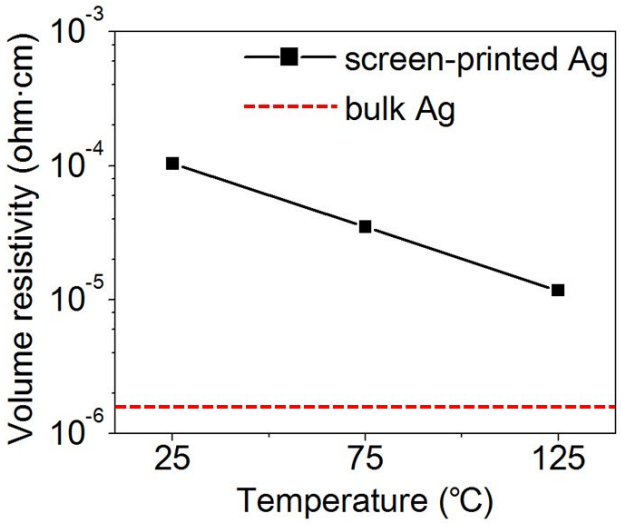

Figure 5. Volume resistivity of screen-printed Ag after annealing for 1 hour in different temperature.

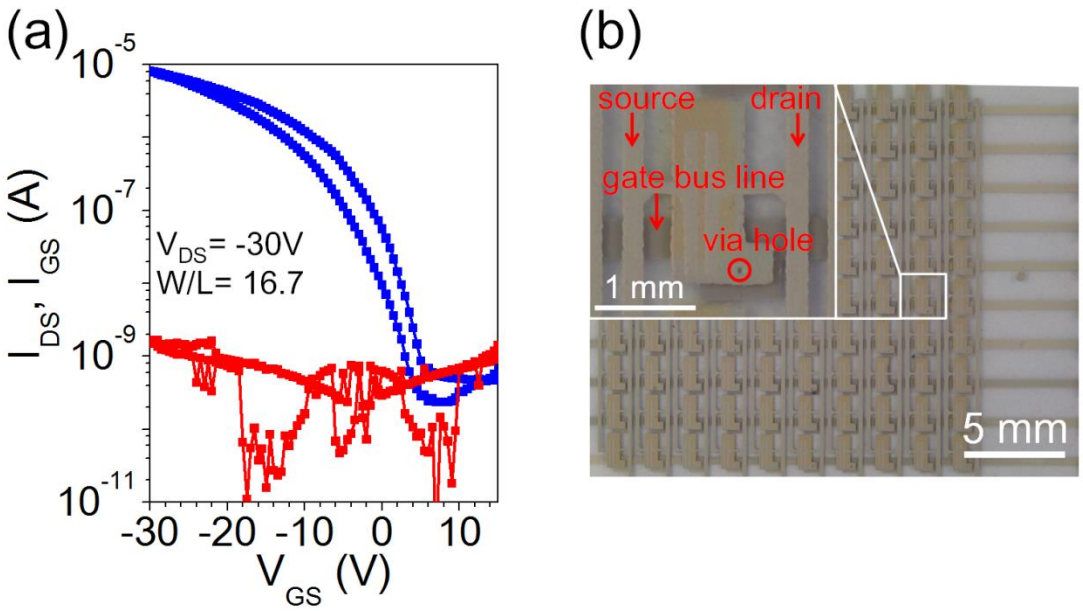

Figure 6. (a) Transfer curve of a transistor in active matrix array form. Blue line is drain to source current, mobility is 0.29 $cm^2V^{-1}s^{-1}$. Red line is gate to source leakage current. (b) Optical image of 10 ×10 active matrix transistor array, inset is magnified optical image of a single pixel. Channel length and width are 75 μm and 1250 μm, respectively. Gate bus line is on the opposite side of substrate.

Based on the fact of screen-printing technique, printing area as large as several m^2 is easy to achieve. Also the highly conductive printed electrodes are critical to large-area transistor array fabrication. Large-area transistor array is extremely critical to next generation flexible display as back panels. We demonstrate a 10 ×10 active matrix transistor array on PEN substrate. Single transistor dimension is only 2 mm ×2 mm with total area as 2 cm ×2 cm. Fig. 6a is the

optical image of 10 × 10 active matrix transistor array. Via hole structure is used for electrical connections between two sides of the substrate. The reason for using via hole structure is to avoid the overlap between gate bus lines and source/drain bus lines, thus largely decreasing possible leakage current paths. Fig. 6b is the transfer curve in active matrix form. Twenty out of one hundred transistors were tested, and average mobility was calculated to be 0.29 $cm^2V^{-1}s^{-1}$. On/off ratio slightly decreased to around 10^4 and leakage current also increased to around 1 nA. For the off current increase, it should be related to the active matrix construction where all source and drain electrodes of ten transistors in a column were connected together, thus off current was increased by around 10 times. For gate leakage current increase, seen from comparison between Fig. 3b and inset of Fig. 6b, the gate to source/drain overlap increased from single transistor to array form, which is the reason why leakage current increased to around 1 nA.

4. CONCLUSION

Transistor with all screen-printed electrodes was fabricated, offering a high mobility and a large on/off ratio. Parylene-C dielectric layer is used for gate dielectric, which offers perfect step coverage and block gate leakage current efficiently. With highly conductive electrodes, the contact resistance of the transistor is low. 10 × 10 active matrix transistor array was demonstrated. Pixel size of 2 mm × 2 mm and channel width of 75 μm indicated the potential of this method in flexible large-area scanning circuit fabrication for large-area sensor or display applications.

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