Improved memory characteristics by NH_3-nitrided GdO as charge storage layer for nonvolatile memory applications

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Charge-trapping memory capacitor with nitrided gadolinium oxide (GdO) as charge storage layer (CSL) is fabricated, and the influence of post-deposition annealing in NH_3 on its memory characteristics is investigated. Transmission electron microscopy, x-ray photoelectron spectroscopy, and x-ray diffraction are used to analyze the cross-section and interface quality, composition, and crystallinity of the stack gate dielectric, respectively. It is found that nitrogen incorporation can improve the memory window and achieve a good trade-off among the memory properties due to NH_3-annealing-induced reasonable distribution profile of a large quantity of deep-level bulk traps created in the nitrided GdO film and reduction of shallow traps near the CSL/SiO_2 interface. [http://dx.doi.org/10.1063/1.4737158]

In recent years, metal-oxide-nitride-oxide-silicon (MONOS) nonvolatile memory (NVM) has drawn attention due to its superior programming/erasing (P/E) speeds and easier dimension scaling compared with the conventional polycrystalline silicon floating-gate memory.[1] For satisfying the requirements of future NVMs, e.g., large memory window, low power consumption, and good data retention, high-k dielectrics, e.g., HfO_2,[2] AlN,[3] and Y_2O_3,[4] have been proposed to substitute Si_3N_4 as the charge storage layer (CSL) of MONOS memory due to their high charge-trapping capacity. It has been reported that gadolinium oxide (GdO) is a promising candidate as the gate dielectric of silicon,[5,6] particularly due to its small lattice mismatch (<0.5%) with Si (100).[7] The memory properties of GdO nano-crystal and Gd-incorporated HfO_2 dielectric as charge trapping layer have been investigated and reported.[8,9] On the other hand, it is generally believed that nitridation can induce a lot of electron traps,[10] and nitrogen incorporation can enhance the permittivity of the dielectric.[11] It is expected that good charge-trapping properties and dielectric performance could be achieved by using nitrided GdO as the CSL of memory device through appropriate post-deposition annealing (PDA). Therefore, in this work, nitrided GdO is prepared as the CSL of memory device and the effects of PDA conditions on nitrogen incorporation and thus memory performance are investigated. Under suitable annealing conditions, good memory characteristics are achieved for the MONOS memory capacitor with nitrided GdO as CSL.

MONOS and metal-nitride-oxide-silicon (MNOS) capacitors were fabricated on p-type Si wafers. After a standard RCA cleaning, SiO_2 was thermally grown in dry O_2 at 900 °C as the tunneling layer. GdO and nitrided GdO were deposited as the CSL by reactive sputtering of Gd_2O_3 target at an Ar/N_2 flow ratio of 2/0 or 2/1 and denoted as GN0 and GN1, respectively. Then, a PDA was carried out in N_2 ambient at 550 °C for 30 s. Also, some nitrided GdO samples were annealed in N_2 or NH_3 ambient at 550 °C for 2 min, denoted as GN2 and GN3, respectively. Next, Al_2O_3 was deposited as blocking layer (BL) by atomic layer deposition method by alternating deposition cycles of $Al(CH_3)_3$ and H_2O precursors at 300 °C for the MONOS capacitors only. Finally, Al was evaporated and patterned as gate electrode and also as back electrode, followed by forming-gas annealing in H_2/N_2 (5% H_2) at 300 °C for 20 min.

The electrical characteristics were measured by HP4284A LCR meter and HP4156A semiconductor parameter analyzer. The flat-band voltage (V_{FB}) of the samples was extracted by assuming $C_{FB}/C_{OX} = 0.5$ (C_{FB} and C_{OX} are the flat-band and oxide capacitances, respectively, determined from 1 MHz high-frequency C-V curve).

The cross-section and interface quality of the MONOS capacitors were examined by transmission electron microscopy (TEM), as shown in Fig. 1. It can be seen that thicknesses of the BL/CSL/SiO_2 layers are almost consistent for the four samples (13 nm/6 nm/3 nm), and the interfaces are clear. Moreover, no clear crystal grain or crystal lattice is observed except for the Si substrate. This is expected for amorphous SiO_2 and Al_2O_3 due to their high crystallization temperature. X-ray diffraction (XRD) analysis is done for these CSL films, as shown in Fig. 2(a). It can be seen that only the GN0 sample exhibits a weak cubic-Gd_2O_3 (200) peak, indicating that little cubic-phase Gd_2O_3 is formed after the PDA and no clear diffraction peaks are observed for the GN1, GN2, and GN3 samples, exhibiting amorphous diffraction pattern, which could be attributed to increased crystallization temperature due to nitrogen incorporation.

From the x-ray photoelectron spectroscopy (XPS) analysis, the composition of the CSL in the GN0, GN1, GN2, and GN3 samples is determined to be $Gd_{0.317}O_{0.683}$, $Gd_{0.368}O_{0.587}N_{0.045}$, $Gd_{0.349}O_{0.615}N_{0.036}$, and $Gd_{0.376}O_{0.580}N_{0.044}$, respectively. The reduced nitrogen content in the GN2 sample could be due to

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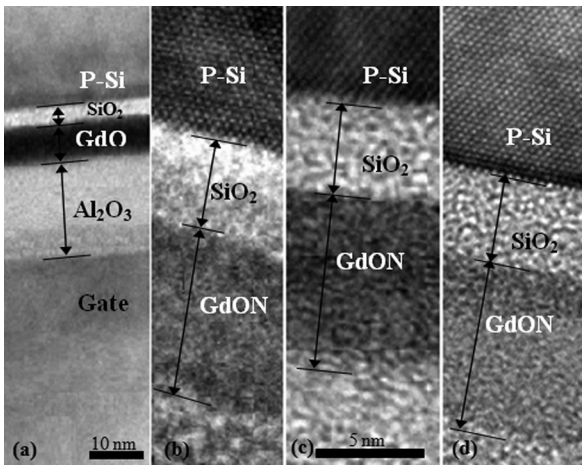

FIG. 1. TEM image of the stacked gate dielectric structure for the four samples: (a) GN0, (b) GN1, (c) GN2, and (d) GN3.

the escape of nitrogen atoms during the annealing in N_2 ambient for 2 min. However, new nitrogen atoms would be incorporated by the NH_3 annealing for the GN3 sample to compensate for the loss of nitrogen content. Fig. 2(b) shows the Gd 4*d* spectrum with two strong peaks as 4*d*5/2 and 4*d*3/2. Compared with the GN0 sample, the Gd 4*d* spectrum of the three nitrided samples displays a shift toward lower binding energy due to nitrogen incorporation and the shift is different for different N content. The spectrum of Gd 4*d*5/2 is deconvoluted into two components, denoted as x and y, respectively. The x peak with lower binding energy is correlated to Gd silicate. The reduced Gd content ratio in the x peak state from the GN0 sample to the GN3 sample (61%, 56%, 49%, and 46%) indicates that nitrogen incorporation during the sputtering and PDA with longer time, especially in NH_3 atmosphere, is effective in improving the structural and interface quality of the CSL due to suppressed formation of gadolinium silicate, e.g., Gd-Gd and Gd-Si bonds.[12]

The V_{FB} extracted from the 1 MHz C-V curve under different P/E voltages is shown in Fig. 3(a). The much larger memory window of the GN1 sample than that of the GN0 sample is observed, indicating that a large quantity of electron traps exists in the CSL of the GN1 sample due to nitrogen incorporation. The large negative flat-band shift of the GN0 sample under erasing operation could be attributed to more pre-existing hole traps in the CSL or generation of positive charges, induced by oxide and/or oxygen vacancies in the CSL.[13] The small negative shift of V_{FB} under erasing operation for the GN1, GN2, and GN3 samples implies that nitrogen incorporation into the GdO film could effectively reduce the oxygen defects and oxygen vacancies to some extent.[14] However, as the annealing time increases, the quantity of the traps in the CSL is reduced due to enhanced densification of the CSL film, thus resulting in a smaller memory window for the GN2 and GN3 samples than the GN1 sample. The larger memory window of the GN3 sample than that of the GN2 sample could be ascribed to creation of extra electron traps related to the hydrogen dissociated from the NH_3 gas.[15]

The charge-trap centroid from the metal/CSL interface (X_t, nm) is extracted using the MNOS capacitors with the same CSL as the GN0, GN1, GN2, and GN3 samples by the constant-current stress method[16]

$$X_t = t_{ox}\left(1 - \frac{\Delta V_{-g}}{\Delta V_{+g}}\right)^{-1}, \tag{1}$$

where t_{ox} is thickness of the gate dielectric and ΔV_{-g} and ΔV_{+g} are the negative and positive gate-voltage shifts. As shown in the inset of Fig. 3(a), the X_t moves towards the SiO_2 side as the constant-current stress increases, implying that the injected electrons tend to fill the traps near the gate side firstly, which is beneficial for the retention characteristics by avoiding electrons tunneling back to the substrate.

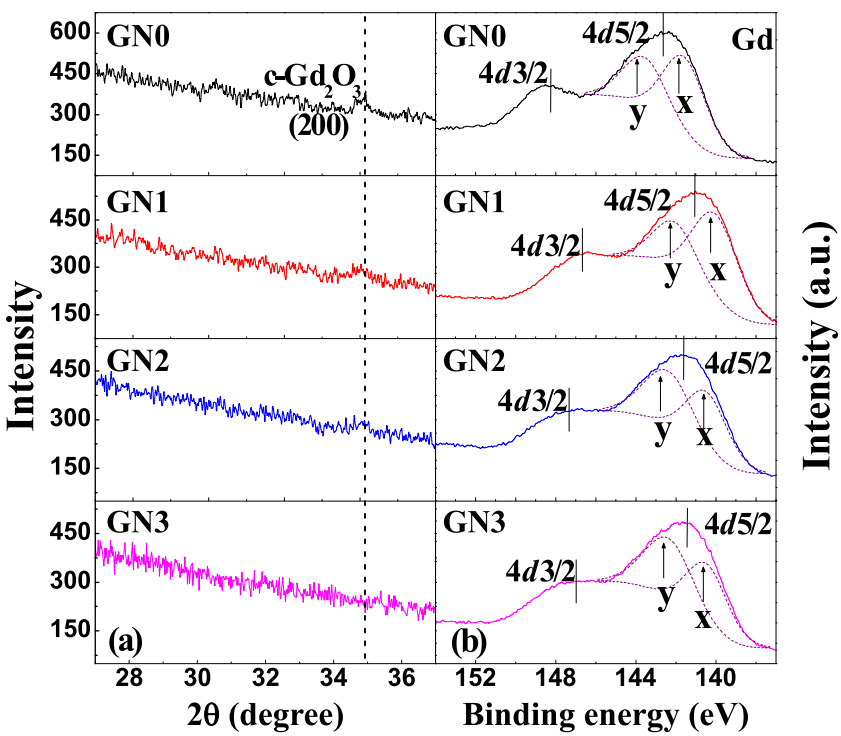

FIG. 2. XRD patterns (a) and Gd 4*d* XPS patterns (b) for the CSL film of the four samples.

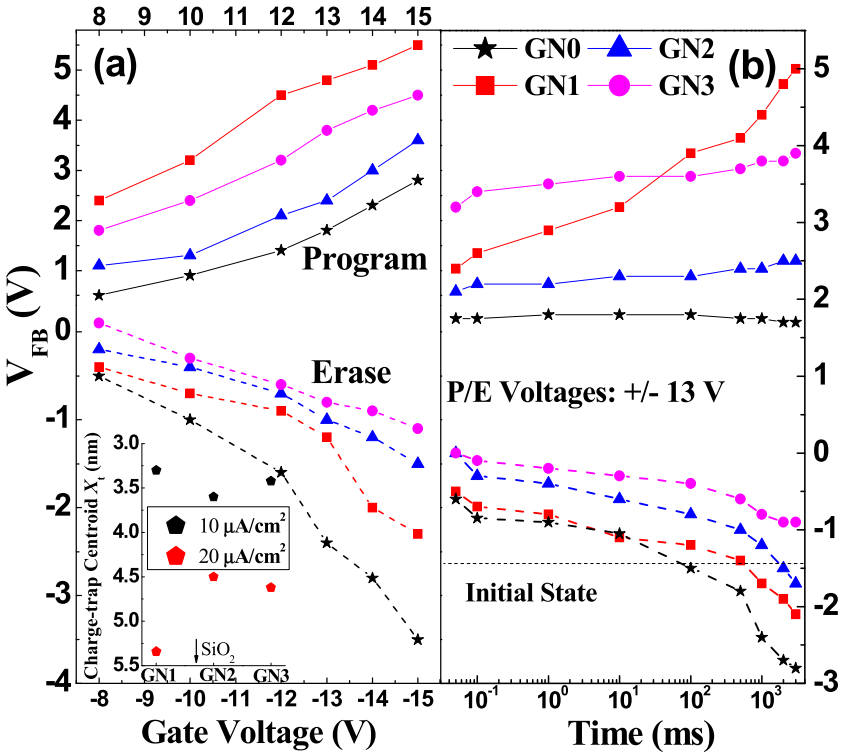

FIG. 3. The V_{FB} shift under different P/E voltages (a); in the inset charge-trap centroid and the change of V_{FB} as a function of P/E time (b).

Furthermore, the X_t of the GN1 sample under 20 μA/cm^2 constant-current stress is much closer to the SiO_2 side than that of the GN2 and GN3 samples. So, it could be suggested that for the GN1 sample, more traps in the CSL are close to the CSL/SiO_2 interface and are effectively passivated by longer annealing in N_2 or NH_3, while bulk traps are dominant for the GN2 and GN3 samples. Moreover, the largest X_t shift for the GN1 sample demonstrates its wider distribution of electron traps as compared to the GN2 and GN3 sample.

In Fig. 3(b), the V_{FB} shift of the samples as a function of P/E time is examined at P/E voltages of $\pm$13 V. For the GN0 sample, the shift of V_{FB} quickly reaches saturation during the initial 100 μs program time and is the minimum among the four samples, indicating a limited amount of electron traps, probably located near the CSL/SiO_2 interface. For the GN1 sample, the V_{FB} shift gradually increases and is smaller in the initial stage and larger after 10 ms than that of the GN3 sample, especially after 100 ms, a quick increase of V_{FB} shift occurs. The low programming speed for the GN1 sample further indicates that there is a wide distribution of electron traps in its CSL and more traps are located near the CSL/SiO_2 interface as mentioned above. For the GN2 and GN3 samples, the high programming speed and efficiency are associated with the high electron-trap density in the bulk of their CSL. For erasing operation, larger negative shift of V_{FB} occurs as erasing time increases and exceeds the initial

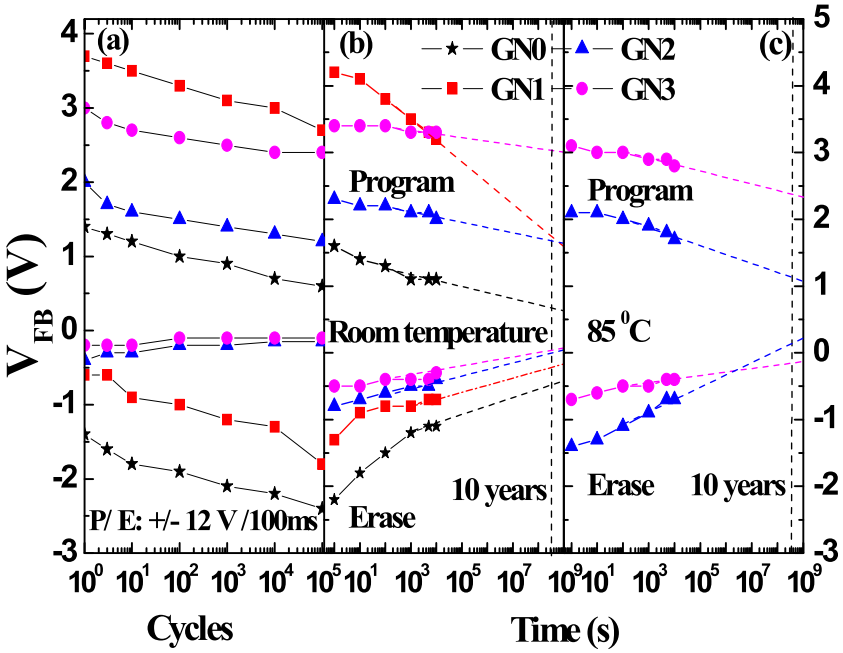

FIG. 4. Endurance (a) and retention characteristics at room temperature (b) or 85 °C (c) for the MONOS memory capacitors.

V_{FB} value after ~60 ms, ~500 ms, and ~1.5 s for the GN0, GN1, and GN2 samples respectively, resulting in an over-erase phenomenon. However, it is observed that the negative V_{FB} shift of the GN3 sample becomes saturated below the initial V_{FB} value after 2-s erasing with no over-erase phenomenon, indicating that the annealing treatment of the N-incorporated GdO in NH_3 is beneficial for suppressing the generation of excess hole traps and thus the over-erase phenomenon.

Fig. 4(a) is the endurance characteristics of the four samples. For the GN0 and GN1 samples, the gradual increase of the erasing window should be due to deep-level hole traps near the interface generated by the P/E stress, thus giving rise to accumulation of holes similar to the phenomenon in Ref. 17. For the GN2 and GN3 samples, the window exhibits a normal closing trend as the P/E cycle increases and is degraded by 45% and 21% after 10^5 P/E cycles, respectively. These indicate that the nitrogen incorporation during the reactive sputtering cannot effectively suppress the generation of interface states near/at the CSL/SiO_2 and SiO_2/Si interfaces during the P/E stress. However, this problem can be solved since the defects and undesired states in the dielectric and at the CSL/SiO_2 interface can be eliminated by the NH_3 annealing,[18] and thus their qualities are improved due to reduction of Gd silicates, and some nitrogen is incorporated at/near the SiO_2/Si interface, which produce stronger chemical bonds.

Figs. 4(b) and 4(c) show the retention characteristics of the samples after removing 100 ms P/E voltages at ±13 V. In Fig. 4(b), the initial memory window is 3.8 V, 5.5 V, 3.1 V, and 4.0 V and become 1.2 V, 2.0 V, 1.7 V, and 3.0 V for the extrapolated 10-year memory window with the initial-window loss of 68%, 64%, 45%, and 25% for the GN0, GN1, GN2, and GN3 samples, respectively. For the GN0 sample, the high loss rate of charges for the erased state in the initial 10 s could be attributed to the excessive hole traps (as mentioned above), which are at shallow energy levels and close to the CSL/SiO_2 interface, thus affecting the stability of the erasing window. Because the electrons in deep traps have lower activation energy comparing with those in shallow traps so that they have a lower probability of directly tunneling to the states at SiO_2/Si interface.[8,19] In programmed state, the GN2 and GN3 samples display better retention characteristics of electron charges with a lower loss rate of 26% and 12%, respectively, as compared with 56% and 58% of the GN0 and GN1 samples, respectively. This could be ascribed to the reduced shallow-level and interfacial traps and increased deep-level bulk traps, which should be more immune to tunneling of electrons back to the substrate, achieved by the longer annealing or incorporation of more nitrogen. As compared to the GN2 sample, the better charge retention of the GN3 sample even at 85 °C in Fig. 4(c) should be attributed to the recapture of de-trapping electrons by a wider and deeper distribution of trap levels in the CSL bulk.[20]

Nitrided GdO as charge storage layer of MONOS memory capacitor has been prepared by nitrogen-reactive sputtering and the effects of PDA on the characteristics of the memory capacitors have been investigated. It was found that the memory window was greatly improved due to a large quantity of electron traps generated in the GdO CSL by N incorporation. Furthermore, a good trade-off among the memory window, P/E speed, endurance, and retention characteristics has been achieved by using an NH_3 annealing at 550 °C for 2 min. These are attributed to nitridation-induced deep-level electron traps in the bulk of the CSL, their suitable spatial distribution, and reduction of shallow traps near the CSL/SiO_2 interface. In addition, the over-erase phenomenon gets effectively suppressed through the NH_3 annealing. Therefore, nitrided GdO dielectric with post-deposition annealing in NH_3 is a promising candidate as the charge storage layer of advanced MONOS nonvolatile memory devices.

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