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Impacts of Ti on electrical properties of Ge metal–oxide–semiconductor capacitors with ultrathin high-*k* LaTiON gate dielectric

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Abstract Ge Metal–Oxide–Semiconductor (MOS) capacitors with LaON gate dielectric incorporating different Ti contents are fabricated and their electrical properties are measured and compared. It is found that Ti incorporation can increase the dielectric permittivity, and the higher the Ti content, the larger is the permittivity. However, the interfacial and gate-leakage properties become poorer as the Ti content increases. Therefore, optimization of Ti content is important in order to obtain a good trade-off among the electrical properties of the device. For the studied range of the Ti/La_2O_3 ratio, a suitable Ti/La_2O_3 ratio of 14.7% results in a high relative permittivity of 24.6, low interface-state density of 3.1×10^{11} $eV^{-1}\,cm^{-2}$, and relatively low gate-leakage current density of 2.0×10^{-3} $A\,cm^{-2}$ at a gate voltage of 1 V.

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1 Introduction

As the Si-based metal-oxide-semiconductor field-effect transistor (MOSFET) is approaching its physical limit, germanium MOSFETs with high-permittivity (high-*k*) gate dielectric (e.g. ZrO_2 [1], HfO_2 [2–4], and Al_2O_3 [5]) are extensively discussed as alternative candidates for future complementary MOS technology due to the high carrier mobilities of germanium [6–8]. However, the growth of unstable and water-soluble germanium oxide during deposition and post-deposition annealing hinders the fabrication of competitive Ge-based MOS devices [9, 10]. To overcome this problem, various techniques including NH_3 surface treatment [2–5] and Si interlayer [11, 12] have been applied in Ge-based MOS devices to enhance device performances. Recently, it was reported that rare-earth metal oxides such as CeO_2 [13, 14], Gd_2O_3 [15] and Dy_2O_3 [16] produced promising electrical properties when directly in contact with Ge. Especially, La_2O_3 thin film shows many advantages, including low interface-states density, very small frequency dispersion and hysteresis due to formation of stable lanthanum germanate (La–Ge–O) [16–18]. However, a relatively low permittivity due to Ge diffusion into the high-*k* dielectric prevents further decrease in equivalent oxide thickness [17].

Ti incorporation has been studied by several groups to increase the permittivity of Hf-based oxides because of the extremely high relative permittivity (k) of Ti-based oxides (∼80) [19, 20]. Higher permittivity has been obtained with Ti incorporation while leading to a gate-leakage increase [21]. On the other hand, N incorporation in HfO_2 results in beneficial characteristics including reduction of gate-leakage current, improved thermal stability of the dielectric material, due to suppression of the onset of dielectric crystallization [22, 23]. In view of the above two effects

on Hf-based oxides, it is expected that better dielectric properties could be achieved by simultaneously incorporating Ti and N into La_2O_3 thin film. Therefore, in this work, capacitors with LaTiON gate dielectric are fabricated and the impact of Ti content on the electrical properties of the capacitors is carefully examined. It is found that some electrical properties, e.g. k value, interface-state density, gate-leakage current and device reliability, strongly depend on the Ti content incorporated in the La_2O_3 gate dielectric. When Ti content is set at an optimal value, a good trade-off among the electrical properties can be obtained.

2 Experiments

The used Ge substrate was (100) Sb-doped n-type Ge wafers with a resistivity of $0.10 \sim 0.11\ \Omega\,\text{cm}$. The wafers were cleaned in organic solvents, and lastly with de-ionized water rinsing followed by 30-s diluted HF (1:50) dipping for several cycles to remove the native oxide. After drying in N_2, LaON thin film was deposited by sputtering of La_2O_3 target at a power of 30 W in Ar and N_2 ($Ar{:}N_2 = 24{:}6$) ambient at room temperature (denoted as LON). In order to investigate the impact of Ti content on the electrical properties of the capacitors, Ti was added into the LaON thin film by reactive co-sputtering of Ti and La_2O_3 targets with different Ti-target powers (11.7 W, 17.4 W, 26.1 W and 33.3 W) as shown in Table 1 (denoted as LTON1, LTON2, LTON3 and LTON4, respectively). All LaTiON films have roughly the same thickness ($7.5 \sim 7.8$ nm). A post-deposition annealing (PDA) was carried out in N_2 ambient with a flow rate of 500 ml/min at 500°C for 5 min. Subsequently, Al was evaporated and patterned by lithography as gate electrodes with an area of $A = 7.85 \times 10^{-5}\ \text{cm}^{-2}$, followed by a forming-gas annealing at 300°C for 20 min.

High-frequency (HF, 1-MHz) capacitance–voltage (C–V) curves were measured by HP4284A precision LCR meter. Gate-leakage current was measured by HP4156A precision semiconductor parameter analyzer. Physical thickness of the gate dielectrics was determined by a multi-wavelength ellipsometer and TEM. High-field stress ($10\ \text{MV}\,\text{cm}^{-1}$ for 3600 s), with the capacitors biased in accumulation by the HP 4156A, was used to examine the device reliability in terms of gate-leakage increase and flatband-voltage shift. All electrical measurements were carried out under a light-tight and electrically-shielded condition at room temperature.

Table 1 Preparation conditions and physical thickness of the gate dielectrics. The Ti/La_2O_3 ratio is calculated from the ratio of the deposition rates of Ti (at different sputtering powers) and La_2O_3 (at a sputtering power of 30 W) in the same $Ar{:}N_2 = 24{:}6$ ambient

Sample	Ti-target power (W)	Physical thickness (nm)	Ti/La_2O_3 (%)
LON	–	8.05	–
LTON1	11.7	7.47	7.3
LTON2	17.4	7.55	14.7
LTON3	26.1	7.60	23.8
LTON4	33.3	7.83	34.0

3 Results and discussion

The Ti content of the dielectric films is evaluated by the Ti/La_2O_3 ratio, which is calculated from the ratio of the deposition rates of Ti (at different sputtering powers) and La_2O_3 (at a sputtering power of 30 W) in the same $Ar{:}N_2 =$ 24:6 ambient, to represent the relative amount of Ti in the dielectric films.

Figures 1(a) and (b) show the TEM pictures of the LON and LTON2 samples, respectively. It can be seen that the interlayer between the high-k dielectric and Ge substrate can be hardly observed in the two samples. This is ascribed to the N incorporation, which inhibits O diffusion and thus suppresses the formation of interlayer [24]. Comparing the two TEM pictures, it can be found that the interface is rougher for the LTON2 sample than the LON sample. A possible reason is that the incorporated Ti in LaTiON thin film strongly reacts with Ge at the surface of the Ge substrate [21].

Typical HF C–V curves of the samples are depicted in Fig. 2. The four Ti-incorporated samples have larger accumulation capacitances (C_{ox}) than the LON sample, with larger C_{ox} for higher Ti-target power (thus higher Ti content), implying larger k value and thus smaller capacitance equivalent thicknesses (CET) can be obtained for higher Ti content (LTON4 sample has the largest k value of 30.8 and smallest CET of 1.0 nm), as shown in Table 2. This should be attributed to an increase of Ti-based oxide in the LaTi-based oxide for higher Ti content, because Ti-based oxide has larger k value than La-based oxide. However, the

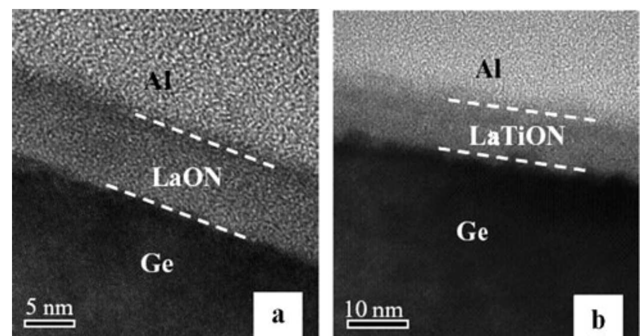

Fig. 1 TEM images of (**a**) LaON/Ge (LON), (**b**) LaTiON/Ge (LTON2) capacitors

Table 2 Electrical parameters of the n-Ge MOS capacitors without or with Ti incorporation, extracted from 1-MHz C–V curves

Sample	C_{ox} (pF)	CET (nm)	V_{fb} (V)	Q_{ox} (cm^{-2})	D_{it} ($eV^{-1}\,cm^{-2}$)	k
LON	129	2.1	0.19	-8.5×10^{11}	1.2×10^{11}	14.9
LTON1	173	1.6	0.30	-2.7×10^{12}	2.4×10^{11}	18.6
LTON2	227	1.2	0.34	-4.3×10^{12}	3.1×10^{11}	24.6
LTON3	252	1.1	0.40	-6.0×10^{12}	1.2×10^{12}	27.5
LTON4	274	1.0	0.46	-7.2×10^{12}	4.1×10^{12}	30.8

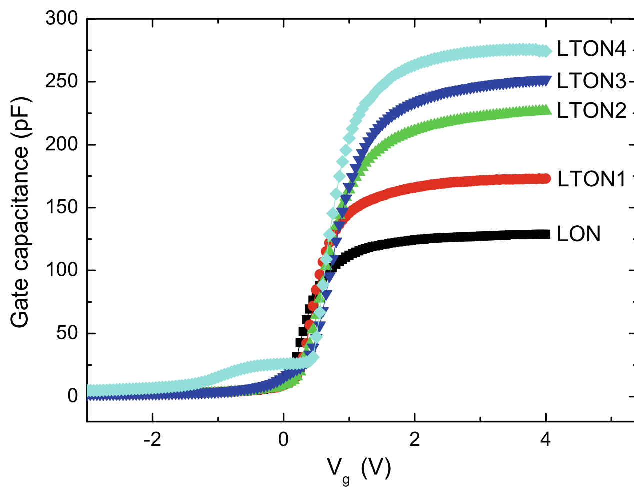

Fig. 2 High-frequency (1-MHz) C–V curves for the n-Ge MOS capacitors without or with Ti incorporation

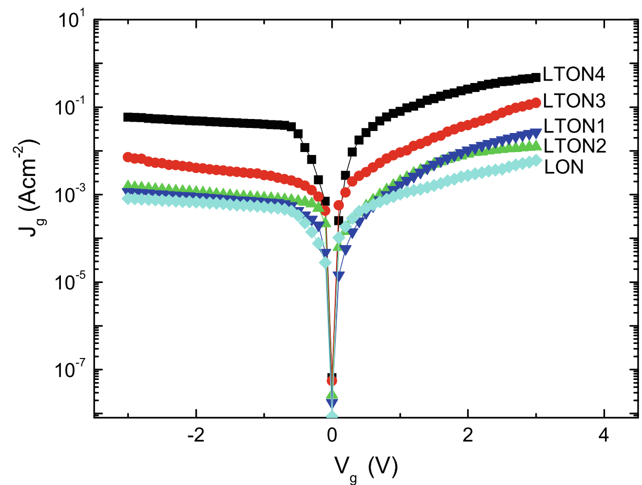

Fig. 3 Gate-leakage current density (J_g) vs. gate voltage (V_g) for the n-Ge MOS capacitors without or with Ti incorporation

interface-state density (D_{it}) increases with Ti content, which is obvious from the distorted C–V curves of the LTON3 and LTON4 samples. This is confirmed by the extracted D_{it} near midgap using Terman's method [25] for the purpose of comparison, with the largest D_{it} for the LTON4 sample ($4.1 \times 10^{12}\ eV^{-1}\,cm^{-2}$), as shown in Table 2. This is probably associated with the fact that stronger reaction between the Ge substrate and LaTiON film could happen as the Ti content increases, similar to the situation of HfTiO in contact with Ge [21]. The higher equivalent oxide-charge density (Q_{ox}) of the Ti-incorporated samples should be mainly due to the high oxide charges near the interface and interface trap charges. The negative Q_{ox} indicates that these traps could be acceptor-like interface and near-interface traps due to the Ge diffusion from the substrate into the high-k layer and the reaction between Ge and Ti near the interface. So, a trade-off consideration between k and D_{it} is necessary when Ti is added into LaON, e.g. for our studied range of Ti-target power, a sputtering power of 17.4 W (LTON2 sample) seems to be suitable, producing a relatively high-k value (24.6) and relatively low D_{it} ($3.1 \times 10^{11}\ eV^{-1}\,cm^{-2}$). Further optimization of the Ti content is necessary for obtaining better trade-off among the device properties.

The gate-leakage properties of the samples are illustrated in Fig. 3. Obviously, the Ti-incorporated samples exhibit larger gate-leakage current than the LON sample, and the higher the Ti content, the larger is the gate-leakage current. The gate-leakage current density (J_g) of the LTON4 sample is $8.1 \times 10^{-2}\ A\,cm^{-2}$ at $V_g = 1$ V, which is nearly 80 times higher than that of the LON sample ($1.0 \times 10^{-3}\ A\,cm^{-2}$) and 40 times higher than that of the LTON1 sample ($1.7 \times 10^{-3}\ A\,cm^{-2}$), although they have almost the same gate-dielectric thickness. This should be closely related to the gradually deteriorated quality of the dielectric/Ge interface as the Ti content increases (see Table 2 and Fig. 2). For the LTON2 sample with relatively few interface defects, an acceptably small J_g of $2.0 \times 10^{-3}\ A\,cm^{-2}$ can be obtained at $V_g = 1$ V.

In order to investigate the device reliability, a high-field stress at 10 $MV\,cm^{-1}$ for 3600 s is performed on the capacitors, with the samples biased in accumulation. Their HF (1-MHz) C–V curves and gate-leakage currents before and after the stress are measured. The shift of flatband voltage ($\triangle V_{fb}$) extracted from the C–V curve and the increase of gate-leakage current density ($\triangle J_g$) at $V_g = 1$ V are summarized in Fig. 4. Obviously, the four Ti-incorporated samples

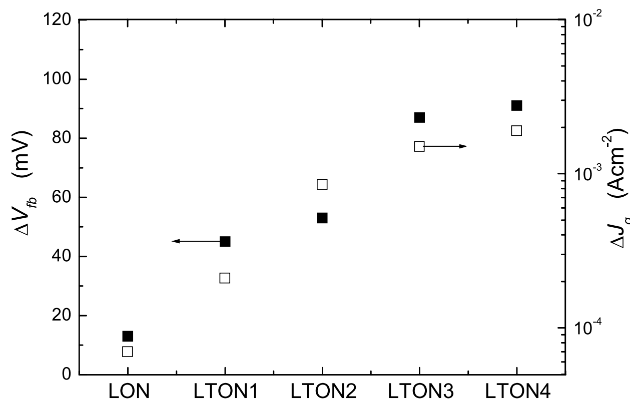

Fig. 4 Flatband-voltage shift ($\triangle V_{fb}$) and gate-leakage increase ($\triangle J_g$) at $V_g = 1$ V for the n-Ge MOS capacitors without or with Ti incorporation after a high-field stress (at 10 MV/cm for 3600 s)

have larger $\triangle V_{fb}$ and $\triangle J_g$ than the LON sample, which should be attributed to the poor interface quality associated with Ti-induced defects [26]. So, the Ti-target power and thus Ti-content control is the key for excellent electrical properties of the LaTi-based gate-dielectric MOS devices.

4 Conclusions

The effects of Ti incorporation into LaON gate dielectric on the electrical properties of MOS capacitors have been investigated. Results indicate that Ti addition can significantly increase the k value and decrease *CET* due to the extremely high permittivity of Ti-based oxides, but deteriorate the dielectric/Ge interface quality, and thus gate leakage properties and device reliability due to Ti-induced defects. Therefore, the Ti content incorporated into LaON has to be carefully chosen to achieve a good trade-off between the k value and D_{it}. For our Ti-incorporated samples, a suitable Ti/La_2O_3 ratio of 14.7% leads to a high k value of 24.6, low interface-state density of 3.1×10^{11} $eV^{-1}\,cm^{-2}$, relatively low gate-leakage current density of 2.0×10^{-3} $A\,cm^{-2}$ at $V_g = 1$ V and good device reliability.

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