Electrical Modelling of Temperature Distributions in On-chip Interconnects, Packaging, and 3D Integration

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***Abstract*— In this talk, we will introduce a novel methodology using existing electromagnetic modelling tools for interconnect and packaging structures to simulate and model the temperature distribution without major modifications to these tools or simulated structures. This methodology can easily be integrated with the chip technology information and frame an electrical circuit simulator into an automatic, template-based simulation and optimization flow.**

A new accurate closed-form thermal model is further developed to simplify unnecessary object details. The model allows an equivalent medium with effective thermal conductivity (isotropic or anisotropic) to replace details in non-critical regions accurately so that complex interconnect structures can be simulated at a system level. Using these techniques, we demonstrate the modelling capability of very complex on-chip interconnects, packaging, and 3D integration technologies.

I. Introduction

With the shrinking size of silicon devices, both passage current density and effective copper resistivity in VLSI are rising [1]. The thermal resistances from metal wires to the silicon substrate are higher due to the inclusion of more metal layers and low permittivity materials in the backend. Meanwhile, to improve the VLSI performance and heterogeneous integration of technologies on a single die, 3D integration technologies are being pursued [2]. Because device layers are stacked on top of each other, 3DI faces more serious thermal challenges. Hence, the Joule heating due to the passage current in on-chip interconnect, packaging and 3DI vias are becoming more important. It leads an additional temperature rises on top of the junction temperature or the temperature near the silicon surface. Without considering these effects, many reliability degradations could be easily underestimated, such as temperature dependent electromigration, stress migration and inter-metal dielectric leakage.

Efficient thermal analysis in complex VLSI problems with the consideration of every entity (such as wires, vias, substrate, and multiple dielectrics) has not been demonstrated. Most methodologies used by industries are implemented in standalone tools, which can only handle relatively small size problems and are difficult to be integrated with existing EDA design flows. Some methods are using approximate analytical models for thermal analysis [2]-[4]. Although one can obtain results quickly through these analytical models, their certain deficiencies have to be solved.

Recently, a methodology was developed by exploiting the well known analogy between electrical and thermal problems [5]. It produces a general fast 3D thermal analysis engine for on-chip interconnect, packaging and 3DI using an existing electrical resistance extraction tool [6]. It is naturally compatible with the IC design environment, where electrical analysis is dominant. However the approximation in [5] that treats the power consuming wire as a single equal potential port is not valid if the temperature gradient along the wire cannot be ignored. To solve this issue, the non-equal potential port is introduced. This paper further pursues a novel and accurate empirical model to allow isotropic and anisotropic equivalent medium replacement of the non-critical region details with minimal error. Thermal analysis of realistic and complex interconnect stacks using proposed methods are subsequently demonstrated.

II. Simulation Methodology

A brief workflow of the proposed method is shown in Fig. 1. It starts from obtaining layout geometries and material properties. A model for electrical analysis (E Model) is generated. If the problem size is too large, non-critical details are replaced by equivalent media. Then thermal boundary conditions, such as heat sources and heat sinks, are added to form a thermal model (T Model). Using an electrical resistance solver [6], the thermal model is processed by the electrical resistance solver to generate either the temperature profile or the thermal resistance network in the SPICE netlist.

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The basic idea behind the methodology is based on the equivalence between the static electrical Laplace equation and the steady state heat conduction equation. The first one is expressed as:

$$\nabla \cdot J_{el} = \nabla \cdot (-\sigma_{el} \nabla \phi) = 0 \quad (1)$$

where J_{el} is the electrical current density; σ_{el} is the electrical conductivity; ϕ is the electrical potential. The heat conduction equation is written as:

$$\nabla \cdot J_{th} = \nabla \cdot (-\kappa_{th} \nabla T) = p \quad (2)$$

where J_{th} is the heat flux density; κ_{th} is the thermal conductivity; T is the temperature; p is the heating power density. It is clear that T is analogous to ϕ, J_{th} is analogous to J_{el}, and κ_{th} is analogous to σ_{el}; the thermal resistance is analogous to the electrical resistance.

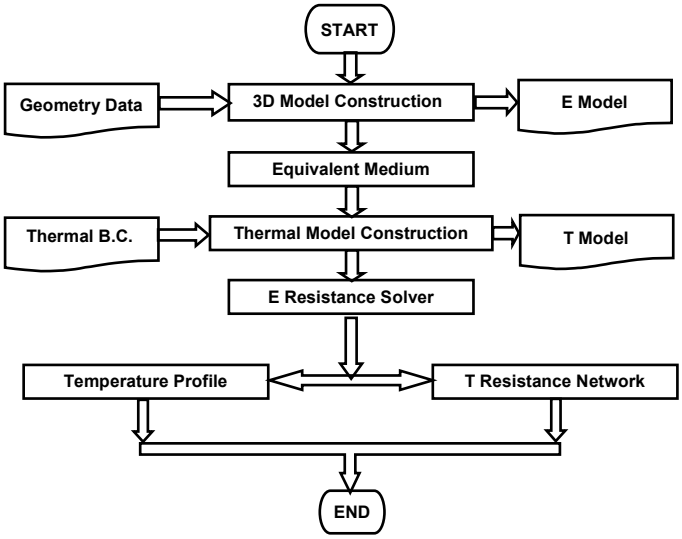


Fig. 1. Flowchart illustrating various steps in the 3D thermal simulation using an electrical (resistance extraction) solver.

Thermal boundary conditions are realized using electrical sources in the resistance solver. There are several important thermal boundary conditions that have to be replaced by limited source options. The constant temperature boundary condition, the most popular one for the ambient temperature setup, is represented by a voltage source. If only the current source is allowed in the resistance solver, a very small parallel resister has to be added to create a voltage source. Another boundary condition is the heat density per unit area, which can be easily replaced by the current source. However, because of limited thermal conductivities, the non-equal potential (temperature) distribution has to be guaranteed. Hence, a series of current sources instead of one is added to enable the heat density boundary condition. The third thermal boundary condition is the Joule heating boundary condition. Obviously it is a function of wires' resistivity and current. Its implementation needs the pre-calculation of consumed power of metal segments and then sets the heat density boundary condition according to current directions.

Hence, it is feasible to develop a fast thermal analysis engine for on-chip interconnect, packaging, and 3DI using existing electrical resistance solvers. There is another reason driving this effort: the thermal-electrical coupling effect. The temperature rise increases the material resistivity according to the temperature coefficient of resistance (TCR). This changes the current distribution and power consumption (Joule heating) inside conductors. In return it alters the temperature profile. Hence, the workflow in Fig. 1 shall be a closed loop instead of an open loop. The temperature profile output shall be fed back to update the material property. New power consumption of wire segments must be modified. An iterative process is required for a true steady state result if Joule heating is centric to the problem. We have done this work through collaborations with Georgia Institute of Technology (GIT). Significant changes were observed over the closed loop iteration. Because we are using the same solver, meshing and solving processes could be correlated and optimized easily. Hence, a unified solver is preferred.

An electrical resistance solver (IBM RGEN) using the finite difference method (FDM) is employed for the proposed thermal analysis. Validation studies have been conducted through canonical benchmarks against theoretical formula and a popular commercial tool [2][3][5]. Excellent agreements have been achieved. There are trade-offs between accuracy and computation time in both tools. However, to achieve the same accuracy, RGEN based analysis was much faster than some commercial tools. It should be noticed that RGEN does not depend on manual meshing. But the manual mapped meshing of some commercial tool requires manually definition of the object mesh in a correct order, which definitely is not feasible for complex VLSI problems. Meanwhile our proposed methodology can be easily integrated with VLSI EDA workflows. Actually this work has been implemented into our cross-platform 3DI thermal map generation flow smoothly and seamlessly.

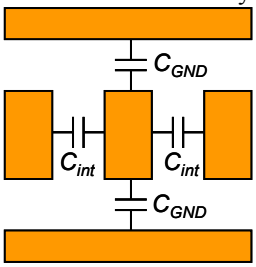


Fig. 2. Schematic plot of the capacitance model with two ground planes.

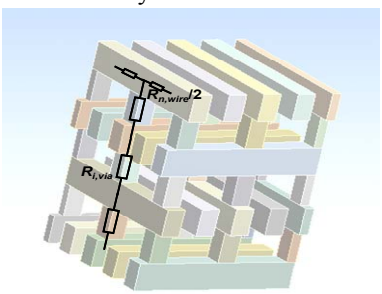


Fig. 3. Schematic plot of a backend interconnect stack (source: [3]).

III. Equivalent Thermal Conductivity Approximation

To further reduce the computation time and memory usage, an equivalent medium with effective thermal conductivity κ_{eff} can be used to replace the detailed metal fills in non-critical regions. This idea was also introduced in [1] and [4]. However,

those analytical models are not comprehensive enough for practical needs.

Our novel model is based on the fact that the electrostatic and thermal problems have similar physical nature. The electrostatic Poisson's equation is expressed as

$$\nabla \cdot D = \nabla \cdot (-\varepsilon \nabla \phi) = \rho \tag{3}$$

where D is the electrical displacement flux; ε is the material permittivity; ρ is the charge density. The similarity between (2) and (3) shows that the thermal conductance is analogous to the electrical capacitance. But it requires that the majority electric field is within bonding dielectrics if we take advantage of corresponding capacitance problems. Or the analogy will require 0 relative permittivity since the electrical potential field can penetrate the vacuum. Since most VLSI problems meet this requirement, the interconnect capacitance models can be used for thermal analysis. It indicates that a capacitance solver could help to establish the thermal resistance network under the above assumption, too.

An interconnect capacitance model is shown in Fig. 2. The empirical interconnect capacitance model in [7] is chosen. The wire-to-ground capacitance per unit length (C_{GND}) is written as

$$C_{GND}/\varepsilon = w/t_{ILD} + 1.086\left(1 + 0.68e^{-t_{wire}/1.343d} - 0.9964e^{-d/1.421t_{ILD}}\right) \cdot \left[d/(d+2t_{ILD})\right]^{0.0476} \left(t_{wire}/t_{ILD}\right)^{0.0337} = func(w, t_{wire}, t_{ILD}, d) \tag{4}$$

$$\left(\text{for } 0.3 \le w/t_{ILD} \le 10, 0.3 \le d/t_{ILD} \le 10, 0.3 \le t_{wire}/t_{ILD} \le 10\right)$$

where t_{ILD} is the distance between wire and ground; t_{wire} is the wire thickness; w is the wire width; d is the wire spacing. It should be noticed that the temperature gradient in metal wires are much lower than that in dielectric due to very high metal thermal conductivity. Substituting C_{GND}/ε with $1/\kappa_{Diel}R_{w2g}$, we can get

$$1/\kappa_{th}R_{w2g} = func(w, t_{wire}, t_{ILD}, d) \tag{5}$$

Hence, the total unit area thermal resistance for a Manhattan interconnect stack can be expressed as

$$R_{total} = \sum_{i=1}^{n-1}\left[R_{i,no\text{-}vias}/(1-f)\right] \| \left(A_{i,via}R_{i,via}/f\right) + \left[R_{n,no\text{-}vias}/(1-f)\right] \| \left[A_{i,via}\left(R_{n,via} + R_{n,wire}/4\right)/f\right] \tag{6}$$

where n is the number of metal wire layers; i stands for the i^{th} layer; $R_{i,no\text{-}vias} = R_{w2g}(w + d)$ is the unit area thermal resistance between the i^{th} and the $(i\text{-}1)^{th}$ wire layers when vias are not considered; $R_{i,via} = (t_{i,ILD} + t_{i,wire}) / \kappa_{metal}A_{i,via}$ is the via thermal resistance of the i^{th} ILD layer; $R_{n,wire}$ is the thermal resistance of top layer wire between two vias; $A_{i,via}$ is the via area of i^{th} layer; f is the via density. The schematic plot of the model structure is shown in Fig. 3.

TABLE I
RESULTS OF UNIT AREA THERMAL RESISTANCE WITHOUT VIAS USING DIFFERENT NUMERICAL OR ANALYTICAL METHODS

	Wire density = 0.5		Wire density = 0.167	
	Thermal resistance R_{total} (K-mm^2/W)	Error w.r.t. [3]	Thermal resistance R_{total} (K-mm^2/W)	Error w.r.t. [3]
Simulation [3]	4.1		5.7	
Model in [1]	3.90	-4.9%	3.92	-31.3%
Model in [4]	4.69	14.4%	13.14	130.5%
Our Model	3.97	-3.2%	6.26	9.8%

Fig. 4. Zoomed in view of a 45 nm technology backend structure. The monitored V_{DD} wire is from x = 0 µm, y = –125 to 125 µm, z = 1.296 µm. The monitored S4 wire is from x = 0.938 µm, y = –125 to 125 µm, z = 1.296 µm

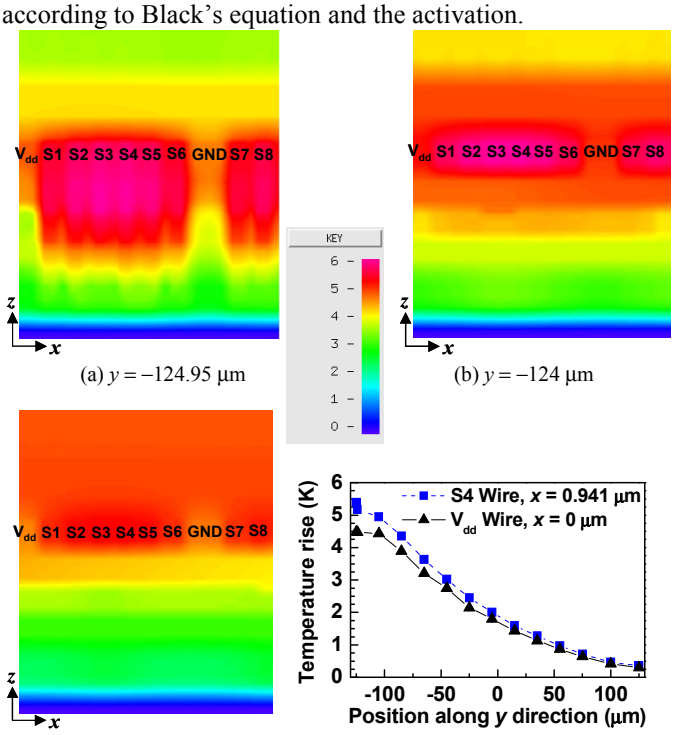
Table I compares our empirical model with the analytical methods from [1] and [4] for a no via case. The simulation data from [3] are used as the reference. It is seen that our model gives much better accuracy.

IV. THERMAL GUIDELINE STUDY OF A 45NM VLSI STACK

As a demonstration, a complex 45 nm technology backend stack was analyzed using the method proposed in Fig. 4, which shows a zoomed view. The width and length of the structure are 2.28 µm ($0 \le x \le 2.28$ µm) and 330 µm (-165 µm $\le y \le$ 165 µm) respectively. Seven interconnect layers are included. The self-heating effect of a practical backend stack can be evaluated by analyzing the thermal profile of this intermediate structure because: (a) a structure with adiabatic boundary condition remains equivalent if it is mirrored to a symmetrical structure and duplicated periodically (this structure can be mirrored to -2.28 µm $\le x \le 0$ and duplicated periodically); (b) layer 8 and above do not have a non-negligible effect on the thermal profile if the self-heating of 5th layer is studied. In this work, 8 signal wires (250 µm long) in the 5th wire layer and their vias are injected with the root mean square (RMS) current. The maximum temperatures of an excited signal wire and a neighbor victim V_{DD} wire are monitored. The reason for monitoring the victim V_{DD} is that the power wires (V_{DD} and GND wires) are more vulnerable to electromigration because of polarized current stress. The current in signal wires is obtained through the electrical backend simulation. To drive the signal wire, an inverter with 2.6 µm wide NMOS and 4.4 µm wide PMOS is used to drive another inverter with 7.8 µm wide NMOS and 13.2 µm wide PMOS. The RMS current is not uniform along the wire. This is because more current is required to charge and discharge the interconnect capacitance at the input of signal wires (or at the output of the previous stage CMOS driver).

There are about 15 million meshed unknowns for the simulation while the computation time is 6.3 hours. The simulation results are shown in Fig. 5. The maximum temperature rise is 5.6 K in the heated signal vias for *S4* wire. The maximum temperature rise in the victim V_{DD} wire is 4.4 K,

which can have significant impact on EM lifetime degradation. The corresponding degradation in the mean time to failure (MTTF) of the victim V_{DD} wire is 19.3% at a junction temperature of 343 K (MTTF at 347.4 K w.r.t. 343 K) according to Black's equation and the activation.



(a) $y = -124.95$ µm (b) $y = -124$ µm

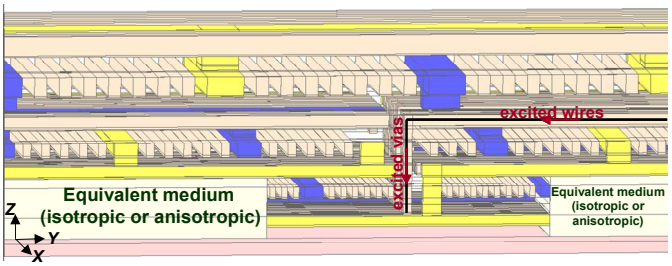
(c) $y = -95$ µm (d) Along the wires

Fig. 5. Cross section of temperature profiles at (a) signal via region ($y = -124.95$ µm); (b) 1 µm away from the signal vias ($y = -124$ µm); (c) 30 µm away from the signal vias ($y = -95$ µm); (d) the temperature distribution along an excited signal wire with maximum temperature rise ($x = 0.938$ µm) and the victim V_{DD} wire ($x = 0$ µm) in the same metal layer ($M5$ layer). (Temperatures are referred to the bottom heat sink with T_{ref})

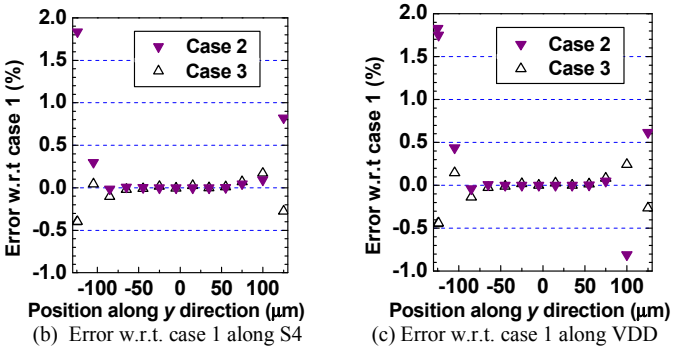
The heat dissipation in y direction is not ignorable for regions close to (< 40 µm) signal vias. For such a situation, equivalent media with anisotropic thermal conductivities can be applied. As an accuracy verification, three cases (Fig. 6.a) are compared (assume Vn is the via layer between Mn and Mn-1 layer in Fig. 4.): case 1 replaces structures from V1 to V3 that are 40 µm away from signal vias using equivalent isotropic media; case 2 replaces structures from V1 to V3 that are 1.7 µm away from the signal vias using equivalent isotropic media; case 3 replaces structures from V1 to V3 that are 1.7 µm away from signal vias using anisotropic media. As shown in Fig. 6.b and Fig. 6.c, regarding case 1 result as the reference, case 3 shows much better accuracy than that of case 2. And the computation time of case 3 is comparable to case 2.

V. SUMMARY

In this work, an efficient and accurate thermal profile acquisition method for complex VLSI interconnect, packaging and 3DI structures is achieved by using purely electrical simulations and modeling approaches. Then we developed a novel accurate empirical thermal model from the electrical capacitance model. The empirical thermal model has been used in deriving the equivalent media to replace complex but non critical regions. Excellent agreements have been achieved by using the proposed methods. For practical design purposes, the thermal profile of a 45nm backend interconnect structure has been solved.



(a) Equivalent medium replacement of Fig. 4.



(b) Error w.r.t. case 1 along S4 (c) Error w.r.t. case 1 along VDD

	S4		VDD		Computation time (hour)
	ΔTmax (K)	Error w.r.t. case 1	ΔTmax (K)	Error w.r.t. case 1	
Case 1	5.5767	-	4.4945	-	6.3
Case 2	5.7225	2.61%	4.5763	1.82%	3.2
Case 3	5.5537	-0.41%	4.4746	-0.44%	4.0

(d) Comparison of accuracy and computation time

Fig. 6. (a) Backend structure shown in Fig. 4 is modified by equivalent media for regions that are 1.7 µm away from signal vias. For both isotropic (case 2) and anisotropic (case 3) replacement, the error w.r.t. case 1 (Fig. 5.d) of temperature distribution along (b) an excited signal wire (S4) with maximum temperature rise (x = 0.938 µm) and (c) the victim VDD wire (x = 0 µm) in the same metal layer (M5 layer). The accuracy and computation time of the three cases are summarized in (d).

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