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Comparative Study of HfTa-based gate-dielectric Ge metal–oxide–semiconductor capacitors with and without AlON interlayer

J.P. Xu · X.F. Zhang · C.X. Li · C.L. Chan · P.T. Lai

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Abstract The electrical properties and high-field reliability of HfTa-based gate-dielectric metal–oxide–semiconductor (MOS) devices with and without AlON interlayer on Ge substrate are investigated. Experimental results show that the MOS capacitor with HfTaON/AlON stack gate dielectric exhibits low interface-state/oxide-charge densities, low gate leakage, small capacitance equivalent thickness (∼1.1 nm), and high dielectric constant (∼20). All of these should be attributed to the blocking role of the ultrathin AlON interlayer against interdiffusions of Ge, Hf, and Ta and penetration of O into the Ge substrate, with the latter effectively suppressing the unintentional formation of unstable poor-quality low-k GeO_x and giving a superior AlON/Ge interface. Moreover, incorporation of N into both the interlayer and high-k dielectric further improves the device reliability under high-field stress through the formation of strong N-related bonds.

1 Introduction

Germanium (Ge) is a promising alternative candidate for future channel material because of its 4× higher mobility for hole and 2× higher mobility for electron comparing to silicon [1–3]. However, unlike Si oxide, the thermodynamically unstable and soluble Ge oxide hinders the development of high-performance Ge metal–oxide–semiconductor field-effect transistor (MOSFET). A thin germanium oxynitride (GeO_xN_y) interlayer formed by rapid thermal nitridation or low-temperature plasma nitridation prior to deposition of high-k dielectric has been demonstrated to improve the interface properties of Ge MOS devices [4–6]. Bai et al. [7] have shown that surface nitridation can suppress GeO_x growth and hence achieve a small equivalent oxide thickness (EOT) with low leakage current, while HfO_2 gate-dielectric Ge MOS capacitor without surface nitridation exhibited both large EOT and high leakage current density. Although a stable and smooth interface with improved electrical properties has been obtained by inserting a thin GeO_xN_y layer between high-k dielectric and germanium substrate, lower k value of GeO_xN_y interlayer limits further scalability of Ge MOS devices. Recently, to avoid the low-k GeO_x interlayer, Kim et al. [8] have demonstrated that atomic layer deposition of insulating nitride layers (AlN: $k \sim 9$ and Hf_3N_4: $k \sim 20$) on Ge prior to high-k oxide formation could effectively passivate the Ge surface and increase the k value of gate dielectrics. In fact, AlN is easy to react with oxygen to form Al oxynitride [9]. So, oxidation of AlN would happen probably prior to Ge oxidation, thus effectively suppressing the formation of GeO_x. In this work, using reactive sputtering method, we comparatively study the electric properties and microstructures of HfTa-based gate dielectrics with and without an AlON interlayer. Ta is intentionally added to improve the crystallization temperature and dielectric constant of Hf-based oxide and oxynitride [10]. Improved electrical properties are obtained for the samples with AlON interlayer as compared to those without it.

J.P. Xu · X.F. Zhang
Department of Electronic Science & Technology, Huazhong University of Science and Technology, Wuhan 430074, People's Republic of China

C.X. Li · C.L. Chan · P.T. Lai (✉)
Department of Electrical & Electronic Engineering, The University of Hong Kong, Pokfulam Road, Hong Kong, Hong Kong
e-mail: laip@eee.hku.hk
Fax: +852-25598738

2 Experiments

N-type (100) Ge wafers with a resistivity of 0.040∼0.047 Ω cm were cleaned using trichloroethylene, acetone, and ethanol and rinsed with DI water for several times, followed by 15-s diluted HF (1:50) dipping and 15-s DI water rinse for five cycles to remove Ge native oxide. After drying in N_2, the wafers were immediately transferred into Denton Vacuum Discovery Deposition System. First, a ∼1-nm AlN_x interlayer was deposited by reactive sputtering of Al in an Ar/N_2 (12:18) ambient followed by the deposition of a 5-nm HfTaO or HfTaN by cosputtering of Ta and Hf in an Ar/O_2 (24:3) or Ar/N_2 (24:6) ambient, respectively (denoted as HfTaO/AlON or HfTaON/AlON samples). For deposition of HfTaN, a larger N_2 ratio was used to incorporate more nitrogen in the dielectric. For comparison, a 5-nm HfTa or HfTaN was directly deposited on the cleaned Ge substrate without the AlN_x interlayer to form the control samples (denoted as HfTaO or HfTaON samples). A post-deposition annealing (PDA) was carried out in wet N_2 (500 ml/min) at 500°C for 5 min to transform the films into oxides or oxynitrides (i.e., HfTaO, HfTaON and AlON) by using the oxygen in the water vapor [11]. The wet-N_2 atmosphere was realized by bubbling pure N_2 through deionized water at 95°C with a flow rate of 500 ml/min. Subsequently, Al was evaporated and patterned by lithography as gate electrode with an area of $A = 7.85 \times 10^{-5}$ cm^{-2}. Finally, forming-gas annealing was performed at 280°C for 20 min.

High-frequency (HF, 1-MHz) capacitance–voltage (C–V) characteristics were measured at room temperature using HP4284A precision LCR meter. Gate-leakage current was measured by HP4156A precision semiconductor parameter analyzer. Structure of the films was determined by transmission electron microscopy (TEM). Physical thickness of the gate dielectrics was determined by a multiwavelength ellipsometer and TEM. A high-field stress at 10 MV/cm for 3600 s, with the capacitors biased in accumulation by HP 4156A precision semiconductor parameter analyzer, was used to examine device reliability in terms of gate-leakage increase and flat-voltage (V_{fb}) shift after the stress. All electrical measurements were carried out under light-tight and electrically-shielded conditions.

3 Results and discussion

Typical HF C–V curves of the MOS capacitors with and without AlON interlayer, measured at 1 MHz and 100 kHz, are shown in Fig. 1. As can be seen, small frequency dispersion is observed except for the HfTaO sample implying lower interface-state density. The accumulation capacitance or oxide capacitance (C_{ox}), physical oxide thickness (t_{phys}), capacitance equivalent thickness (CET), and equivalent k value ($= C_{ox} t_{phys}/\varepsilon_0 A$) for the samples are extracted from the HF C–V curves and listed in Table 1. A distortion is observed in the region from depletion to inversion of the C–V curves for the two samples without the AlON interlayer (especially for the HfTaO sample) but does not exist for the two samples with the AlON interlayer. This difference is obviously associated with the AlON interlayer. For the HfTaO sample, significant interfacial defects are probably created due to formation of GeO_x or strong interdiffusion and reaction between the HfTaO dielectric and Ge substrate due to the absence of the AlON interlayer, which is illustrated to some extent by the rough interface shown in Fig. 2b, while a smooth and distinct interface is formed for the HfTaO/AlON stack gate dielectric due to the blocking role of the AlON interlayer against interdiffusion of species

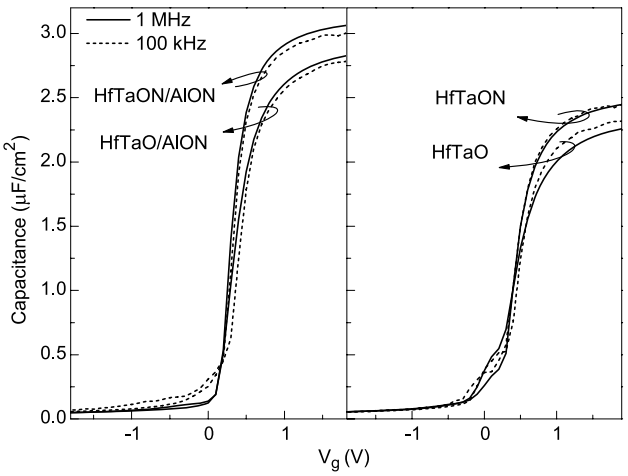

Fig. 1 Typical high-frequency (1 MHz) C–V curve of the Ge MOS capacitors with and without AlON interlayer. The *solid line* is the ideal HF C–V curve

Table 1 Parameters of the Ge MOS capacitors extracted from HF C–V curves and physical thicknesses t_{phys}'s of the high-k and interfacial layers determined from TEM images (the second value for the HfTaO and HfTaON samples is for the unintentional GeO_x interfacial layer)

Sample	HfTaO/AlON	HfTaON/AlON	HfTaO	HfTaON
C_{ox} (pF)	225	243	181	195
t_{phys} (nm)	5.00/0.88	5.08/0.81	5.06/0.90	5.14/0.92
CET (nm)	1.2	1.1	1.5	1.4
Equivalent k	19.0	20.9	15.4	17.0
D_{it} (eV^{-1} cm^{-2})	7.5×10^{11}	7.4×10^{11}	2.5×10^{12}	1.6×10^{12}
Q_{ox} (cm^{-2})	-1.7×10^{12}	-1.6×10^{12}	-2.2×10^{12}	-2.2×10^{12}

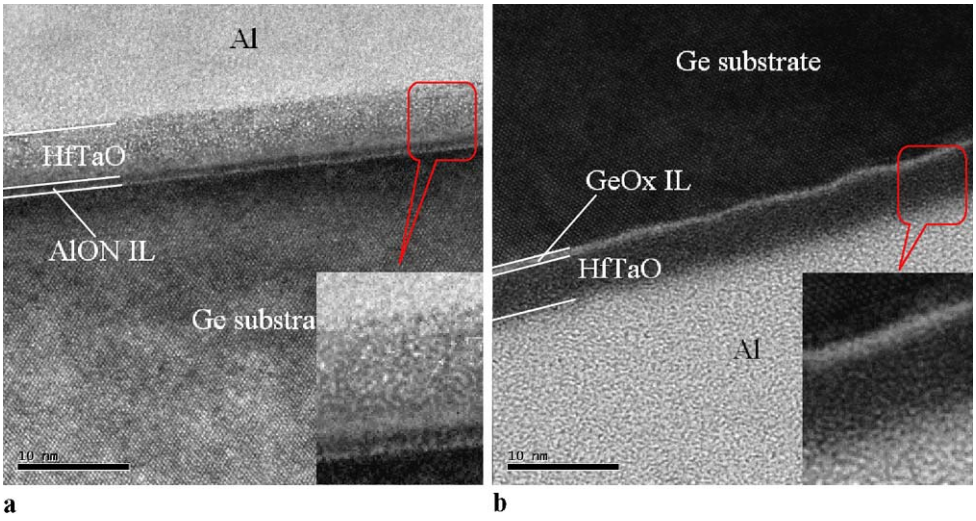

Fig. 2 TEM images of (**a**) HfTaO/AlON sample and (**b**) HfTaO sample

(see Fig. 2a). Therefore, it can be suggested that the AlON interlayer can effectively block the interdiffusion and reaction between the HfTa-based dielectric and Ge substrate and thus effectively passivate the Ge surface. It should be noted that C_{ox} of the oxynitrides is larger than that of their oxide counterparts, which leads to larger k value for the oxynitrides (e.g., the largest k value of 20.9 and the smallest CET of 1.1 nm for the TaHfON/AlON sample) than the oxides ($k = 15.4$ and $CET = 1.5$ nm for the HfTaO sample) under almost the same physical thickness. Similar phenomenon is also mentioned by Lysaght et al. [12]. From the TEM images in Fig. 2, it is can be seen that no crystallization occurs in the dielectrics, which is probably attributed to the breaking of the periodic crystal arrangement or the inhibition of continuous crystal growth in the gate dielectric by incorporating Ta into Hf-based oxide or oxynitride, thus increasing the crystallization temperature [10] and improving the thermal stability of the gate stack. The equivalent oxide-charge density ($Q_{ox} = -C_{ox}(V_{fb} - \varphi_{ms})/q$, where the work-function difference φ_{ms} between Al gate and n-Ge substrate is calculated to be 0.0706 V) and the interface-state density near midgap (D_{it}) estimated by the Terman's method [13] are also listed in Table 1. As compared to the control samples, D_{it} is obviously reduced by inserting a thin AlON interlayer between the high-k gate dielectric and Ge substrate. Moreover, smaller Q_{ox} is also obtained for the two samples with the AlON interlayer comparing to the control samples, especially for the HfTaON/AlON sample. These demonstrate that the AlON interlayer plays a key role as a barrier against penetration of oxygen into the Ge substrate and outdiffusion of Ge during the high-temperature annealing, greatly suppressing the formation of a GeO_x interlayer and thus reducing D_{it} and Q_{ox}. The negative Q_{ox} should be mainly related to the wet-annealing ambient [14]. The origin of the negative charges might be OH^-, which cannot diffuse out from the interface at an annealing temperature below 550°C [15].

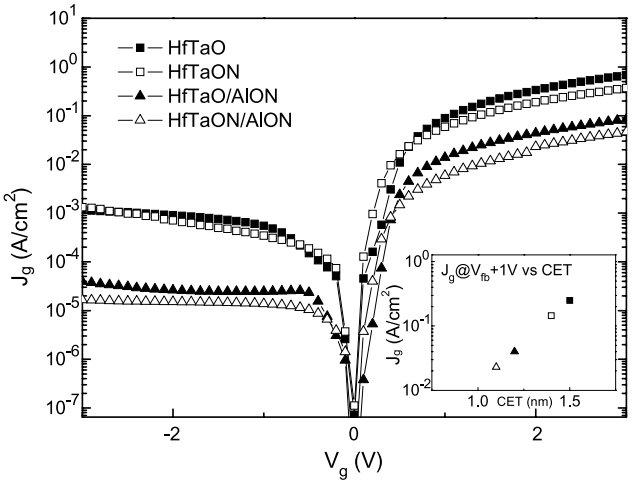

Fig. 3 Gate leakage current density of the Ge MOS capacitors, with $J_g@V_{fb} + 1$ V vs. CET shown in the *inset*

Figure 3 shows the gate leakage properties of the samples. The two samples with the AlON interlayer have lower leakage current than their control samples, while the leakage current of the oxynitride samples is smaller than their oxide counterparts, with the smallest and largest leakage current densities (5.9×10^{-3} and 8.9×10^{-2} A cm^{-2} at $V_g = V_{fb} + 1$ V) for the HfTaON/AlON and HfTaO samples, respectively. It was reported that the incorporation of nitrogen into high-k dielectrics could reduce gate leakage current by inhibiting interdiffusion of species and changing local coordination of high-k material and thus suppressing onset of crystallization [12]. Therefore, the smaller leakage current for the oxynitride samples should be ascribed to N incorporation.

A high-field stress at 10 MV/cm [$= (V_g - V_{fb})/t_{phys}$] for 3600 s, with the capacitors biased at accumulation, is used to examine the reliability of the samples. The I_g–V_g property is measured before and after stressing the samples, as

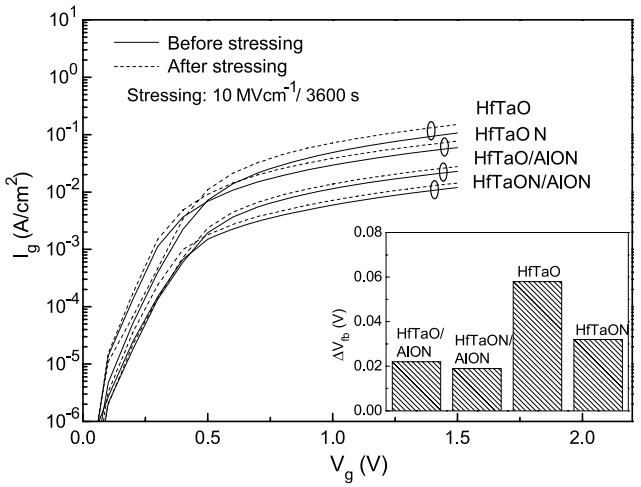

Fig. 4 Gate-leakage increase of the Ge MOS capacitors after a high-field stressing at 10 MV/cm for 3600 s, with the samples biased at accumulation. The *inset* shows the flat-band-voltage shift of these samples after the stress

shown in Fig. 4. The V_{fb} shift after stress is extracted from the HF C–V curves measured before and after stressing and is shown in the insert of Fig. 4. Increases of the leakage current and flat-band voltage after the stress are larger for the control samples than the samples with the AlON interlayer due to growth of an unstable GeO_x at the high-k dielectric/Ge interface of the former. Among the samples, the HfTaON/AlON sample exhibits the best reliability due to the formation of strong N-related bonds by significant incorporation of N in both the interlayer and high-k gate dielectric.

4 Conclusions

In conclusion, a thin AlON interlayer between high-k dielectric and Ge substrate deposited by reactive sputtering can give largely improved device performances due to its strong barrier role against species diffusions of Hf, Ta, Ge, and O and its good interface properties with the Ge substrate. Moreover, the electrical properties and high-field reliability of the devices are further improved by using nitrided high-k dielectric due to N incorporation and thus formation of strong N-related bonds. Therefore, the HfTaON/AlON stack dielectric is a promising gate structure for making high-performance Ge-based MOSFET.

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