Electrical properties of HfTiON gate-dielectric metal-oxide-semiconductor capacitors with different Si-surface nitridations

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Electrical properties of HfTiON gate-dielectric metal-oxide-semiconductor (MOS) capacitors with different Si-surface nitridations in N_2O, NO, and NH_3 prior to high-k film deposition are investigated and compared. It is found that the NO-nitrided sample exhibits low interface-state density and gate leakage current, and high reliability. This is attributed to formation of a SiON interlayer with suitable proportions of N and O. The MOS capacitor with $Hf_{0.4}Ti_{0.6}O_xN_y$/SiON gate dielectric stack (capacitance equivalent thickness of 1.52 nm and k value of 18.9) prepared by NO surface nitridation has an interface-state density of 1.22×10^{11} cm^{-2} eV^{-1} and gate leakage current density of 6×10^{-4} A cm^{-2} ($V_g=1$ V). Moreover, only a small degradation of electrical properties after a stressing at 10 MV/cm for 3000 s is observed for the NO-nitrided sample. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2767177]

Development of high-k gate dielectric for future complimentary metal-oxide-semiconductor (CMOS) devices is indispensable for achieving both low leakage current and small equivalent oxide thickness.[1] Among various kinds of high-k materials, HfO_2 (Ref. 2) receives more and more attention for the forthcoming CMOS technology due to its good compatibility with Si, such as suitable band gap offset with Si and higher carrier mobility for Hf silicates compared with other high-k materials.[3] Addition of Ti in Hf oxide can form Hf/Ti-based oxide or oxynitride with higher k value because Ti oxide has higher k value than Hf oxide.[4] Therefore, it is expected that HfTiON used as the gate dielectric of a MOS device should increase its k value. In order to avoid the formation of a low-k interlayer between the high-k gate dielectric and Si substrate during deposition and postdeposition annealing, it is important to form an interlayer with suitable contents of N and O. In this work, nitridations of Si surface in N_2O, NO, and NH_3 ambients prior to HfTiON deposition are investigated and compared. It is found that the NO-nitrided $Hf_{0.4}Ti_{0.6}O_xN_y$ gate-dielectric MOS capacitor exhibits excellent electrical properties and reliability, and gives a capacitance equivalent thickness (CET) of 1.52 nm and a k value of 18.9.

MOS capacitors with HfTiON as high-k gate dielectric were fabricated on (100)-oriented n-type Si wafers with a resistivity of 0.07 Ω cm. After RCA cleaning, the wafers were put in diluted HF for 1 min to remove the native SiO_2. Surface pretreatment was performed at 700 °C for 1 min in N_2O, NO, and NH_3 ambients (500 ml/min) (denoted as N_2O, NO, and NH_3 samples, respectively). Then, the wafers were immediately transferred to the vacuum chamber of vacuum discovery deposition system made by Denton Corporation. A HfTiN film was deposited at room temperature by cosputtering of a Hf target at 25 W rf power and a Ti target at 33 W dc power in an $Ar/N_2=24/6$ ambient, with 60 mTorr igniting pressure and 6.6 mTorr sputtering pressure. Next, the samples were transferred in air to a postdeposition annealing (PDA) system. The PDA was performed in N_2 (500 ml/min) at 700 °C for 30 s to transform HfTiN into HfTiON by consuming the residual oxygen in the N_2 ambient[5] and PDA system. Control sample with surface pretreatment in N_2 was also fabricated with the same sputtering and PDA conditions. Al was thermally evaporated and patterned using lithography technology as the gate electrode with an area of 7.85×10^{-5} cm^2. Also, Al was evaporated as the back electrode of the MOS devices to decrease contact resistance. Finally, all samples were annealed at 400 °C in forming gas ($N_2/H_2=95/5$) for 25 min.

High-frequency (1 MHz) C-V curves were measured at room temperature using HP4284A precision *LCR* meter. Flatband voltage (V_{fb}) and oxide-charge density (Q_{ox}) were extracted from the high-frequency C-V curves. The interface-state density (D_{it}) at midgap was also extracted from the high-frequency C-V curve using the Terman method.[6] High-field stress (10 MV/cm for 3000 s), with the capacitors biased in accumulation by HP4156A precision semiconductor parameter analyzer, was used to examine device reliability in terms of flatband-voltage shift (ΔV_{fb}) and gate-leakage increase. All measurements were carried out under a light-tight and electrically shielded condition.

The C-V curves of the samples with different surface nitridations are measured, as shown in Fig. 1. The NO and N_2O samples exhibit smaller accumulation capacitance than

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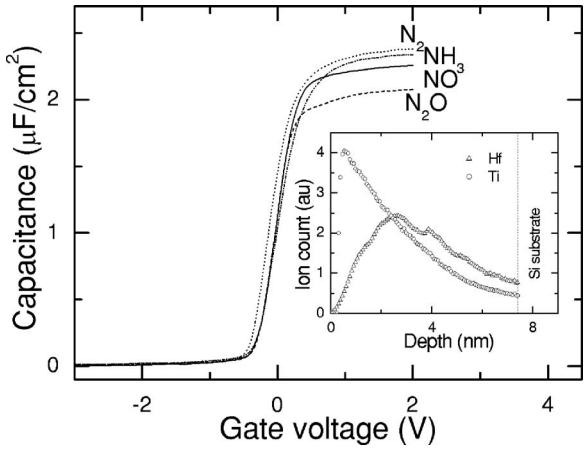

FIG. 1. High-frequency *C-V* curves of MOS capacitors with different Si-surface nitridations. The insert shows the SIMS depth profiles of Ti and Hf in the NO sample.

the control and NH_3 samples, with accumulation capacitance of the NO sample being slightly larger than that of the N_2O sample. This is because the oxidation and nitridation roles of NO are, respectively, weaker and stronger than those of N_2O, resulting in thinner interlayer and more nitrogen incorporation in the NO sample than in the N_2O sample, as can be seen from the Transmission Electron Microscopy (TEM) images in Fig. 2. The higher nitrogen content is favorable for preventing the growth of low-*k* oxide during the subsequent PDA.[7,8] On the other hand, since the NH_3 sample has the strongest nitridation effect and the control sample has no intended growth of interlayer, they have larger accumulation capacitance and thus smaller CET.

TABLE I. Electrical properties of MOS capacitors with different Si-surface pretreatments.

Sample	NO	N_2O	N_2	NH_3
D_{it} (10^{11} cm^{-2} eV^{-1})	1.22	4.1	8.0	6.4
V_{fb} (V)	−0.09	−0.10	−0.19	−0.08
Q_{ox} (10^{11} cm^{-2})	4.7	5.7	18.7	3.4
CET (nm)	1.52	1.66	1.45	1.48

Electrical parameters of the samples are extracted from the HF *C-V* curves and listed in Table I. The equivalent (Q_{ox}) including fixed-oxide charge, border-trap charge, mobile-ion, and interface-state charges, is calculated according to $Q_{ox}=-C_{ox}(V_{fb}-\varphi_{ms})/q$, where φ_{ms} is the work-function difference between aluminum and Si substrate. The NO sample shows the lowest interface-state density. This should be attributed to the fact that with its weaker oxidation role, the NO surface nitridation can more easily form a stoichiometric SiON interlayer by providing suitable proportions of N and O compared to the N_2O surface nitridation. As shown by the secondary-ion mass spectroscopy (SIMS) profile in the insert of Fig. 1, there is a Hf-rich region with less Ti near the interface, thus suppressing the possible effects of Ti on the interlayer due to possible reaction between Ti and Si.[9] As a result, better interfacial properties are obtained. An average Hf/Ti ratio of about 0.4/0.6 is obtained from the inset, which is basically consistent with that obtained from the deposition rates of Hf and Ti, and such high Ti content contributes to the larger equivalent *k* value of the HfTiON/SiON/Si system, e.g., $k=18.9$ for the NO sample. However, the NO and N_2O samples have slightly larger CET ($CET=k_0k_{SiO_2}/C$, where k_0 and k_{SiO_2} are permittivity of vacuum and dielectric constant of SiO_2, respectively; *C* is accumulation capacitance per unit area, as shown in Fig. 1) than the control and NH_3 samples due to the oxidation role of NO and N_2O. It is worth pointing out that the smallest values of Q_{ox} and V_{fb} for the NH_3 sample probably arise from a compensation effect between the negative charges of hydrogen-related electron traps and the positive fixed charges associated with N incorporation.[10]

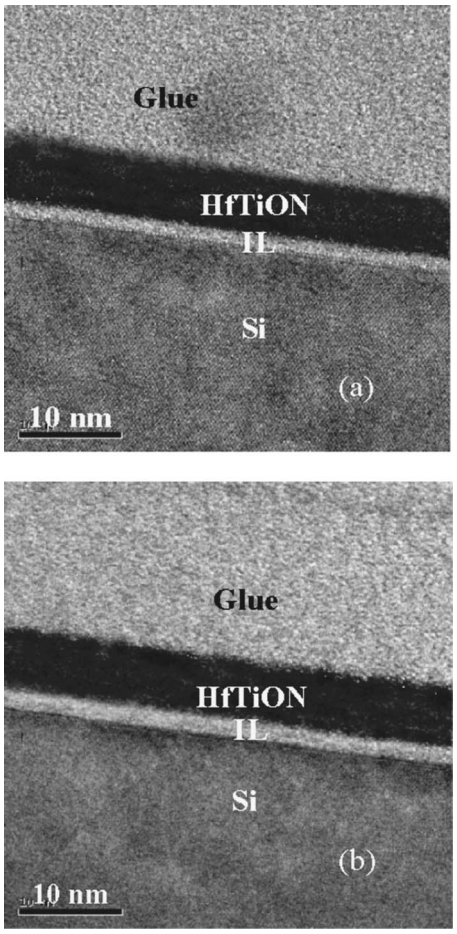

FIG. 2. TEM image of (a) NO sample and (b) N_2O sample, with an interlayer thickness of 13 and 1.5 nm, respectively.

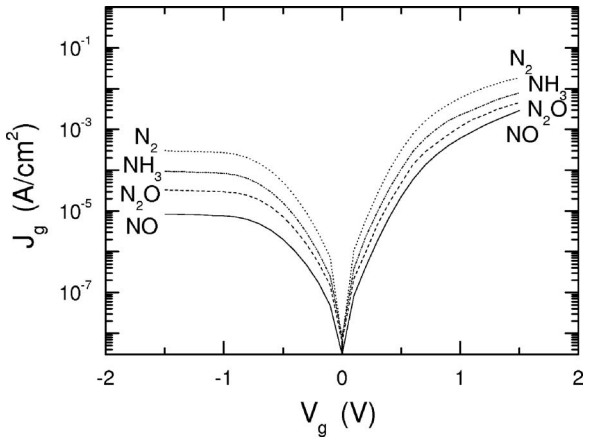

FIG. 3. Gate leakage current density of MOS capacitors with different Si-surface nitridations.

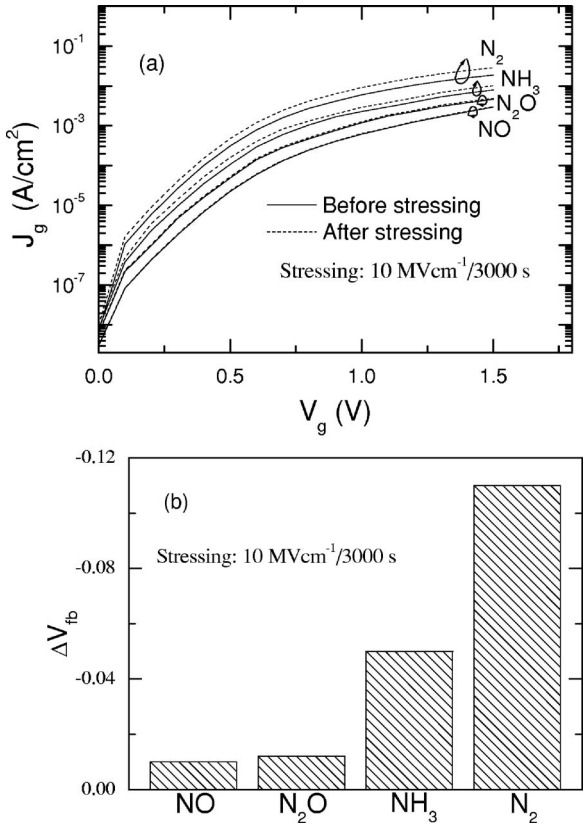

FIG. 4. (a) Increase of gate leakage and (b) shift of flatband voltage of MOS capacitors after a high-field stressing at 10 MV/cm for 3000 s, with the samples biased in accumulation.

The gate leakage currents of different samples are shown in Fig. 3. The NO and control samples have the smallest and largest leakage currents (7×10^{-6} and 2.7×10^{-4} A cm^{-2} for $V_g=-1$ V; 6×10^{-4} and 5.9×10^{-3} A cm^{-2} for $V_g=1$ V) respectively. Obviously, this is associated with the low/high oxide-charge and interface-state densities of the former and latter samples, respectively. The large D_{it} of the control sample is due to the formation of an unpassivated HfTiON/Si interface without a SiON interlayer. For the NH_3 sample, large gate leakage current results from the high interface-state density and a large amount of hydrogen-related electron traps induced by the NH_3 nitridation.[11]

A high-field stress at 10 MV/cm [$=(V_g-V_{fb})$/CET] for 3000 s is used to examine the reliability of the samples. Increase of leakage current and flatband voltage (ΔV_{fb}) are measured after the stress, and are shown in Fig. 4. The NO and control samples have the smallest and largest increase of leakage current and ΔV_{fb}, indicating that the NO sample has the best reliability due to the largest incorporation of nitrogen in the interlayer of NO sample, i.e., near/at the SiON/Si interface.

Si-surface nitridations in N_2O, NO, and NH_3 prior to high-k film deposition are employed to improve the electrical properties of MOS capacitors with HfTiON high-k gate dielectric. The experimental results show that the NO-nitrided sample exhibits excellent interface properties, low gate leakage current, and high device reliability. The involved mechanism lies in the formation of a stoichiometric SiON interlayer. An interface-state density of 1.22×10^{11} cm^{-2} eV^{-1}, a gate leakage current density of 6×10^{-4} A cm^{-2} for $V_g=1$ V, a CET of 1.52 nm, and a k value of 18.9 are obtained for the MOS capacitor with $Hf_{0.4}Ti_{0.6}O_xN_y$/SiON gate dielectric stack prepared by the Si-surface nitridation in NO. Therefore, the surface nitridation in NO is a promising technique for preparing small-sized MOS field-effect transistors with excellent electrical performance and high reliability.

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