Straightforward Transient & Noise Analysis for ΣΔ PLL-based Synthesizers of Multiple Feedback and Feedforward Structures

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Abstract — This paper presents a noise analysis model, which allows basic phase noise calculations of a ΣΔ PLL fractional-N synthesizer. Calculation results on various ΣΔ orders of multiple architectures, feedback and feedforward, and on transient process, which provides quick visualization of the design methods used to minimize the required settling-time, will be presented.

I. INTRODUCTION

In contrast to classical integer-N PLL, it is well known that a factional-N synthesis greatly increases the frequency resolution of the synthesizer without lowering the reference frequency. However, by varying the divider modulus, phase jitter is produced resulting in spurs at the synthesizer output [1]. The method of combining ΣΔ modulation and a fractional-N synthesis has been introduced to conflict this problem. ΣΔ modulation is a noise shaping technique, which modulators generate a control sequence with an average density corresponding to the desired frequency such that the inherent phase jitter is shifted away from baseband to higher frequencies.

PLL-based synthesis is widely used in cellular telephones and communications systems where good phase noise is critical [2]. However, a ΣΔ based synthesizer has the negative effect of introducing quantisation noise. Simulating the effects of this quantisation noise as well as the synthesizer's dynamic response to variations of the ΣΔ input can help evaluate stability and characterize the system's performance. Besides phase noise and spurious signals performances, an important aspect of PLL design is the required settling-time. Requirements are that the synthesizer has to switch between bands and settle to another frequency within a preset time. The settling-time is fundamentally determined by the loop bandwidth. Many loop bandwidth enhancement schemes have been reported in literature [3,4] in attempting to generate low noise and low spur signals while achieve fast settling-time. These adaptive PLLs are typically based on increasing the charge pump current and/or reducing the time constants of the loop filter.

Agilent EEs of Advanced Design System may consider the most popular software for simulating a fractional-N PLL [5]. An instantaneous realization of its performance aspects will be very useful before any time-consuming simulation. This paper examines the required settling-time of PLL design and its phase noise performance. Using the Laplace transform technique, the transient process can easily be evaluated. The effects on settling-time by using different settings for the loop's capacitors and for the roots ratio of the characteristic polynomial have been quantified. The computed results provide quick visualization of the design methods used to minimize the required settling-time will be presented. A simple model for ΣΔ PLL fractional-N synthesizer that allows basic analysis of its dynamic and noise performance also has been developed. Calculation results on various orders for ΣΔ modulators of two commonly used structures, multiple feedback and multiple feedforward, illustrate the impact of ΣΔ quantisation noise.

II. BACKGROUND

A closed-loop ΣΔ fractional-N synthesizer typically comprises a phase-frequency detector (PFD), a loop filter and a voltage-controlled oscillator (VCO) in the forward path, a frequency modulus divider in the feedback path and a ΣΔ modulator. A PFD is a nonlinear device whose output contains the phase difference between the two oscillating input signals, the reference signal and the divided signal. The output of a PFD, the phase error, is used as the control voltage for the VCO. The phase error is then low pass filtering through a loop filter. VCO is another nonlinear device, which output frequency is further divided down to a lower frequency signal by a divider. The synthesizer ensures high frequency resolution by dithering, dithered between integer values to achieve fractional divide ratios. This dithering action is accomplished through a ΣΔ modulator. The synthesizer ultimately achieves accurate setting of its output frequency by locking to the reference frequency.

III. MODELING OF ΣΔ PLL-BASED SYNTHESIZERS

A. Fractional-N PLL

A phase detector executes the PLL locking action by comparing the phase of the divided version of the VCO output, $\Phi_{div}[k]$, and the phase of the reference source, $\Phi_{ref}[k]$, to generate an error signal, $e(t) = K_P\{\Phi_{ref}[k] - \Phi_{div}[k]\}$. The phase detector has a gain of K_P (V/rad).

A typical 3rd order filter as a function of zero frequency, ω_z, and pole frequency, ω_p, has a transfer function of $K_F = \{R_2C_2 / R_1(C_2+C_3)\}\cdot\{\omega_p(s+\omega_z) / s(s+\omega_p)\}$. The loop filter conditions the system's response to the error signal and drives the VCO to produce an output signal equal to $2\pi f_c + 2\pi K_V\int V_{in}(t)dt$. Parameters f_c, K_V and $V_{in}(t)$ represent the free-running frequency, the gain (Hz/V) and the control voltage, respectively. In the phase domain, the Laplace transform of the VCO output is $\Phi_{out}(s) = K_O V_{in}(s)$, or equivalently $K_V V_{in}(s)/s$.

The divider is modeled by relating its output in phase to the VCO output by $K_N\{\Phi_{out}[k] - \Phi_m[k]\}$, whereas $K_N = 1/N$ is the divider gain and $\Phi_m[k]$ is the output of the divider accumulation action. By taking the z-transform of $\Phi_m[k]$, the accumulator of the divider has a transfer function of $K_A = 2\pi z^{-1}/(1-z^{-1})$.

B. ΣΔ Modulator

ΣΔ modulators are the most suitable ADC for low frequency, high-resolution applications [6]. Many topologies have been developed but most are a variation of single-stage structure and cascaded structure, as described by $y(z) = x(z)STF(z) + r(z)NTF(z)$. The modulator passes its input, $x(z)$, to the output, $y(z)$, along with quantisation noise, $r(z)$, that is shaped by the noise transfer function, $NTF(z)$. The quanitzation noise is assumed white and uniformly distributed between 0 and 1 so that its spectrum is flat and of magnitude $S_{\Phi_r}(f) = 1/12$.

A single-stage ΣΔ architecture can further divided into multiple feedback and multiple feedforward. The former structure has a $STF(z)$ of z^{-n} and a $NTF(z)$ of $(1-z^{-1})^n$, whilst the latter with $STF(z)=[(1-z^{-1})^{n-1}+(1-z^{-1})^{n-2}...+(1-z^{-1})^{n-1})]$

$^1)^1+1]/[(1-z^{-1})^n+(1-z^{-1})^{n-1}...+(1-z^{-1})^1+1]$ and $NTF(z)=[(1-z^{-1})^n]/[(1-z^{-1})^n+(1-z^{-1})^{n-1}...+(1-z^{-1})^1+1]$.

For cascaded ΣΔ modulators, for examples 3rd order MASH (multistage noise shaping) architectures like MASH 1-1-1 and MASH 1-2, have the same $NTF(z) = (1-z^{-1})^3$ as the single-stage structure with feedback loops, but with a different $STF(z)$ of 1. By combining the results of section III a generic model of ΣΔ PLL fractional-N synthesizer is obtained (See Fig.1).
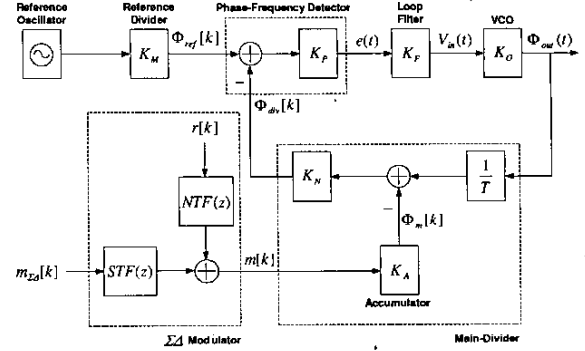

Fig. 1. A model for ΣΔ PLL fractional-N synthesizers

IV. PARAMETERIZATION OF ΣΔ PLL-BASED SYNTHESIZER

A. Dynamic and Noise Analysis Model

The PLL loop operates on various noise sources, as tabulated in Table I. The magnitude of the loop transfer function squared, $|H(f)|^2$, multiplied by the phase noise of the source, $S_{\Phi\_in}(f)$, provides the output phase noise power of that source, $S_{\Phi\_out}(f)$, at the output of the loop. Calculation of the output phase noise power for some noise sources however is complicated by the fact that both discrete-time and continuous-time signals are presented.

Since the noise sources appear in different circuit nodes throughout the loop, the frequency response of loop transfer function between each source and the output will be different. It can also be seen from Table I that a base function that provides a simple description of all the loop

TABLE I
LOOP TRANSFER FUNCTION OF THE ΣΔ PLL FOR VARIOUS NOISE SOURCES

Noise Source, $S_{in}(f)$	Forward Gain, $F_{Fw}(f)$	Feedback Gain, $F_{Fb}(f)$	Loop Transfer Function, $H(f)$	Equivalent Loop Transfer Function, $H(f)$
Ref.-Oscillator, S_{ro}	$K_PK_FK_O$	K_N	$K_PK_FK_O/(1+K_PK_FK_OK_N)$	$(1/K_N)\cdot GH(s)/[1+GH(s)]$
Ref.-Divider, S_{rd}	$K_PK_FK_O$	K_N	$K_PK_FK_O/(1+K_PK_FK_OK_N)$	$(1/K_N)\cdot GH(s)/[1+GH(s)]$
PFD, S_{pd}	K_FK_O	K_PK_N	$K_FK_O/(1+K_PK_FK_OK_N)$	$(1/K_PK_N)\cdot GH(s)/[1+GH(s)]$
Loop-Filter, S_F	K_FK_O	K_PK_N	$K_FK_O/(1+K_PK_FK_OK_N)$	$(1/K_PK_N)\cdot GH(s)/[1+GH(s)]$
Main-Divider, S_{md}	$K_PK_FK_O$	K_N	$K_PK_FK_O/(1+K_PK_FK_OK_N)$	$(1/K_N)\cdot GH(s)/[1+GH(s)]$
VCO, S_{VCO}	1	$K_PK_FK_OK_N$	$1/(1+K_PK_FK_OK_N)$	$(1/GH(s))\cdot GH(s)/[1+GH(s)]$
ΣΔ Quantisation, S_r	$K_PK_FK_OK_N$	1	$K_PK_FK_OK_N/(1+K_PK_FK_OK_N)$	$GH(s)/[1+GH(s)]$

transfer functions of interest is described by $A(s) = GH(s)$ / [1+$GH(s)$],

$$A(s) = K_P K_F K_V / (sN + K_P K_F K_V) \quad (1)$$

By superposition the results tabulated in Table I, it is possible to power sum the effects of all the individual noise sources. Fig.2 shows the parameterized model of a $\Sigma\Delta$ PLL for dynamic response and noise calculations. VCO noise is high-passed filtered by the PLL dynamics, 1 - $A(f)$, whilst the other noises are low-passed filtered by the PLL dynamics, $A(f)$.
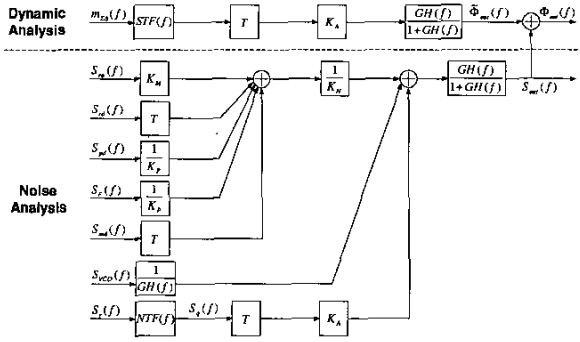

Fig. 2. Parameterized model of a $\Sigma\Delta$ fractional-N synthesizer for noise calculations

B. Transient Process Analysis

By letting $U = \omega_P/\omega_Z$ and $V = \omega_c/\omega_Z$ the open-loop gain, with an open-loop cut-off frequency of ω_c, can be defined as $GH(s) = (\omega_c^2/s^2)(sU + \omega_c U/V) / (sV + \omega_c U)$. Then, the characteristic equation, CE = 1+$GH(s)$, can be derived that $s^3 + s^2(\omega_c U/V) + s(\omega_c^2 U/V) + (\omega_c^3 U/V^2) = 0$. By solving the parameter U further with the pole and zero frequencies yields $U = C_2/C_3+1$. The roots of the characteristic equation become the closed-loop poles of the overall transfer function. On the s-plane, these roots are typically $s_1 = a$ and $s_2 = b + j\gamma$ and $s_3 = b - j\gamma$ with a polynomial $(s - a)((s - b)^2 + \gamma^2)$. Equalizing coefficients in this polynomial and the CE, and following by solving the obtained equations simultaneously yields

$$V = 2\alpha(C_2/C_3 +1)^2 / [(1+2\alpha)^2(C_2/C_3 - 2\alpha)] \quad (2)$$

where α is the ratio between b and a, for 0< α ≤1.

The transient process is obtained by computing the inverse Laplace transform of $\Delta f_i(s)/[1+GH(s)]$. The parameter $\Delta f_i(s)$ represents the frequency step function at the PFD input in the complex domain. The settling-time, t_s, in turn depends on the normalized settling-error, $\beta = e/\Delta f_i$, whereas e is the error signal (residual error).

V. RESULTS

A. Phase Noise

Four noise sources are used in here to demonstrate the effectiveness of the parameterized noise model shown in Fig.2, which include reference-oscillator, main-divider, VCO and $\Sigma\Delta$ modulator. The $\Sigma\Delta$ PLL-based synthesizer consists of a PFD with K_P of 0.5V/rad, an active integrator, a VCO with K_V of 10MHz/V, and a feedback division ratio of 10^3. The overall phase noise output is computed through the use of the phase noise coefficients k_i that were reported in reference [2], for a commercial 10MHz crystal oscillator, a main-divider, and a VCO. It was reported that these coefficients, as tabulated in Table II, were experimentally determined using asymptotic lines with various slopes to approximate the noise plot from a given manufacturer's data sheet. For the quantisation phase noise, a 2nd order $\Sigma\Delta$ modulator of multiple feedback structure rejects the noise by -40dB/decade.

The total phase noise along with the four contributors that make up the overall noise is shown in Fig.3. The overall noise power in the PLL output is a function of its bandwidth. The influence of oscillator noise and main-divider noise dominate at low frequencies, whilst VCO and $\Sigma\Delta$ quantisation noise dominate at high frequencies. Fig.4 demonstrates the impact of $\Sigma\Delta$ quantisation noise on a conventional PLL's noise performance. It is clearly seen that a $\Sigma\Delta$ PLL-based synthesizer has a dramatic effect on the overall phase noise at high frequencies. High-pass filtering of this quantisation noise can be achieved through higher order $\Sigma\Delta$ modulators, which consequently improve the signal to quantisation noise in the baseband. In comparison between a single-stage $\Sigma\Delta$ modulator of multiple feedforward and of multiple feedforward, the former structure attempts to further improve the process of noise shaping than the latter.

TABLE II
PHASE NOISE COEFFICIENTS FOR THE THREE DIFFERENT NOISE SOURCES

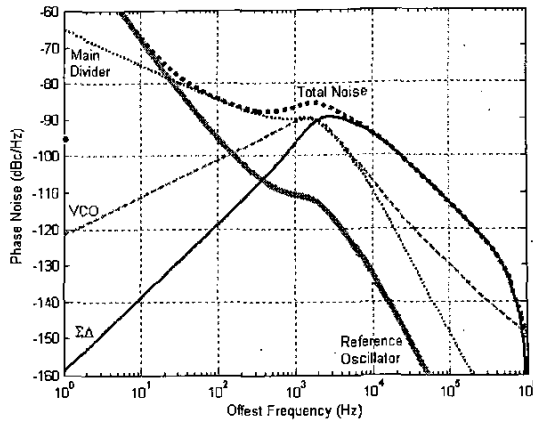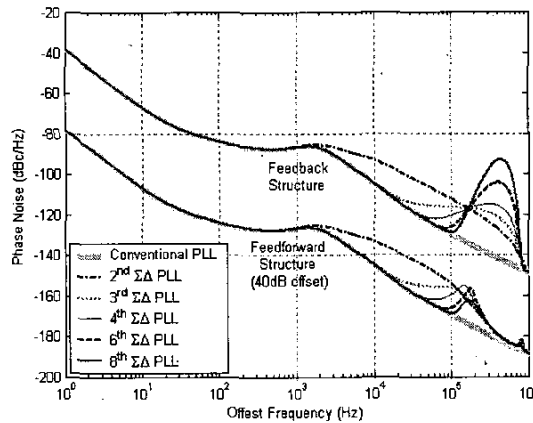|	k_0 (white phase)	k_1 (f^{-1} flicker phase)	k_2 (f^{-2} white FM)	k_3 (f^{-3} flicker FM)
Reference-oscillator	-158dB$_c$/Hz	-127dB$_c$/Hz	-98.5dB$_c$/Hz	-78.2dB$_c$/Hz
Main-divider	-155dB$_c$/Hz	-125dB$_c$/Hz	-	-
VCO	-155dB$_c$/Hz	-	-30dB$_c$/Hz	7dB$_c$/Hz

Fig. 3.   Overall phase noise and its contributors

Fig. 4.   Overall phase noise for a conventional PLL, $\Sigma\Delta$ PLL-based of feedback and feedforward structures with various orders

Fig. 5.   Normalized settling-time against C_2/C_3 for various α

B. Settling-Time & Bandwidth

Fig.5 shows the simulation results for various b-to-a ratios (α), for $\beta = 10^{-5}$. They are described by the change in normalized settling-time, $t_s \cdot \omega_c$, as a function of C_2/C_3. The cut-off frequency determines approximately the closed-loop bandwidth. From Fig.5 it is observed that the case with $\alpha = 1.0$ ($b = a$) ensures the shortest settling-time, for the range $4.7 < C_2/C_3 < 7.7$. Moreover, the minimal normalized transient-time become more distinguishable as α increases in value. As it is expected that the higher the relative settling-error β the faster the settling-time is required. Fig.5 provides a quick visualization of the design methods used to minimize the required settling-time. For example, a loop filter with C_2/C_3 of value 6.65 and a cut-off frequency of 1Mrad/s, a near minimal settling-time of $< 12\mu s$ is required, for $\alpha = 1.0$ and $\beta = 10^{-5}$. It is noted that Eq(2) indicates an approximation for the settling-time, although it does not ensure the exact global minimum.
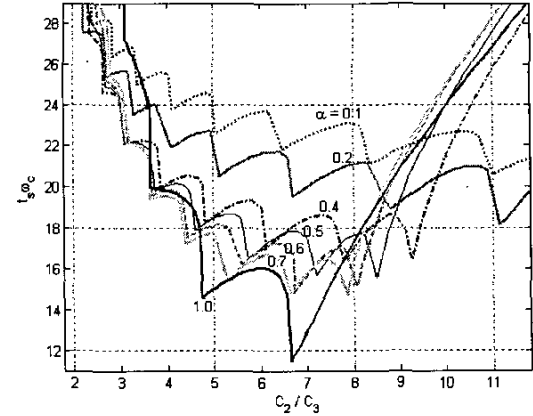
VI. CONCLUSION

In this paper, a general model for $\Sigma\Delta$ PLL-based synthesizers has been developed. The model was obtained by simply incorporating a $\Sigma\Delta$ modulator model into a PLL. The PLL model was shown best to describe by a base transfer function $A(f)$, and was then parameterized by $A(f)$, which further simplifies phase noise calculations. This was used to illustrate the effect of $\Sigma\Delta$ quantisation noise. The multiple feedforward structure was shown to provide better noise shaping at high frequencies than the multiple feedback structure of the same $\Sigma\Delta$ modulator's order. A quantitative feels for a near minimal settling-time of PLL design also has been presented, which further comforts the problem of loop bandwidth enhancement.

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