Practical Solutions to the Design of Current-driven Synchronous Rectifier with Energy Recovery from Current Sensing

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Abstract: Current-driven synchronous rectifier with current sensing energy recovery has been proved to be suitable for almost all high frequency switching topologies. The synchronous rectifier can be driven on and off automatically according to the current direction. In fact it can be taken as an active diode with very low power dissipation. Some theoretical analysis and experimental results have been shown in the previous work. This paper presents an extended analysis to some practical considerations when applying this current-driven synchronous rectifier in switching converter design.

I. INTRODUCTION

Low supply voltage can effectively reduce the total power consumption of modern VLSI digital circuits. Some state-of-the-art high speed digital circuits and microprocessors have already made use of supply voltage lower than 1V to save power consumption [1]. To deliver supply voltage as low as this level with high efficiency, synchronous rectification with a low conduction drop MOSFET is the only possible solution. A lot of work has been done by many researchers in this area. A major issue to be considered in the SR circuit is the gate drive design.

Generally speaking, there are two basic approaches to drive a synchronous rectifier (SR) in a switching converter.

The first approach drives the SR with a voltage signal within the switching topology which is synchronized with the desired drive timing. The SR driven by this method can be taken as a bi-directional controlled switch. This kind of synchronous rectifier may allow both forward and reverse current flowing through it. Switching converters implemented with these kinds of synchronous rectification usually has no DCM (discontinuous conduction mode) under the whole load and line range. There are also other disadvantages in practical applications such as the risk of reverse power sinking in parallel application and the difficulty of optimizing drive voltage for variable voltage range. [1]. The SR drive schemes are usually different in different switching topologies.

The second approach is actually to design a unidirectional low loss diode using MOSFET. A sensor senses the current or the voltage of the SR and then turns on and turns off the SR accordingly. The SR driven with this mechanism does not allow a reverse current flowing through it. This makes a SR converter has very similar operation characteristic to a diode converter except that the rectification loss is much lower. The effectiveness of this kind of SR drive schemes depends heavily on the response speed of the adopted sensing circuit. Usually a low loss wide bandwidth sensing and driving circuit is required for high frequency operation.

Current-driven SR with current sensing energy recovery as shown in Fig. 1 was proposed and analyzed in prior work [2-7]. This current-driven SR can be taken as an active diode which can directly replace the conventional diode rectifier in most switching topologies. This can greatly ease the SR design. The SR drive signal is derived automatically through an efficient current sensing and drive circuit. By recovering the current sensing energy, the current-driven SR can operate at high frequency with high efficiency.

This paper presents some practical issues in the application of the current-driven SR in switching converters. These issues include the SR turn off delay, the possible gate ringing during turn off period and the short circuit related problems. These issues are investigated and the solutions to tackle these problems are given. Analytical results and experiments demonstrate the effectiveness of these solutions.

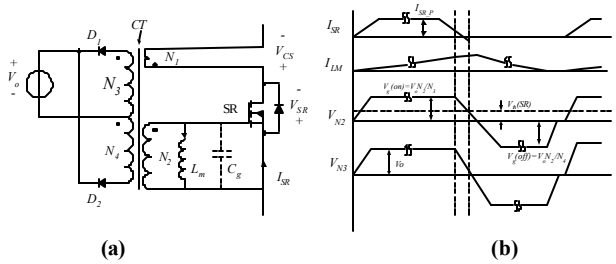


Fig. 1. Current-driven SR: (a) circuit model (b) critical waveforms

II. DESCRIPTION OF CURRENT-DRIVEN SR CIRCUIT

The circuit diagram of current-driven SR is shown in Fig.1. This current driven SR is composed of a MOSFET, a current transformer with four coupled windings and a DC source. Winding N_1 is the current sensing winding which is connected in series with the SR MOSFET. Any current flowing SR also goes through N_1. Winding N_2 is the drive winding which is connected to the gate and source of the MOSFET. Winding N_3 is the current sensing energy recovery winding which is connected to a DC source through a diode D_1. N_4 winding is the magnetic reset winding for the current transformer which can reset the magnetic flux period by period. Such circuit arrangement allows the current direction of SR to be detected and a proper gate drive signal to be generated at the SR gate terminal. In Fig. 1, the magnetizing inductance L_m and the SR gate capacitance C_g are also shown. The circuit operation can be briefed as follow.

When a forward current flows through the source to the drain of the SR and N_1 winding of the current transformer, there is a reflected current flowing out from N_2 winding and charges up SR gate capacitance. Consider the magnetizing inductance of the current transformer, the charge up process is a second order resonance [1]. Before the time when this SR gate voltage reaches its threshold, the forward current is carried by SR body diode. After the gate voltage reaches and goes beyond its threshold, the SR channel is turned on and all current is diverted to the low impedance SR channel.

The SR gate voltage continues to go up until the reflected N_3 winding voltage reaches the DC source voltage V_o. Then diode D_1 conducts and all the windings are clamped by V_o. This ensures a constant SR turn on gate voltage which is independent of the line voltage. As long as the SR current continues to flow, the gate voltage remains at this clamped value and keeps the on status of SR. The gate drive voltage can be easily programmed by adjusting the N_2 and N_3 winding turns ratio so that an optimal gate voltage can be chosen.

There is an important current sensing energy recovery concept in this drive mechanism. The current sensing energy taken by N_1 winding can be delivered through N_3 winding and diode D_1 to the DC source V_o so that current sensing circuit has very low power dissipation. This feature ensures the high efficiency of this current-driven SR.

When the forward SR current drops, the reflected current in N_3 winding also drops until it drops to zero. Diode D_1 then blocks the N_3 winding from the DC source. With the forward SR current continues to drop after that, another second order resonance is induced. This discharges the SR gate capacitance accordingly. When the SR gate voltage drops below its threshold, the SR blocks and no further reverse current can flow through it.

The SR gate voltage continues to drop negatively because of the discharging process caused by the gate capacitance and the magnetizing current. The negative gate voltage can be clamped when diode D_2 conducts and all windings are again clamped by the DC source. All the magnetizing energy is then sent back to the DC source V_o. After the magnetic reset process is over, the gate voltage returns back to zero and keeps the off status of SR until the next switching cycle.

From the above descriptions, we can know that the high performance operation of this current-driven SR is determined by several factors. Firstly, the turn off process should be as prompt as possible to ensure no significant amount of reverse current occurs. Secondly, during the off state of the SR, there should be no positive drive voltage whatsoever. Lastly, the DC source is important to ensure the gate turn on voltage. It must be capable of sinking power.

III. PRACTICAL ISSUES AND PROPOSED SOLUTIONS IN IMPLEMENTING A CURRENT-DRIVEN SR

A. Turn off delay

The turn off process was described thoroughly in [3]. Circuit models and waveforms are also shown in Fig. 2. The turn off delay time T_{off_d} is defined as the time duration from SR current commutates to zero until the SR gate voltage drops below its threshold voltage. It was found out as (1).

$$T_{off\_d} = \sqrt{2 \times \frac{V_g(on) \quad V_{th}}{m_2} \times \frac{N_2}{N_1} C_g} \quad \frac{N_2}{N_1} \times \frac{V_g(on)}{m_2 L_m} \times DT_S \quad (1)$$

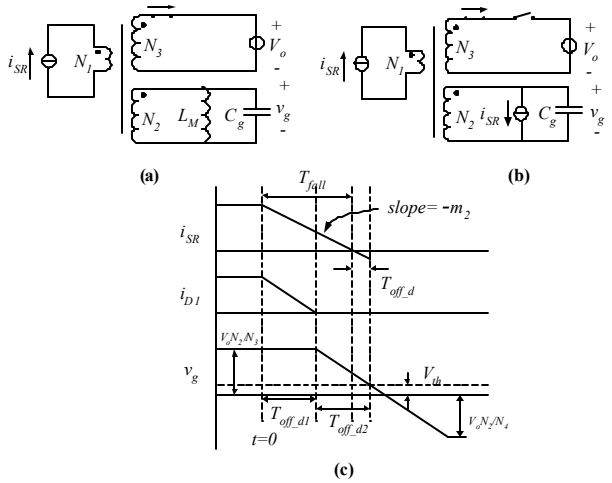


Fig. 2. Circuit modes and waveforms at turn off transient (a) turn off mode I (b) turn off mode II (c) critical waveforms

where $V_g(on)$ is the clamped voltage which is equal to $V_o \times N_2 / N_3$, V_{th} is the SR threshold voltage, m_2 is the falling slope of SR current, DT_s is the turn on time of the SR and N_1~N_4 are the numbers of turns of the respective windings.

It is obvious that the turn off delay time should be as close as possible to zero. If T_{off_d} is greater than zero, there is a reverse current flowing through the SR. The amplitude of this reverse current is determined by the current falling slope m_2 as well as T_{off_d}. For a converter operating in CCM this amplitude is usually very high because the parameter m_2 is determined mainly by the applied transformer winding voltage and the small parasitic loop inductance. This indicates even very small turn off delay time may induce a high reverse current which deteriorates the performance of synchronous rectification. If T_{off_d} is smaller than zero, it means the SR turns off before it drops to zero. Whenever this happens, the remaining SR current is carried by the SR body diode. As this remaining current is usually much lower than the normal load current, the so caused body diode reverse recovery problem usually does not exhibit a serious problem. In fact, many conventional SR drive solutions also face the similar problems and accurate drive timing is almost impossible considering the many load and line variations.

In our design, we try to minimize the turn off delay time so that it can be near or smaller than zero. If the turn off timing is actually before the zero current crossing point, a simple delay circuit can be added for maximal efficiency operation. Based on (1), at least the following procedures can be done to minimize the turn off delay.

Solution 1 *- by adjusting the L_m:*

Based on (1), a lower magnetizing inductance L_m can help reduce the turn off delay. This L_m can be designed either by controlling the number of turns of current transformer windings or by choosing a magnetic core with suitable permeability and size. It should be noted that to ensure the operation of this current-driven mechanism, the magnetizing inductance should also not be too small. Otherwise the magnetizing current may take the whole reflected SR current and improper turns off signal may be issued by the drive circuit [3]. Hence we can design a current transformer that can satisfy constrain (2) to ensure no turn off delay.

$$\frac{V_o \times DT_s \times N_2^2}{I_{SR\_P} \times N_1 \times N_3} \quad L_m \quad \frac{V_g(on) \times DT_S}{\sqrt{2m_2 \times [V_g(on) \quad V_{th}] \times \frac{N_1}{N_2} \times C_g}} \quad (2)$$

where I_{SR_P} is the forward peak SR current.

Solution 2 *- by adding a buffer to the gate drive:*

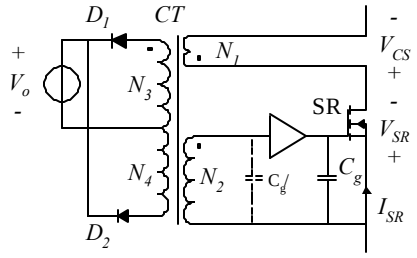


Fig. 3. Speed up turn off process with a buffer

From (1), it can also be seen that SR gate capacitance is another parameter that can affect turn off delay time. Smaller gate capacitance can always speed up the turn off process. As is shown in Fig. 3, if a buffer with current gain b is added between the N_2 winding and the SR gate terminal, the equivalent gate capacitance needed to be driven by the current transformer is then reduced by b times smaller. This reduces the first term in (1) by $\sqrt{b}$ times. A practical buffer has certain delay between the input and output signal. This delay time can be in the range of 5ns to 30ns depending on the buffer design. Taking the buffer delay time T_{buffer_d} into consideration, the current gain requirement of this buffer can be described by (3).

$$b \quad \frac{2 \times (\frac{V_g(on) \quad V_{th}}{m_2}) \frac{N_2}{N_1} C_g}{(\frac{N_2}{N_1} \times \frac{V_g(on)}{m_2 \times L_m} \times DT_s \quad T_{buffer\_d})^2} \quad (3)$$

Solution 3 *- by adding a small inductor in series with D_1:*

By introducing a small accelerating inductor L_a between the DC source and the diode D_1, the turn off time can be greatly reduced. The circuit diagram is shown in Fig. 4. Equivalent circuit and critical waveforms are given in Fig. 5. The drive signal at winding N_2 starts to fall at the beginning of the SR current commutation period. Hence turn off signal can be issued much earlier than the basic current-driven solution as shown in Fig. 2.

Before the SR current commutation process, there is a

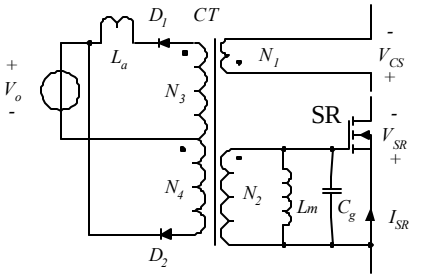


Fig. 4. Speed up turn off process with a inductor

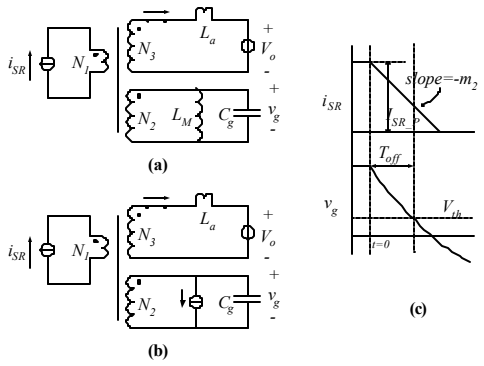


Fig. 5. (a), (b) Turn off equivalent circuitwith accelerating inductance. (c) critical waveforms

steady current flowing through the Diode D1 and N3 winding. At time t=0, the SR current begins to commutate. The equivalent circuit is as shown in Fig. 5(a). It is a third order resonant circuit with two inductors and one capacitor. The accelerating inductor L_a is very small compared with the current transformer magnetizing inductor. The magnetizing current can be assumed to be constant during the short switching transition period. Then the circuit model can be simplified as Fig. 5(b). It is a second order circuit with initial conditions (4) and (5). The SR current can be expressed as (6). Solving this second order circuit with (4), (5) and (6), The resonant SR gate voltage can be found as (7).

$$v_g(0) = V_o \times N_2 / N_3 \tag{4}$$

$$i_{La}(0) = I_{SR\_P} \times N_1 / N_3 \tag{5}$$

$$i_{SR} = I_{SR\_P} \quad m_2 \times t \tag{6}$$

$$v_g(t) = \frac{N_1 \times N_2}{N_3^2} \times m_2 \times L_a \times \cos\left(\frac{N_3}{N_2} \times \frac{1}{\sqrt{L_a \times C_g}} \times t\right) + \frac{N_2}{N_3} \times V_o \quad \frac{N_1 \times N_2}{N_3^2} \times m_2 \times L_a \tag{7}$$

$$T_{off} = \frac{N_2}{N_3} \times \sqrt{L_a \times C_g} \cos^{-1}\left(1 + \frac{V_{th} \quad \frac{N_2}{N_3} \times V_o}{\frac{N_1}{N_3} \times \frac{N_2}{N_3} \times m_2 \times L_a}\right) \tag{8}$$

The accelerating inductor L_a during the turn off process works like a di/dt detector. When the di/dt of SR is high, the gate will see a turn off signal due to the L_a and C_g resonance. To ensure the turn off process, the minimal value of the resonant gate voltage v_g must be smaller than its threshold voltage, otherwise the accelerating inductance does not help turn off the SR at all. Based on this consideration, we can estimate the range of desired L_a by (9). This gives the accelerating inductor a lower limit which may make early turn off process possible.

$$L_a \quad \frac{\frac{N_2}{N_3} \times V_o \quad V_{th}}{2 \times \frac{N_1 \times N_2}{N_3^2} \times m_2} \tag{9}$$

It can also be noted that this inductance value could not be too high. On the one hand, a large inductor increases the gate voltage at turn on transient. On the other hand, because this inductance value determines the frequency of the second order resonance, too high inductance value may cause a long resonant duration that slows down the turn off process. If the SR turn off time is longer than the current commutation time, reverse current occurs again.

The upper limit of L_a does not have an explicit mathematical solution. Numerical calculation and iterations with the help of computing software have to be used to find out this value. The following conditions need to be considered together.

$$V_g < V_{th} \tag{10}$$

$$i_{N3} > 0 \tag{11}$$

$$T_{off} < T_{fall} \tag{12}$$

where i_{N3} is the current flowing through N_3 winding, T_{off} is the time duration from the time SR current starts to commutate to the time SR gate voltage drops to threshold. T_{fall} is the SR current commutation time. (10) ensures the turn off process. (11) expresses the constrain caused by diode D_1. (12) determines the maximal resonant period to turn off SR so that no reverse current occurs.

Practical implementation of this accelerating inductor is very simple. The typical value of this accelerating inductor is less than 1μH. A one-turn tiny magnetic bead can usually be sufficient to fulfill the turn off acceleration task.

All the above three solutions can effectively minimize the SR turn off delay time. In the practical SR design, these solutions can be combined together to ensure the high performance of current-driven synchronous rectification. A well-designed current-driven synchronous rectifier may have reverse current smaller or comparable to SR body diode reverse recovery current [1, 8].

It should be noted that the turn off delay is an important issue only for converters operating in CCM. For a DCM operation converter, because the di/dt is much lower than CCM, the basic energy recovery current driven method can operate very well without the need of the turn off delay concerns.

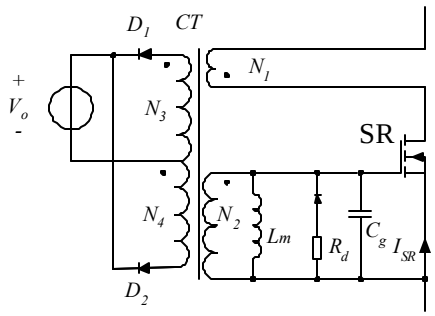


Fig. 6. Damping of gate voltage resonance with a resistor

B. Gate voltage resonant during turn off time.

A false drive signal may occur during the off period when current transformer magnetic reset process is over. This is caused by the resonance of the magnetizing inductance and parasitic capacitance. This resonance may induce a positive gate voltage across the drive winding and falsely trigger the SR.

Solution *- by adding a damping resistor across the drive winding:*

This issue can be solved by adding a damping resistor R_d in parallel with N_2 winding as shown in Fig. 6. A critical or over damping is needed to prevent gate voltage from going positive during off status. A diode can be added in series with the damping resistor so that this damping circuit does not dissipate energy during SR turn on period. (13) shows the required R_d for critically damped response. This equation is for reference only as the parasitic capacitance may not be measured easily. The actual value of R_d can be tested in the circuit design. The practical range is around 100 to 5K .

$$R_d = 2\sqrt{\frac{L_m}{C_p}} \qquad (13)$$

where C_p is the equivalent parasitic capacitance across the drive winding N_2.

C. Gate drive signal during short circuit operations

There is a DC source in this current-driven SR. Typically this DC source makes use of the output voltage of the converter. However, if the converter output is shorted, there will be no gate drive voltage either. All load current flowing through the body diode may overheat the SR during the short circuit condition if there is no special method to prevent this.

Solution 1 *- using an alternative DC source other than output voltage*

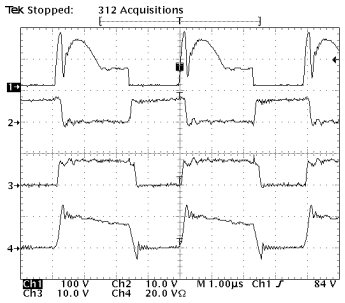
Theoretically any DC source can be used to clamp the gate voltage and recover the current sensing energy. While the load short-circuit is very typical in power supply application, an intuitive way to prevent this is to use another DC source. It can be the input voltage or any other DC voltage in the converter that can it capable of sinking power.

Solution 2 *- using hiccup mode short circuit protection:*

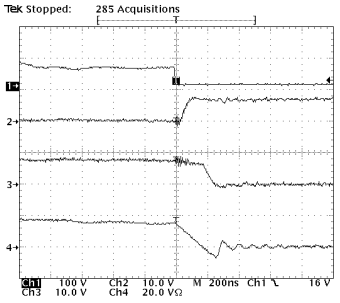
The hiccup mode short circuit protection is very typical for short circuit protection. This can reduce the average power handled by the current-driven SR and hence reduce the power loss and relieve thermal problem of the current-driven SR during output short circuit condition.

IV. EXPERIMENTAL VERIFICATIONS

A single-end forward DC to DC converter with switching frequency of 250kHz and output of 2.2V and 20A is built to demonstrate some of the proposed solutions. Fig. 7 (a) shows the captured waveforms of such a current-driven converter with a buffer but without an acceleration inductor. A sudden voltage drop can be seen in the primary drain. This is due to the forward SR reverse current. Fig. 7(b) shows the exemplified waveforms during the freewheel SR turn off transient. The SR turn off delay and so caused reverse current can be clearly seen. This reverse current can lower the converter efficiency by 1~2%.



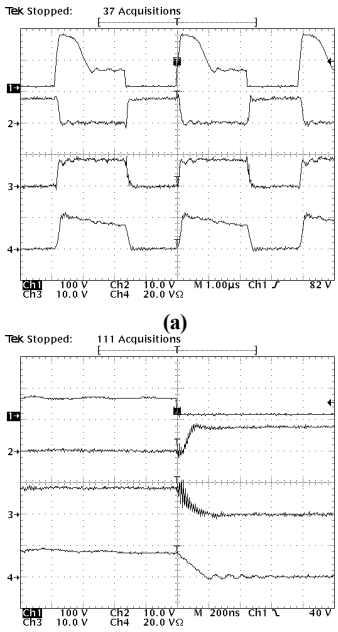
(a)



(b)

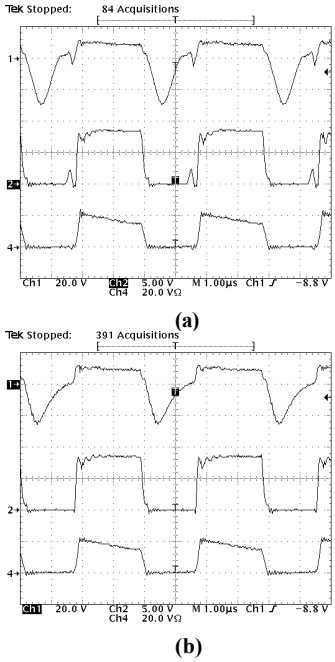
Ch1: Drain voltage of primary switch (100V/div)
Ch2: Gate drive of forward SR (10V/div)
Ch3: Gate drive of freewheel SR (10V/div)
Ch4: Current of freewheel SR (20A/div)

Fig. 7. 2.2V/20 forward current-driven SR converter without accelerating inductor



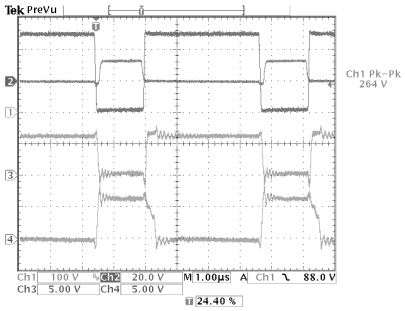
Ch1: Drain voltage of primary switch (100V/div)
Ch2: Gate drive of forward SR (10V/div)
Ch3: Gate drive of freewheel SR (10V/div)
Ch4: Current of freewheel SR (20A/div)

Fig. 8. 2.2V/20 forward current-driven SR converter with accelerating inductor



Ch1: Drive winding voltage
Ch2: Gate drive of freewheel SR
Ch4: Current of freewheel SR (20A/div)

Fig. 9. False SR gate voltage ringing and its damping



Ch1: Drain voltage of primary low switch (100V/div)
Ch2: Gate voltage of primary low switch (20V/div)
Ch3: Gate voltage of freewheel SR (5 V/div)
Ch4: Gate voltage of forward SR (5/div)

Fig. 10. 1.5V/40A AC/DC converter capable of parallel application

Fig. 8 (a) shows the improvement of turn off delay time by adding a buffer as well as an accelerating inductor. Fig. 8(b) shows the exemplified waveform during the freewheel SR turn off transient. It can be clearly seen that the turn off process happens at the time of current commutation. The reverse current in the two SRs is almost eliminated with the turn off acceleration mechanism. The accelerating inductor is realized by a ferrite bead with an inductance value of 0.8 H.

Fig. 9 shows the effect of gate ringing and the damping solution to prevent it. Fig. 9(a) shows the drive winding waveforms as well as the gate waveform. There is a positive gate voltage in the drive winding. This may falsely turn on the SR due to this positive resonant voltage. A damping resistor of 2k is connected in parallel with the gate drive winding to damp this resonance. Experimental waveforms shown in fig. 9(b) demonstrate that the false turn on voltage can be eliminated by such a critical damping process.

Apart from this, an AC/DC converter with 1.5V/40A output is built with this current-driven SR solution. Asymmetric half-bridge topology is used to achieve ZVS for high efficiency AC/DC operation. Critical waveforms are shown in Fig. 10. Due to the unidirectional characteristic of current-driven SR, the converter modules can be paralleling without taking the risk of reverse power sinking. Paralleling 5 of such AC/DC modules can deliver a 1.5V low voltage at 200A [9]. No oring diodes are required.

V CONCLUSIONS

Some critical design issues, such as turn off delay and gate drive ringing in the operation of energy recovery current-driven SR are addressed and analyzed. Practical solutions to the addressed issues are proposed with equations derived for the calculations of circuit parameters and the required component values. Experiments with captured waveforms demonstrate the validity of the proposed solutions.

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