Current-Driven Synchronous Rectification Technique For Flyback Topology

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Abstract- **For low voltage, high current application, synchronous rectification technique can help improve efficiency in a flyback converter. This paper investigates some technical challenges within a synchronous rectification flyback converter. One of the major problems is that the discontinuous current mode (DCM) operation is not achievable with a control-driven or self-driven synchronous rectifier. Continuous current mode operation may introduce excessive RMS current and circulation energy at light load or high line condition. To solve this problem, we propose to use energy recovery current-driven synchronous rectifier for flyback topology. Analysis and experiments demonstrate the performance of this approach.**

I. INTRODUCTION

Flyback topology is widely adopted for small power (≤50W), isolated energy conversion. There is only one magnetic component in the flyback converter. So cost and size reduction can be easily achieved, especially for multi-output applications. It is generally known that a flyback converter can usually operate in either continuous current mode (CCM) or discontinuous current mode (DCM), or both modes, depending on the practical design and load/line conditions. If the flyback converter operates in both CCM and DCM, it can withstand high input voltage range and load current range. Some flyback converters are especially designed to operate in DCM. A popular example is the DCM flyback converter for single stage PFC.

The aim of this paper is to investigate the various synchronous rectification techniques for flyback topology. Synchronous rectification (SR) technique is widely used in low voltage, high current power conversion to minimize rectification loss and improve efficiency. There are hundreds of technical papers studying the SR techniques for forward, center-tap or current doubler topology. However, very few papers discussed the operation of synchronous rectification in a flyback converter [1]-[2]. There are several reasons behind. Firstly, flyback converter is rarely used for high current output. The flyback output filter is only composed of capacitor. With the secondary pulsating current, this filtering capacitor must have high capacitance value as well as low ESR value to suppress the output ripple. But when the output current is not quite high, say, for less than 10A output, flyback topology is still worth considering. Secondly, the popular self-driven SR solution theoretically cannot work within a flyback converter. This is because the turn off signal of the flyback SR should be issued prior to the primary switch turn on time to prevent cross conduction. If flyback SR is driven with a transformer coupled winding, turn off signal is always issued after the primary switch turn on time. As we can see from the next section, this will not be too much of a problem if we consider the practical transformer leakage inductance, SR MOSFET packaging inductance and the loop parasitic inductance. Thirdly, when self-driven or control driven synchronous rectification is implemented in a flyback converter, there is usually no DCM any more. When the secondary SR current drops to zero, because the SR is still driven on, the secondary current will go negative continuously until the SR gate signal is off. At light load or no load, there is still a significant amount of energy circulating between the primary and secondary. This surely increases the conduction loss. As mentioned before, DCM is especially popular for flyback topology. To achieve DCM operation in a SR flyback converter, a current sensing circuit is usually needed. In this paper, we propose to use an energy recovery current-driven SR for flyback topology. It allows SR to operate at both CCM and DCM. Before we go to the details of this current-driven solution, we first re-examine the conventional SR flyback solutions.

II. COMPARISON OF CONVENTIONAL SYNCHRONOUS RECTIFICATION SOLUTIONS FOR FLYBACK TOPOLOGY

A. Ideal Self-Driven SR Flyback Converter

Circuit diagram of an ideal self-driven synchronous rectification (SDSR) flyback topology is shown in Fig.1. The flyback SR is driven directly by a winding coupled from the flyback transformer. When the primary switch turns off, energy stored in the flyback transformer flows out first

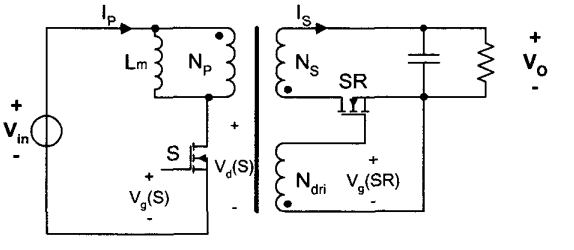

Fig.1 Ideal Self-driven Synchronous Rectification Flyback Converter

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through the body diode of SR. Then the SR is driven on by the reflected winding voltage. When the primary switch turns on, the input voltage applies directly to the primary winding. However, the output voltage also applies to the secondary winding due to the secondary continuous current. Two coupled windings are then clamped by two different voltage sources. For an ideal converter, the current in both windings should go up to infinity instantaneously. If the switches are implemented by real MOSFET, this current does not go infinite due to MOSFET resistive drop, but it also produces very high surge current across both the primary and the secondary loops. This surge current not only increases switching losses and current stress to the MOSFET switches, but also introduces serious EMI problem. Because of this SR turn off cross conduction problem, it is even pointed out in [1] that self-driven SR cannot be implemented in flyback converter.

B. Practical Self-Driven SR Flyback Converter

SDSR flyback may still work properly when practical leakage parameters are taken into consideration. A practical SDSR flyback circuit is shown in Fig.2. In the practical circuit, a power transformer always has some leakage inductance. A SR MOSFET has its packaging inductance. There also exists stray inductance associated with the PCB layout. Here the SR packaging inductance, secondary loop stray inductance and transformer secondary leakage inductance are merged together as a single L_{ks}. An auxiliary winding coupled from the main transformer is used to drive the flyback SR. Because the leakage energy will cause more or less resonant spike across the transformer windings, to prevent this resonant voltage from reaching the flyback SR gate terminal, a damping resistor and a buffer is added between the drive winding and SR gate. Another benefit of adding this buffer is that the SR doesn't need to suffer from the negative gate drive voltage during its off time. The input of the buffer is still the bi-directional voltage while the SR gate can only see the zero or positive voltage. It is easily seen that the SR can be turned on with some delay due to the damping process. Lucky that body diode can always conduct before the SR gate reaches its threshold. So the problem at turn on transient is mainly the loss due to body diode conduction.

The electrical model of flyback topology and its equivalent

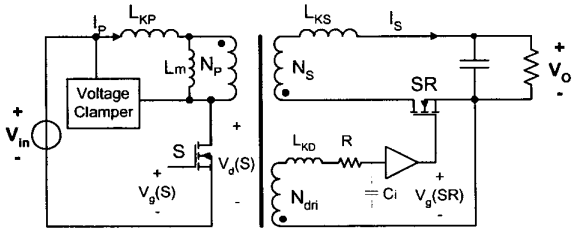


Fig.2 Practical SDSR Flyback Converter

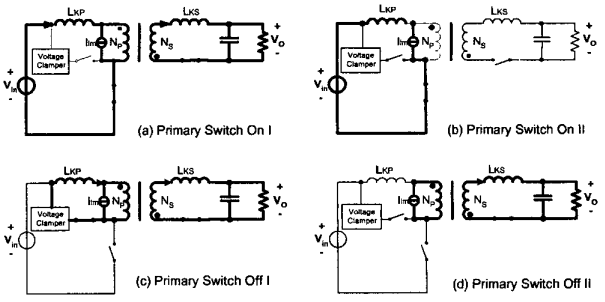
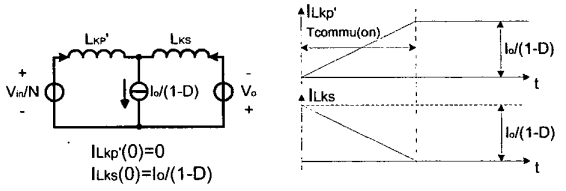
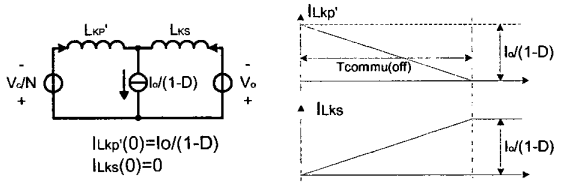


Fig.3 Four Operation Modes of Flyback Converter



(a) Turn on transient equivalent circuit



(b) Turn off transient equivalent circuit

Fig.4 Equivalent circuits at primary switch on/off transient

circuit at primary switch turn on transient are shown in Fig.3(a) and Fig.4 (a) respectively. Because of the existence of these inductive parameters, current commutation between the primary winding and the secondary winding is not instantaneous. The rate of commutation speed is determined by the voltage across the inductance parameters. With initial conditions, we can know the secondary current commutation period at turn on transient.

$$V_o = \frac{V_{in}}{N} \cdot \frac{D}{1-D} \tag{1}$$

$$L_{kp}' = L_{kp} / N^2 \tag{2}$$

$$T_{commu}(on) = \frac{(L_{ks} + L_{kp}') \cdot \frac{I_o}{1-D}}{V_{in}/N + V_o} \tag{3}$$

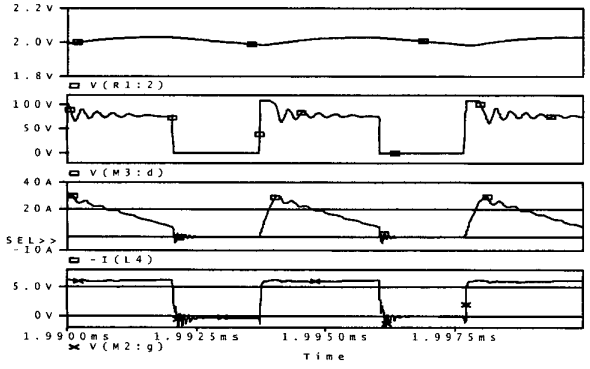
where D is the primary switch operation duty ratio.

From (1) and (2), equation (3) can be simplified as (4),

$$T_{commu}(on) = \frac{(L_{ks} + L_{kp}') \cdot \frac{D}{1-D} \cdot I_o}{V_o} \tag{4}$$

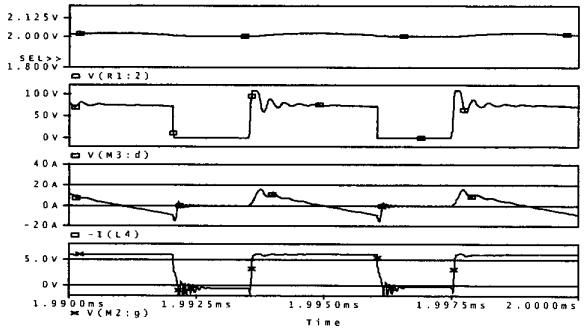
It can be seen from (4) that the higher the output current, or the lower the output voltage, the longer the SR current commutation period. During this commutation period, if SR can be turned off through the winding coupled voltage, the

remaining secondary current will be carried by the SR body diode. There is reverse recovery problem from the body diode conduction. However the previously mentioned overshoot doesn't actually happen if the shut down signal is issued during the current commutation. The following example will give you a better understanding of how long this commutation time can be. We assume the total secondary stray inductance is only 15nH. This estimation is rather conservative because even the SR MOSFET packaging inductance is already 12nH. The primary reflected leakage is neglected. If the output of flyback converter is 2V/10A, the operation duty is 0.4. From (4), we can know that the commutation time is as long as 50ns. This is usually long enough for the SR drive circuit to issue the turn off signal. Simulation of such a 48V input, 2V/10A output SDSR flyback converter is shown in Fig. 5. It can be clearly seen that the SDSR can be driven properly under this load condition. However, if the load current decreases, from (4), we know the commutation time also decreases correspondingly. The SR turn off time, which is mainly determined by the RLC parameters and the delay of the buffer, is almost invariable. This means the overshoot may occur when the output current is low and SR cannot shut down within the commutation period. The overshoot current is totally dependant to the parasitic inductance and the SR



Waveforms from top to bottom: Vo, Vds(pri), I_{SR}, Vg(SR)

Fig.5 Simulation of a 48V input, 2V/10A output SDSR flyback converter



Waveforms from top to bottom: Vo, Vds(pri), I_{SR}, Vg(SR)

Fig.6 Simulation of a 48V input, 2V/1A output SDSR flyback converter

turn off speed.

Flyback converter with diode rectification can operate at DCM automatically when secondary current drops to zero. In a SDSR flyback converter, the SR is controlled by the reflected winding voltage. In the case of light load, or high line input, SR current may drop to zero and continues to go negative linearly because the winding still drives SR on. This means the output capacitor releases energy back to the flyback transformer. The stored energy is then transferred back to the input when the primary switch turns on during the next switching cycle. Hence there is excessive circulating energy go back and forth between the input and output. It increases conduction loss significantly. When the SR has negative current, its RMS current is also much higher than in the DCM operation. This further increases the SR conduction loss. Simulation of the same SDSR flyback converter with 2V/1A output is shown in Fig.6. The reverse current can be seen from the simulation waveform.

C. Flyback Converter with Active Clamp and SDSR

Active clamp flyback topology was discussed thoroughly in [3]. With active clamp circuit, leakage energy can be effectively absorbed and ZVS can be achieved at the expense of increased circulating energy between the active clamp circuit and the primary transformer. During each switching cycle, only part of the stored energy in the primary inductance delivers to the secondary output. RMS current in both the primary side and the secondary side is much higher than the conventional flyback converter. Moreover, the active clamp flyback rectifier is shut down at its peak current. This is OK for a Schottky diode, but it is too bad for a synchronous rectifier due to the reverse recovery problem. Hence it is believed that active clamp SR flyback is not a good topology for the low voltage, high current application.

D. Control-Driven SR Flyback Converter

In a control-driven SR flyback topology, the secondary SR drive signal is derived from the primary switch. This is based on the idea that primary switch and flyback SR operate complementarily. There is usually some dead time between the primary switch gate signal and the secondary SR gate signal to prevent the current overshoot. This dead time also brings the body diode conduction loss and reverse recovery loss. Like SDSR flyback topology, the SR gate drive signal contains no current information. It cannot shut down the SR when SR current drops to zero. Hence there is also no DCM in the control-driven SR flyback topology.

E. SR Flyback with a secondary control IC

There are such kinds of control IC available in the market [4]. With a specially designed IC, SR drain voltage or the winding voltage is detected and then the IC generates drive signal for the SR. The IC can be designed for SR in both CCM and DCM operation. Application of these kinds of IC in

flyback topology is promising. Performance of these kinds of IC is worthy of further investigation.

F. Current-driven Synchronous Rectifier Flyback Converter

If we want to control the flyback SR so that it can work at both CCM and DCM, we can makes use of the current information flowing through the SR. In [5],[6], [7], an energy recovered current-driven SR is proposed. This new current-driven solution can be used in almost all switching topologies. Detailed description will be shown in section IV.

Generally speaking, the SR in the flyback topology can be self-driven, control-driven, or current-driven. Self-driven is a simple solution, but the turn off delay of SR may cause overshoot current if the turn off signal is issued after the secondary current commutation period. For low voltage, high current output, there is usually no problem because the commutation time is relatively long. Control-driven SR is also easy to be implemented. The dead time between the primary and secondary switches guarantees the flyback operation without cross conduction. But the flyback SR also suffers from body diode conduction loss and reverse recovery loss. One thing in common between these two approaches is that they all have no DCM. The only CCM operation is good from the control point of view, but not so efficient in energy delivering at light load. Current-driven SR is an excellent way to tackle all these problems.

III Comparison Of Ccm & Dcm In Sr Flback Converter

Although we can design a diode rectifier flyback converter so that it operates only in CCM under all the load and line conditions, it is usually not economical to do that. To maintain the CCM at light load and high line, a large inductance value is needed. This usually increases the size and cost of a flyback transformer. Most practical flyback converters prefer to operate in DCM at light load.

The condition that determines whether a flyback converter operates at CCM or DCM is given by (5), (6), (7)

$$\tau = \frac{L_s \cdot f}{R} \tag{5}$$

$$\tau_{crit} = \frac{(1-D)^2}{2} \tag{6}$$

$$K = \frac{\tau}{\tau_{crit}} \tag{7}$$

where τ and τ_{crit} are the system time variable and sytem time constants respectively,. f is the switching frequency. R is the load resistance. Ls is the transformer secondary inductance. D is a value determined by (1). It is the primary switch duty cycle in CCM operation.

If $K>1$, the flyback converter operates at CCM. If $K<1$, the flyback operation mode depends on which kind of rectifier is used. If a diode rectifier or the current-driven SR is used, the flyback converter runs into DCM. If the self-driven or control driven SR is used, the flyback converter still remains in CCM, but the secondary rectifier current falls below zero. This means the output has to deliver some amount of energy back to the input. We hereafter name this specific CCM operation mode as reverse energy transfer mode.

Because SR conduction loss is determined by its RMS current, we now analyze the SR RMS current under different operation modes. In the following analysis, this current is normalized by the flyback DC output current.

If the converter operates only in CCM mode, its normalized RMS current can be expressed by (8),

$$\frac{I_{rms}}{I_o} = \sqrt{\frac{1}{1-D} + \frac{R^2 \cdot (1-D)^3}{12 \cdot L_s^2 \cdot f^2}} \tag{8}$$

From (5), (6) and (7), we can simplify (8) as (9),

$$\frac{I_{rms}}{I_o} = \sqrt{\frac{1}{1-D} \cdot (1 + \frac{1}{3} \cdot \frac{1}{K^2})} \tag{9}$$

(8) and (9) are also valid for the flyback converter in the reverse energy transfer mode when $K<1$.

If the flyback converter operates at DCM when $K<1$, the normalized secondary RMS current can be found as (10)

$$\frac{I_{rms}}{I_o} = \sqrt{\frac{4}{3} \cdot \sqrt{\frac{R}{2 \cdot L_s \cdot f}}} \tag{10}$$

Also from (5), (6) and (7), (10) can be simplified as (11),

$$\frac{I_{rms}}{I_o} = \sqrt{\frac{4}{3} \cdot \frac{1}{1-D} \cdot \frac{1}{\sqrt{K}}} \tag{11}$$

It should be noted that in (11), the duty cycle is NOT the primary switch duty cycle at DCM. It is a system constant solely determine by (1).

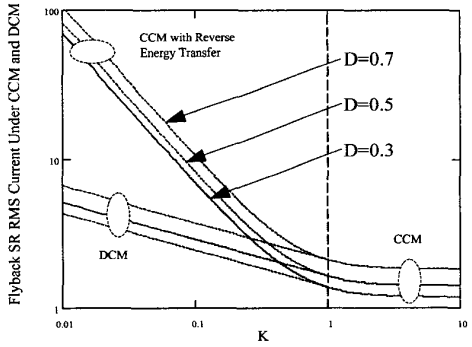


Fig.7 Normalized RMS Current Comparison under CCM and DCM in a SR flyback converter

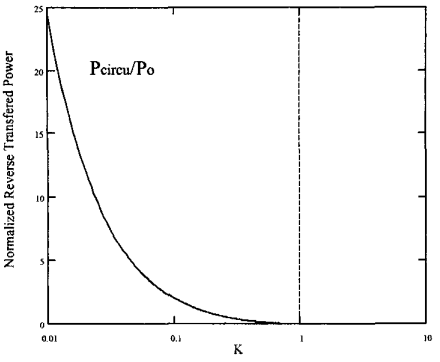


Fig.8 Normalized Reverse Transferred Power in CCM Flyback Converter

As shown in Fig.7, if $K>1$, in the CCM mode, we can see that normalized RMS current of flyback SR is always greater than 1. This means that the secondary SR current is always greater the output current. If K<1, RMS current which runs at CCM has much greater value than at DCM. The further away from $K=1$ point, the greater the difference. This indicates the significant conduction loss at reverse energy transfer mode.

The reverse transferred power can be calculated from (12). This power is normalized by the flyback output power.

$$\frac{P_{circu}}{P_o} = \frac{1}{4} \cdot (K + \frac{1}{K} - 2) \qquad (12)$$

where P_o is the flyback output power. This normalized circulation power is also shown in Fig.8. When K>1, there is no circulation power. This means all the power goes from the input side to the output side. When K<1, energy circulation between the primary and secondary begins. The smaller the K is, the greater the relative circulation power.

IV. Current-Driven Synchronous Rectification For Flyback Topology

An energy recovered current-driven synchronous rectifier (CDSR) was proposed in [5,6]. This current-driven SR is suitable for most switching topologies. With the recovery of current sensing energy, this current-driven solution can be applied at high frequency with high efficiency. Detailed analysis and operation description can be referred to [6].

Circuit diagram of the proposed current-driven SR is shown in Fig. 9. Here a small inductance is added in series with D1 to speed up turn off process. When a forward current flowing through the CDSR, this forward current will also be coupled to the gate drive winding and turn on the SR. The gate drive voltage will be clamped by the DC source through the N2 and N3 winding coupling. The current sensing energy taken it by N1 winding will be coupled to N3 winding and send to the DC source. This DC source is usually the DC output. When the forward current tends to go negative, the SR gate capacitance is then discharged by the drive winding reflected negative current.

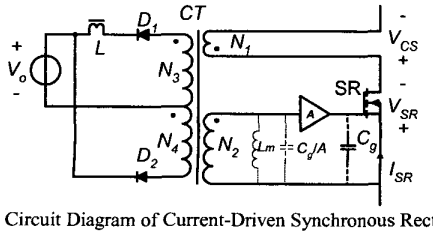


Fig.9 Circuit Diagram of Current-Driven Synchronous Rectifier

As the proposed current-driven solution drives the SR from the current signal it detects, it will introduce both turn on delay and turn off delay. The turn on delay is actually not so much of a problem because the SR has its internal body diode which can carry current before the gate signal is applied. The turn off delay should always be designed as small as possible to prevent reverse current overshoot in CCM. In DCM, this turn off delay is less important compared with in CCM because of the low rate of di/dt. In CCM, if there is no such a small inductor L, the turn off process starts at the time when the forward current drops to the point that is lower than the reflected transformer magnetizing current. After that, the magnetizing current together with the SR current begins to discharge the gate capacitance [6]. With this small inductor, the SR gate turn off process starts when high negative di/dt is applied to N1 winding. The small inductance will resonate with the gate capacitance and speed up the turn off process significantly. The small inductance is typically implemented with a small magnetic bean.

Practical implementation of a CDSR flyback converter is shown in Fig. 10. Its operation is very much like a diode rectifier flyback converter. Under load and line variation, it can automatically operate in either CCM or DCM.

A 250kHz current-driven SR flyback converter is built. It's input voltage is 48V. The output is 2V with 10A maximal current. Two switch clamping solution is used to effectively absorb the leakage energy. The SR is implemented with IRL3803S (6 mΩ). Current transformer has turn ratio of 1:39:13:3(N1~N4). The converter is designed to operate at CCM in 10A full load. At around 4A, it reaches the CCM/DCM boundary condition. It goes into DCM when load current is less than 4A. In Fig.11, the critical waveforms are captured at typical load current three typical load conditions. Because the SR flyback secondary loop is a low impedance path, to minimize the influence from the impedance of current probe, the transformer primary winding current is measured. Fig.11(a) shows the waveforms captured at 10A

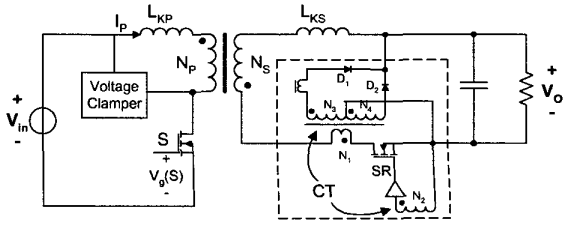
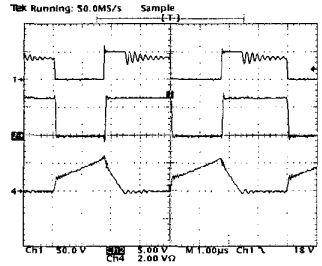
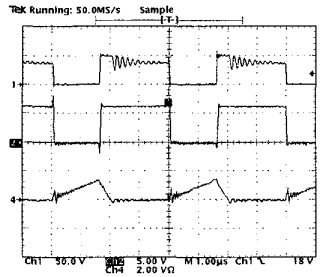


Fig.10 Circuit Diagram of A Current-Driven SR Flyback Converter

full load. The SR shuts down before the commutation time, so there is no cross conduction. Fig.11(b) shows the waveforms at 4A load current. There is a small amount of overshoot current because of the SR turn off delay. It should be noted that at this boundary condition, commutation time is around zero. So this is the worst case for cross conduction. The overshoot current surely increases the conduction loss, however its magnitude is not too high to be acceptable. Fig.11(c) shows the waveforms captured at 2A load current. The converter runs at DCM at this load condition. When the load current is lower than 1A, there is no sufficient current sensing energy to drive the SR on properly, the body diode is then into conduction. Converter efficiency is measured and shown in Fig.12. For comparison, efficiency of the same converter with control-driven SR solution and schottky diode rectifier is also measured. The schottky diode is implemented with one B2535L. It can be seen that efficiency of CDSR flyback can always be higher than the schottky diode up to 4% except at very light load when the CDSR cannot properly drive the SR. Control-driven SR can achieve higher efficiency than current-driven SR in CCM. This is because the current-driven SR has inherent conduction loss in the energy delivery diode D1 together with turn on and turn off loss [6]. But the efficiency difference is very small when the output current approaches full load where control driven SR suffers from the serious reverse recovery problem. At light load, the current-driven SR is obviously a winner. Control-driven method has very low efficiency at light load.



(a)



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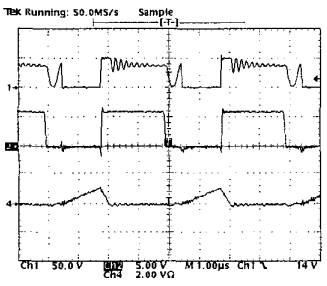
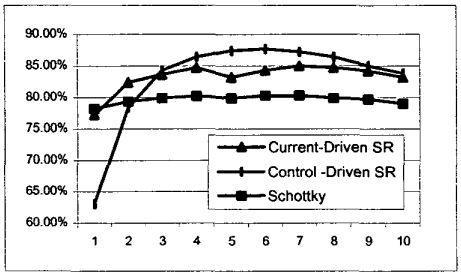


(c)

Waveforms from Upper to lower:

Primary lower switch drain voltage	(50V/div)
Flyback SR gate voltage	(5V/div)
Primary winding current	(2A/div)

Fig.11 Waveforms of 48V input, 2V/10A flyback converter under different load conditions



X: Load Current (A) Y: Efficiency

Fig. 12 Efficiency measurement under different load current

IV CONCLUSION

The DCM operation is widely used in diode rectifier flyback converter. With conventional self-driven or control driven SR, flyback topology can only operate at CCM. CCM operation at light load produces high RMS current and circulation energy. This causes high conduction loss under light load and high line. To tackle this problem, energy recovery current-driven SR is proposed for flyback topology. Current-driven SR flyback converter can operate at either CCM or DCM like a flyback diode converter. Experiments demonstrate the performance of this approach.

REFERENCES

[1] M. T. Zhang, M. M. Jovanovic and F. C. Lee, "Design considerations and performance evaluations of synchronous rectification in flyback converters," Power Electronics, IEEE Transactions on Volume: 13 3 , May 1998 , Page(s): 538 -546

[2] Alvarez-Barcia, L.; Ollero, S.; de la Cruz, E.; Canizales, F. "Low power multioutput converter with post-regulation based on synchronous rectification and windings integrated in the PCB." Applied Power Electronics Conference and Exposition, 1998. APEC '98. Conference Proceedings 1998., Thirteenth Annual Volume: 1 , 1998 , Page(s): 191 -197 vol.1

[3] Watson, R.; Lee, F.C.; Hua, G.C "Utilization of an active-clamp circuit to achieve soft switching in flyback converters." IEEE Transactions on Power Electronics Volume: 11 1 , Jan. 1996 , Page(s): 162 -16

[4] SRMOS. Inc. website: http://www.srmos.com

[5] X. F. Xie, J. C. P. Liu, F. N. K. Poon and M. H. Pong, "Two methods to drive synchronous rectifiers during dead time in forward topologies," Applied Power Electronics Conference and Exposition, 2000. APEC 2000. Fifteenth Annual IEEE Volume: 2, 2000 , Page(s): 993 -999 vol.2

[6] X. F. Xie, J. C. P. Liu, F. N. K. Poon and M. H. Pong. " A Novel High Frequency Current-Driven Synchronous Rectifier for Low Voltage High Current Applications," Applied Power Electronics Conference and Exposition, 2001. APEC 2001. Sixteenth Annual IEEE Volume: 1, 2001 , Page(s): 469 -475 vol.1

[7] Poon; Ngai Kit Frankie; Liu; Chui Pong Joe; Pong; Man Hay Bryan; Xie; Xue Fei, "Current driven synchronous rectifier with energy recovery," US patent No. 6,134,131