A CHIP-INTERLEAVING DS SS SYSTEM AND ITS PERFORMANCE UNDER ON-OFF WIDE-BAND JAMMING

X. Gui and T.S. Ng

Department of Electrical and Electronic Engineering
The University of Hong Kong
Pokfulam Road, Hong Kong

ABSTRACT

A modified direct sequence spread spectrum system employing the concept of chip-interleaving is proposed. Its performance under periodic on-off wide-band jamming is analyzed and closed-form bit error rate (BER) performances of the proposed system for both the best case and the worst case are obtained. The proposed system is compared with conventional system using numerical examples.

1. INTRODUCTION

The industry of cellular mobile communications is growing rapidly in recent years. Direct sequence spread spectrum (DS SS) modulation is known as an important competitive technology for mobile communication applications due to its many advantages [1]. Various types of interferences presented in the wireless channel can simply be categorized into narrow-band or wide-band as compared to the SS bandwidth. Although DS SS system has inherent immunity to narrow-band jamming, it can not survive from impulsive interfering which is wide-band in nature [2,3]. A chip-interleaving system was first proposed by Tachikawa and Marubayashi [4] and analyzed by Tachikawa [5] to combat periodic on-off wide-band jamming or "burst noise" in their terminology. In their system, the time intervals between the spreading chips are randomized by using multi-elements *m*-sequences or Tausworthe-Lewis-Payne (TLP) sequences and amplitude limiters are used [4,5]. However, accurate analysis of the system performance seems to be difficult.

In this paper, a novel chip-interleaving DS SS system is proposed which can combat impulsive jamming effectively. The system is easy to analyze and implement due to its simplicity. The paper is organized as follows: Section **2** describes the proposed chip-interleaving system. Performance analysis of the system under periodic on-off wide-band jamming is presented in Section **3**. Numerical results are presented and compared with conventional DS SS system in Section **4**. Finally, conclusions are drawn in Section **5**.

2. SYSTEM MODEL

The block diagram of the proposed system is depicted in Fig.1. A serial-parallel converter together with a rotary switch is required in both transmitter and receiver. The major difference of the proposed system from the conventional one is the order in which chips are transmitted. Let $\mathbf{B}=[\ b_1\ \ b_2\ \ \ldots\ \ b_M\ ]$, $\mathbf{A}=[\ a_1\ \ a_2\ \ \ldots\ \ a_L\ ]$, where $b_1\ \ b_2\ \ \ldots\ \ b_M$ is the sequence of data bit and $a_1\ \ a_2\ \ \ldots\ \ a_L$ is the PN sequence, M is the number of data bits and L is the number of PN chips per data bit, i.e., processing gain. If the bit duration and chip duration are denoted by T_b and T_c respectively, then $L=T_b/T_c$.

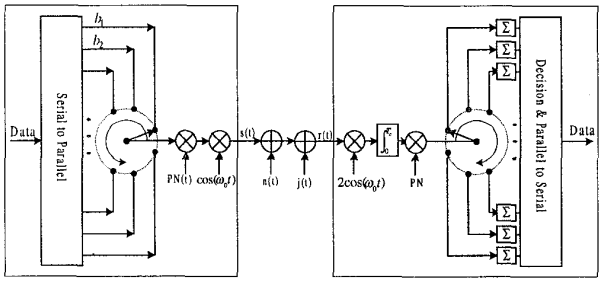

Fig.1. The proposed DS SS system

Define

$$\mathbf{D}=\mathbf{B}^{\mathrm{T}}\mathbf{A}=\begin{bmatrix} b_1 \\ b_2 \\ \vdots \\ b_M \end{bmatrix}\begin{bmatrix} a_1 & a_2 & \ldots & a_L \end{bmatrix}=\begin{bmatrix} d_{11} & d_{12} & \ldots & d_{1L} \\ d_{21} & \ddots & & d_{2L} \\ \vdots & & \ddots & \vdots \\ d_{M1} & d_{M2} & \ldots & d_{ML} \end{bmatrix} \quad (1)$$

where d_{ij} is actually the sequence being sent out. The emphasis here is the order of sending **D**. Conventional system transmits the contents of **D** row by row, left to right, while the proposed system transmits them column by column, top to bottom. To be specific, the sequence it sends out can be written as $d_{11}d_{21}\ldots d_{M1}d_{12}\ldots d_{M2}\ldots d_{1L}\ldots d_{ML}$. Thus, the adjacent chips of the same data bit is separated by M-1 chips from M-1 different information bits. It can be seen that the system transmits M information bits in MT_b duration, with processing gain L which is the same as that of conventional system. Note that when M equals one, the new system reduces to conventional system. Therefore conventional system can be considered as a special case of the proposed system.

Mathematically the spread spectrum signal transmitted by the proposed system using BPSK modulation can be represented by

$$s(t)=\sqrt{2P}\sum_{i=1}^{M}b_i\sum_{k=1}^{L}a_k u_{T_c}\left(t-(kM+i-1)T_c\right)\cos(\omega_0 t), \qquad (2)$$

where

$$u_{T_c}(t)=\begin{cases}1 & -MT_c\le t\le(-M+1)T_c\\ 0 & \text{elsewhere}\end{cases}$$

P and ω_0 are the power and carrier frequency of the DS SS signal, respectively. Note that the assumption of perfect synchronized coherent reception is adopted in the analysis of system performance.

3. PERFORMANCE ANALYSIS

The jammer model was described in [3], which is the same as that used in [5]. It is assumed that the noise produced by the jammer is also white Gaussian with increased power spectral density. The jammer operates periodically with on duration xT_b and off duration yT_b. When the jammer is on, the spectral power density of the noise is σ_j^2, when it is off, the noise reduces to background noise with variance σ_0^2, and $\sigma_j^2>>\sigma_0^2$. For brevity we consider the case that T_c is less than or equal to xT_b and yT_b, i.e., $x\ge 1/L$ and $y\ge 1/L$. For cases that T_c is larger than xT_b and/or yT_b, interested readers are referred to [3] for analysis of various combinations of T_c, xT_b and yT_b. We define function $m_k(s)$ as the fraction in the kth chip duration of a data bit that the jammer is on, where s is the distance of the starting edge of the first chip of a data bit from the starting edge of the jamming noise as shown in Fig.2.

From the figure, we see that $m_k(s)$ is a periodic function with minimum period $x+y$. For the first chip of a data bit, $m_1(s)$ can be obtained analogously as in *case 1a* of [3] and can be written as

$$m_1(s)=\begin{cases}1/L & 0\le s\le x-1/L\\ x-s & x-1/L\le s\le x\\ 0 & x\le s\le x+y-1/L\\ s-(x+y-1/L) & x+y-1/L\le s\le x+y\end{cases} \qquad (3)$$

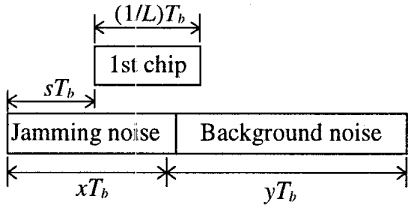

Fig. 2. Distance s between starting edges of jamming noise and the first chip of a data bit.

Since the adjacent chips of the same information bit are separated with distance $(M/L)T_b$, the portion of an information bit being affected by the jammer is found to be

$$\tilde{m}(s)=\sum_{k=1}^{L}m_k(s)=\sum_{k=1}^{L}m_1\left(s+(k-1)\cdot\frac{M}{L}\right). \qquad (4)$$

For a partially jammed BPSK signal, its probability of error is

$$P_e=0.5\,\mathrm{erfc}\left(\sqrt{\overline{\gamma_b}}\right), \qquad (5)$$

where

$$\overline{\gamma_b}=PT_b\Big/\left((1-\tilde{m}(s))\sigma_0^2+\tilde{m}(s)\sigma_j^2\right). \qquad (6)$$

Assuming the starting time of the jammer is random, s has a uniform distribution over the interval [0, $x+y$]. The proposed system performance can be calculated by averaging the P_e of Equation (5) over s, i.e.,

$$P_b=\frac{1}{x+y}\int_0^{x+y}\frac{1}{2}\,\mathrm{erfc}\left(\sqrt{\frac{PT_b}{(1-\tilde{m}(s))\sigma_0^2+\tilde{m}(s)\sigma_j^2}}\right)ds. \qquad (7)$$

In general, the explicit expression of $\tilde{m}(s)$ is unknown and we cannot obtain closed-form expression for Equation (7). In terms of overall system performance, it is desired that the system distributes the chips of a data bit evenly over the jamming period $x+y$ to minimize the effect of periodic on-off wide-band jamming and hence achieving the best performance. This can be achieved by adjusting the interleaving parameter M (Details on how to choose M are

given in [6]). When the chips of a data bit are evenly distributed over the jamming period $x+y$, equation (4) can be approximated by

$$\tilde{m}(s)=\frac{x}{x+y} \tag{8}$$

if L is large. Substitute (8) into (7), we obtain

$$P_b=\frac{1}{2}\mathrm{erfc}\left(\sqrt{\frac{PT_b}{\sigma^2}}\right), \tag{9}$$

where $\sigma^2=\left(y\sigma_0^2+x\sigma_j^2\right)/(x+y)$. Furthermore, the worst performance of the proposed system occurs when all the chips of the same data bit are located in the jammer-on period which results in extreme uneven distribution of jammed chips in data bits. Closed form BER of the worst case is obtained after some algebra and is given by

$$P_b=\overline{w}_0P_0+\overline{w}_jP_j+\overline{w}_0'P_0'+\overline{w}_j'P_j', \tag{10}$$

where

$$P_0=\frac{1}{2}\mathrm{erfc}\left(\sqrt{\frac{PT_b}{\sigma_0^2}}\right) \qquad P_j=\frac{1}{2}\mathrm{erfc}\left(\sqrt{\frac{PT_b}{\sigma_j^2}}\right)$$

$$P_0'=\frac{1}{2}\exp\left(-\frac{PT_b}{\sigma_0^2}\right) \qquad P_j'=\frac{1}{2}\exp\left(-\frac{PT_b}{\sigma_j^2}\right)$$

$$\overline{w}_0=y-\frac{1}{L}-\frac{1}{L}2\cdot\frac{\sigma_0^2+2PT_b}{\sigma_j^2-\sigma_0^2} \qquad \overline{w}_j=x-\frac{1}{L}+\frac{1}{L}2\cdot\frac{\sigma_j^2+2PT_b}{\sigma_j^2-\sigma_0^2}$$

$$\overline{w}_0'=\frac{1}{L}\frac{4}{\sqrt{\pi}}\cdot\frac{PT_b}{\sigma_j^2-\sigma_0^2}\sqrt{\frac{\sigma_0^2}{PT_b}} \qquad \overline{w}_j'=-\frac{1}{L}\frac{4}{\sqrt{\pi}}\cdot\frac{PT_b}{\sigma_j^2-\sigma_0^2}\sqrt{\frac{\sigma_j^2}{PT_b}}.$$

We shall point out that the worst case can always be avoided in the design.

4. NUMERICAL RESULTS

We compare the proposed system performance to that of conventional system under small duty cycle ($x \ll y$) on-off wide-band jamming. System parameters are chosen as follows: the jammer power $\sigma_j^2=100$, background noise power $\sigma_0^2=1$, processing gain L=127, jammer on duration x=0.5 and jammer off duration y=5. In Fig.3, we plot the system bit error rate (BER) performance versus signal energy per bit to background noise power ratio PT_b/σ_0^2. Both the best case and the worst case are shown in the figure. The performance of conventional system under such condition is also evaluated using the analytical result of [3]. In the figure two extreme cases, jammer is on all the time and jammer is off all the time, are also plotted. As shown in Fig.3, even a small duty cycle jammer can degrade conventional system performance significantly. On the other hand, the best case performance of the proposed system is substantially better under such conditions when the signal to background noise ratio PT_b/σ_0^2 is larger than 13dB. It is also shown in the figure that the worst case performance of the proposed system is approximately the same as that of conventional system.

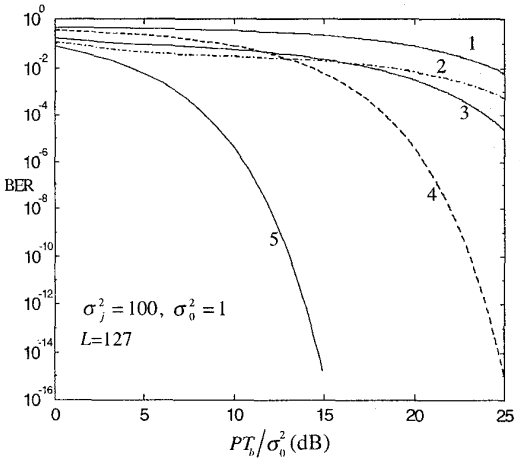

Fig. 3. BER performance comparison between the proposed system and conventional system under periodic wide-band jamming (x=0.5, y=5).

1. Jammer is on all the time
2. Proposed system — the worst case
3. Conventional system
4. Proposed system — the best case
5. No jammer

5. CONCLUSIONS

We have described a chip-interleaving DS SS system which can be considered as a generalization of conventional DS SS system. Its performance under periodic on-off wide-band jamming has been analyzed. It is found that under low duty cycle periodic on-off wide-band jamming, the proposed system, with proper choice of parameters, performs much better than the conventional system as the signal energy per bit to background noise power ratio increases. Numerical results show that the proposed system is very effective in combating low duty cycle on-off wide-band jamming when properly designed.

6. REFERENCES

[1] R.L. Pickholtz, D.L. Schilling, L.B. Milstein, "Theory of Spread-Spectrum Communications—A Tutorial", *IEEE Transactions on Communications*, vol.COM-30, no.5, pp. 855-884, May 1982.

[2] M.K. Simon, J.K. Omura, R.A. Scholtz and B.K. Levitt, *Spread Spectrum Communications* Volume 1, chapter 3, Computer Science Press, 1985.

[3] X. Gui, T.S. Ng, "Performance of DS SS System Under On-off Wide-Band Jamming", *IEE Electronics Letter*, vol.33, no.7, pp.557-559, 27th March 1997.

[4] S. Tachikawa and G. Marubayashi, "Spread Time Spread Spectrum Communication Systems", *Globecom'87*, 16.5, pp. 615-619, Nov. 1987.

[5] S. Tachikawa, "An Effect on Chip Interleaving and Hard Limiter against Burst Noise in Direct Sequence Spread Spectrum Communication Systems", *IEICE Trans. Fundamentals*, vol. E78-A, No. 2, pp. 272-277, Feb. 1995.

[6] X. Gui, T.S. Ng, "A Novel Chip-interleaving DS SS System", submitted to *IEEE Transactions on Vehicular Technology*, 1997.

ACKNOWLEDGMENT

This work was supported by the Hong Kong Research Grants Council and the CRCG of The University of Hong Kong.