A Novel Soft-Switching Double Modulation Converter (DMC)

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Abstract - **This paper introduces a new and simple converter topology by which both the amplitude and the duty cycle are modulated to achieve soft switching characteristic in a standard half bridge configuration. This novel Double Modulation Converter (DMC) is able to provide zero voltage switching and non-pulsating input ripple current. Constant switching frequency, simple control and gate drive circuit makes the DMC an ideal converter to fill the low to media power application gap in which the soft switching Phase Modulation method is costly to apply. The DMC is also applicable to full bridge for higher power output. An off-line 1MHz 50W DMC is built which demonstrates the high efficiency and the compactness of the converter.**

I. INTRODUCTION

Soft switching is a popular technique in switch mode power supply. With soft switching the switching losses of the switching device can be significantly reduced. In fact soft switching is inherent in some of the well-known topologies. Fig. 1 shows the theoretical circuit of a standard half-bridge topology and the actual equivalent model of a half-bridge configuration. Fig. 2 compares the ideal and practical waveform across the switch of a standard half-bridge configuration. The difference between the ideal and actual waveform is the spike which occurs at the trailing edge of every squarewave. In fact the spike comes in a form of resonate waveform determined by the equivalent series leakage inductance of the transformer and the equivalent C_s, stray capacitance, which is predictable and controllable.

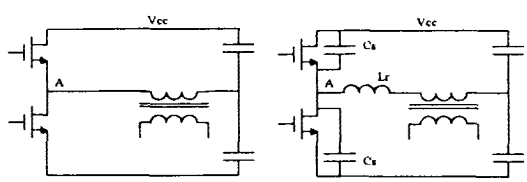
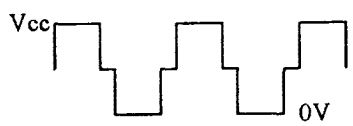
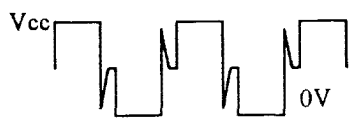


Fig. 1



Theoretical waveform at Pt. A



Actual waveform at Pt. A

Fig. 2

The actual waveform of Fig. 2 is a waveform well explained by many publications. The spikes at each edge of the squarewave had been treated as "unfriendly" waveform that engineers always attempted to reduce, usually by snubbing approach. In fact, the voltage spikes may be not so harmful.

Imagine that if the amplitude of the spike is high enough such that it reaches 0V or *Vcc* when one MOSFET turns off, the other MOSFET will experience a almost 0V(-0.7V) before it is turned on. By measuring the voltage across the MOSFETs, one can tell that the MOSFET have in fact turned on twice although it is designed to turn on once. The first "turn on" occurs when the MOSFET reverse conducts through its body diode and the second turn on is driven by the gate pulse. By increasing the duty cycle one can bring these two "turn on" closer until they finally coincide. In this case the switches turns on with zero voltage and there is no need to absorb the spike energy by snubbing.

In this paper a novel Double Modulation Technique is introduced. With this Modulation Technique zero voltage switching is obtained while the switching frequency remains constant.

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II. DOUBLE MODULATION TECHNIQUE

In traditional PWM configuration, possible zero-voltage switching can only occur at maximum duty cycle and the dead time is set to be small. It is no surprised that some engineers may experience a sudden increase in efficiency while the input voltage is dropped to the minimum value, and that is the condition in which the duty cycle is forced to maximum. By generalizing the zero-voltage switching condition, one may find that if the turning on of one MOSFET lags behind the turning off the other MOSFET by a short deadtime, the voltage swing generated by the turning off of the MOSFET may have energy to reach the voltage of the supply line. An intuitive solution of the above idea is to use the asymmetry gate drive technique to keep a short and constant dead time. Fig. 3 shows the DMC gate drive waveform compared to the conventional PWM gate drive waveform of a half-bridge configuration.

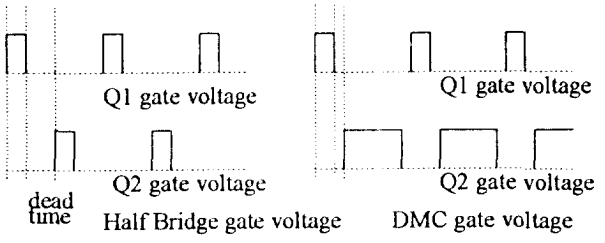


Fig 3

One can immediately see the merit of changing from the traditional symmetric PWM driving technique to the asymmetric DMC driving technique. For typical PWM topologies, it must have dead time in which both switches are turned off, usually no current is consumed from the supply voltage, and this dead time is dependent on the duty cycle. While any switch is turned on, the power source should supply current to energize the converter. It makes the supply voltage have to deliver a pulse current to the converter, which might cause EMI problems. One can see that the conventional PWM has variable dead time that is dependent on the duty cycle, but the DMC needs a constant and short dead time between two cycles. The short dead time allows zero-voltage soft-switching to occur as described before. Immediately a problem might arise that the unbalance driving technique may cause the transformer to saturate and one may need a series capacitor to block the DC component. Fortunately, in most cases, one does not need a series capacitor in the half bridge configuration to balance the offset caused by the unbalance waveform, since the two voltage dividing capacitors are already equivalent to the DC blocking capacitor. Fig. 4 shows a half-bridge and full-bridge configuration. Fig. 5 shows the detailed non-zerovoltage switching waveform at pont "A" of the tradition half bridge configuration. One can see that if one align the turn on of Q2 or Q1 right at the moment that the voltage reaches the supply rail or ground, one can obtain a zero-voltage switching. This is the time within tz' on Fig. 5.

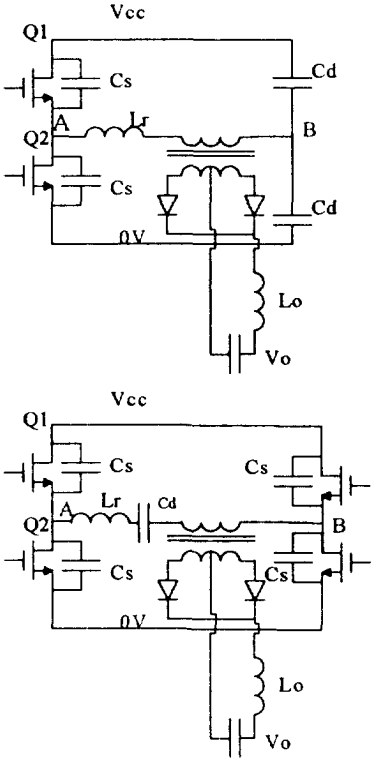


Fig. 4

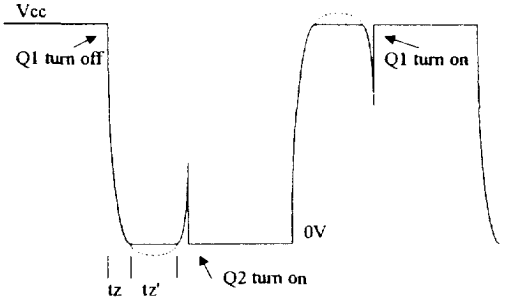


Fig. 5

III. DC AND AC ANALYSIS

In carrying out the analysis, a few assumptions are made : (a) all switches and diodes are ideal; (b) the magnetizing inductance of the transformer is large compared with the equivalent series inductance; (c) the load current is large enough to keep the circuit in continuous mode; (d) the total

dead time t_t is small and fixed in one cycle; (e) the shorter pulse drives the upper MOSFET and is defined as D; (f) half-bridge configuration is considered.

A. Output Voltage

Fig. 6 shows the output waveform injected to the inductor L_o *and* C_o, it is quite different with the traditional PWM waveform in the way that the amplitude of the rectified DMC waveform is changeable with the duty cycle. There are two levels of amplitude in one cycle and these amplitudes are variable. This waveform is the result of rectifying a AC PWM waveform generated by the transformer. According to the equalization of volt-second product of the output inductor L_o which should be equal to zero over a complete cycle, for $D_t = t_t / T$ one can then obtain the output voltage as,

$$V_o = 2NVccD(1 - D - D_t) \qquad (1)$$

Fig. 7 compares the characteristics of a flyback, forward and the DMC steady state output characteristic with $D_t = 0$.

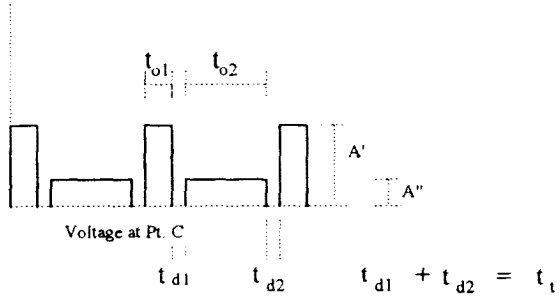


Fig. 6

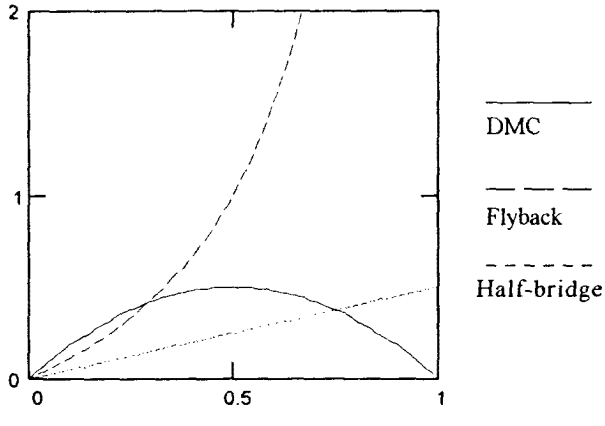


Fig. 7

One can observe that the characteristics of the output voltage regulation of the DMC lies between the flyback and the forward configuration. the major difference of the DMC with the other topologies is that the steady state response is symmetry about the duty cycle of D = 0.5, that mean the response is not monotonic, it will has a positive and negative response while it is operated on left or right of the axis of D = 0.5. One should bewared to set the duty cycle operate within D = 0 to 0.5 or operate with D = 0.5 to 1.

B. Zero-Voltage Switching

The basic behavior of the zero-voltage soft switching does not involve kind of resonate requirement, and one have to realize that zero-voltage switching does not really need a resonate state, the DMC only need the diode and the inductor to complete the zero-voltage switching. However there is always a stray capacitor C_s between the drain and source of the MOSFETs, and a short period of resonate waveform can be found. Just after one switch is turned off, the current flowing in the inductor L_r will try to find a path for itself and not to diminish. The diode of the other switch will provide a path for that current, and while the current flows through the diode, the switch will then obtain a zero-voltage state, and that is the right time to really turn on that switch. And this transient resonate state only last for a short period while the voltage waveform drop to -0.7V and turn on the body diode of the MOSFET. This state is represented as tz and shown on Fig. 5. The equivalent transient resonate model of the circuit become a simple L-C resonant circuit , Fig. 8 shows the equivalent, the initial condition is that the inductor current is equal to *Ip* for $t = 0$.

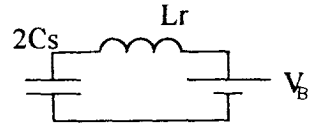


Fig. 8

The time t_z is different when the voltage at Pt. A is swing from Vcc to ground and swing from ground to Vcc[1][2][3], case 1 when the voltage is swing from Vcc to ground,

For $\omega = \dfrac{1}{\sqrt{2L_rC_s}}$

and V_B = voltage at point "B"

$$t_z = \frac{1}{\omega} * \tan^{-1}\left(\frac{I_p\sqrt{L} - \sqrt{I_p^2 L - 4C_s V_{cc} V_B + 2C_s V_{cc}^2}}{\sqrt{2C_s}\,(V_{cc} - 2V_B)}\right), \quad (2)$$

Case 2, when the voltage is swing from ground to Vcc,

$$t_z = \frac{1}{\omega} * \tan^{-1}\left(\frac{I_p\sqrt{L} - \sqrt{I_p^2 L + 4C_s V_{cc} V_B - 2C_s V_{cc}^2}}{\sqrt{2C_s}\,(V_{cc} - 2V_B)}\right), \quad (3)$$

It is obvious that if the solution of the t_z has a complex solution, it implies that the voltage swing at point A cannot reach the ground or V_{cc}. The reason is because energy store in the inductor is not enough to charge or discharge the capacitor C_s to V_{cc} or ground. And that is one should avoid.

Once the voltage is swing to V_{cc} or ground, the voltage will be clamped to V_{cc} or 0V by the turning on of the body diode of the MOSFETs, the voltage will be hold until the current flows through the inductor L_r diminishes to zero. One call this interval as $t_{z'}$. During the time interval $t_{z'}$ current will flow though the body diode of the MOSFET, then pass though the leakage inductance and finally to the supply lines. In this interval, *the reverse conducting MOSFET should be turned on to achieve zero voltage switching.*

For $V_{difference}$ = |*Pt. B voltage - Pt. A voltage*|,

and $V_B = V_{cc}\frac{D}{1 - D_t}$,

Case 1, the voltage is swinging from V_{cc} to ground,

$$I_{p'} = 2C_s\left[\frac{I_p}{2C_s}\cos(\omega t_z) + \frac{(V_{cc} - V_B)}{\omega}\sin(\omega t_z)\right], \quad (4)$$

Case 2, the voltage is swinging from ground to V_{cc} ,

$$I_{p'} = 2C_s\left[\frac{I_p}{2C_s}\cos(\omega t_z) + \frac{V_B}{\omega}\sin(\omega t_z)\right] , \quad (5)$$

Where $I_{p'}$ is the current flow through the inductor L_r at the time t_z , and by simple physical law, one can immediately obtain the interval $t_{z'}$ is,

$$t_{z'} = \frac{L_r I_{p'}}{V_{difference}} , \quad (6)$$

C. Dynamic Analysis

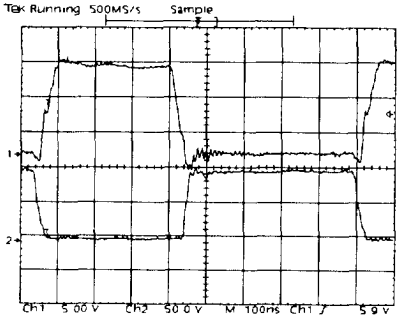
The output waveform of the transformer is so different from any ordinary type converter, one have to derive new dynamic transfer characteristics. By the average modeling method [4] , the dynamic transfer function is,

$$\frac{V_o(s)}{D(s)} = \frac{2NV_{cc}(1 - D_t - 2D)}{1 - D_t}\frac{1}{L_o C_o}\frac{1}{(s^2 + \frac{s}{R_o C_o} + \frac{1}{L_o C_o})}, \quad (7)$$

The system is described to be a non-linear system since the gain is dependent on the duty cycle D and the small signal response is a typical second order response. One should be very careful that the AC gain will move from the positive region to the negative while the duty cycle D is going from less 0.5 to greater than 0.5 while the D_t is assumed to be zero. In actually design, one can only use either the positive or negative region.

IV. EXPERIMENTAL RESULT

A half bridge prototype has been build which runs at 1MHz switching frequency, by choosing the value of Lr = 13 uH, Cd = 0.022uF, transformer ratio N = 6/16, Cs = 100pF. Fig. 9 shows the gate drive waveform at the lower MOSFET $Q2$ and the voltage waveform at the junction of the MOSFETs of *Pt.A*. Fig. 10 compares the measured and theoretical result of DC output voltage against the duty cycle for Vin = 140V, Io=2.5A, switching period T = 850nS , D_t =0.12,



Vgs of Q2

Vds of Q2

Fig. 10

The upper trace is the gate driver waveform and the lower trace is the drain voltage of the MOSFET Q2, one can obtain

a very smooth and near perfect wavefrom at 1MHz switching frequency.

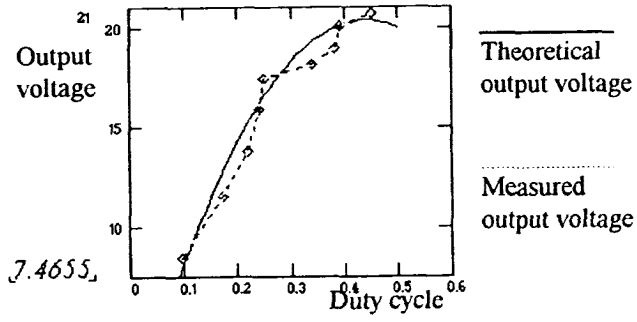


Fig. 11

The TO-220 package MOSFETs being used in this prototype require no heat sinks with soft-switching. The temperature rise is only 35°C. With a MOSFET thermal resistance of 62.5°C/W, one can roughly estimate that the losses on each MOSFET is 0.56W. The conduction resistance of the MOSFET is 1.5 ohm, the conduction loss of each MOSFET is 0.45W. Comparing the total loss and the conduction loss, the switching loss is merely 0.11W which is very much reduced compared to conventional configurations which is usually a few times that of the conduction loss. Fig. 12 shows the input current waveform in the presence of a 0.22uF filtering capacitor at the input, and Fig. 13 shows the dynamic transfer characteristics of the system.

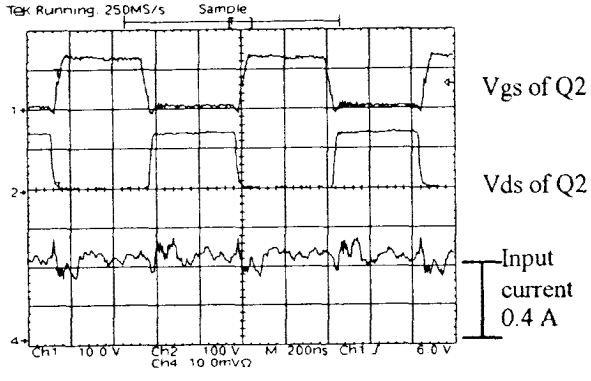


Fig. 12

The trace of Fig. 12 are gate driver waveform, drain voltage waveform and input current waveform respectively. One can see the current waveform is non-pulsating, low EMI is inherent since there are no sharp rising or falling edges of current. Also the AC response is very close to prediction. The theoretical overshoot at high frequency is due to the neglected internal resistance of the L_o *and* C_o.

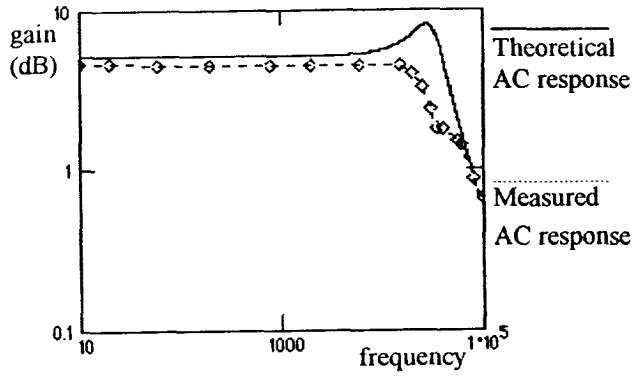


Fig. 13

V. CONCLUSION

Soft switching can reduce the switching losses and DMC provides almost continuous input current conduction on each cycle because of the small and fixed dead time. A very simple filter can smooth the input current to a desired level with low EMI. The low losses make the 50W half bridge prototype work without heatsinks which enables the whole circuit to be packed to a very small size.

Most soft-switching technique require a lot of auxiliary switches and components to fulfill the zero-voltage characteristic. This deters engineers from applying it to low power and cost sensitive application. The merit of DMC is that it can be immediately applied to any standard half/full bridge configuration, the simple control and drive technique make it readily applicable in the industry.

A Patent has been applied for the configuration of DMC.

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