A PFC Voltage Regulator With Low Input Current Distortion Derived From a Rectifierless Topology

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***Abstract*—This paper presents an ac–dc converter topology for realization of power factor correction (PFC) voltage regulators for applications where the mains frequency is high and a low input current harmonic is required, e.g., in aircraft power systems. The proposed converter represents a minimal configuration consisting of two basic converters, which can be systematically derived from a previously proposed general synthesis procedure for rectifierless ac–dc converters. The proposed PFC converter has incorporated a control method which drastically reduces the circulating power and hence raises the efficiency to a level comparable to existing PFC converters. The proposed PFC converter can completely eliminate any crossover distortion, which can be significant for supply systems having a high mains frequency. In addition, the proposed converter allows bidirectional energy flow ensuring all inductors work in continuous conduction mode hence eliminating the distortion due to the abrupt change of dynamic response when the operating mode changes. Analysis and design of the power and control circuits will be given and discussed. An experimental system will be presented for verification purposes.**

***Index Terms*—AC–DC converter, airborne application, low distortion, power factor correction (PFC), rectifierless converter.**

I. Introduction

THE AIM of power-factor-correction (PFC) converters is to reduce the input current harmonics and provide high power factor to the ac mains supply. A bridge rectifier followed by a boost converter operating at critical conduction mode or in continuous conduction mode under average current mode control is being widely used for PFC applications because of its simplicity [1], [2]. Researchers have revealed two major distortions in boost type PFC configurations [3], [4].

1) It has been shown by Sun [3] that the use of the average current mode control method and a filtering capacitor placed after the input bridge rectifier for eliminating high-frequency ripple current will introduce a leading phase to the input current relative to the input mains. Near the zero crossing point of the input ac voltage, the input current reverses in advance of the voltage due to the phase lead, and the input bridge rectifier will be reverse biased and cease to conduct current. This causes a step change in the input current and gives rise to crossover distortion. The significance of this distortion increases with the mains frequency and can be very serious when the power system operates at 400 Hz or above in airborne applications. Fig. 1 shows the crossover distortion of input current of a PFC caused by the phase lead of input current to the mains voltage and the input bridge rectifier.
2) Another distortion is caused by the change of operating mode of the boost inductor when the load and/or input voltage is changed. The dynamics of the converter changes abruptly, causing distortion to the input current. Although critical conduction mode operation can alleviate the problem, it is undesirable for high power applications since the high ripple current flow in the inductor and switches increases the conduction loss. Moreover, the problem can be reduced by adding a special correction factor to the input current sampling circuit [4], at the expense of an increased complexity of the control circuits. Fig. 2 shows the distortion at the change of operating mode.

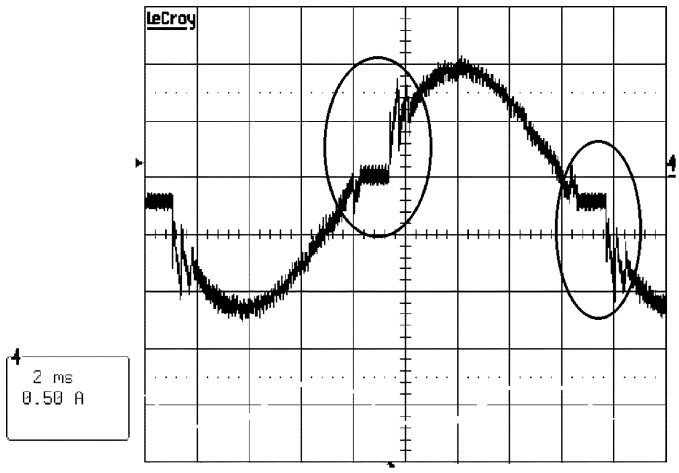

Fig. 1. Crossover distortion.

In this paper, we propose a PFC converter topology that can eradicate the distortions described above. This topology is derived from the general synthesis procedure for rectifierless ac–dc conversion topologies presented in Liu *et al.* [5]. It represents a minimal configuration consisting of only two basic converters that can accomplish the required objectives of PFC and voltage regulation. The basic idea is to use two

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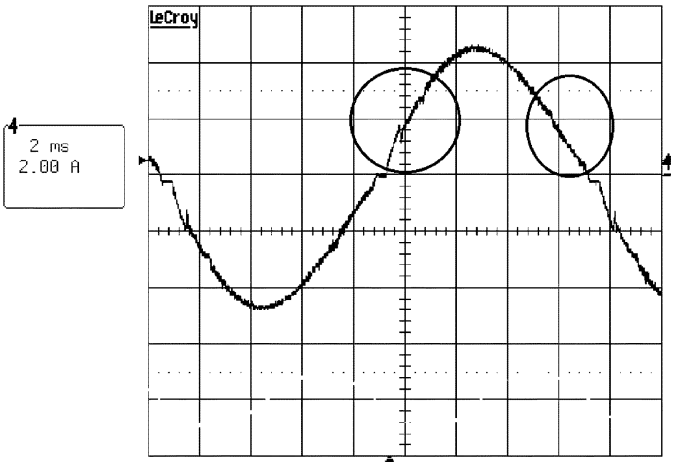


Fig. 2. Distortion due to mode change.

dc–dc converters to provide a dc stacking voltage to the ac input voltage, thereby preventing polarity change of the input voltage and hence eliminating the need for input rectifiers. The specific converter configuration chosen for this application is shown in Fig. 3(a). Also, the specific choice of constituent dc–dc converters, as shown in Fig. 3(b), has been found to give lowest voltage stress on the switches. Moreover, it has been revealed [5] that this rectifierless topology suffers from circulating power loss, which becomes significant when the stacking voltage is large. Thus, in this paper, instead of using a constant dc stacking voltage, we introduce a variable stacking voltage, resulting in significant reduction of the circulating power and loss.

A remark worth mentioning, before we describe details of the circuit, is that the circuit looks a *prima facie* kind of four-quadrant converter. However, we demonstrate in this paper how such a circuit can be systematically decomposed into two basic dc–dc converters, thus allowing suitable control strategies to be more readily developed to satisfy any desired operation.

This paper is organized as follows. In Section II, we will review the operation of the proposed circuit, and explain how circulating power loss can be reduced in this circuit. In Section III we will present experimental results verifying the operation of the circuit and its ability of eliminating distortion at high line frequency (400 Hz). Finally, Section IV gives the conclusion.

II. Operation Analysis

The power conversion stage consists of two dc–dc bidirectional converters, as shown in Fig. 3(b). DC–DC converters 1 and 2 are boost and buck converter according to the power flow directions shown by the solid arrows. To realize the input rectifierless ac–dc conversion, dc–dc converter 2 should provide a stacking voltage $\xi(t)$ to the mains Vi such that the input voltage of dc–dc converter 1, V_1, is always positive regardless of V_i. To satisfy this condition, the output voltage U and $\xi(t)$ must satisfy

$$U > D_2(t)U = \xi(t) > E\sin 2\pi f_e t \quad \text{for all } t \tag{1}$$

where all symbols are defined in Fig. 3.

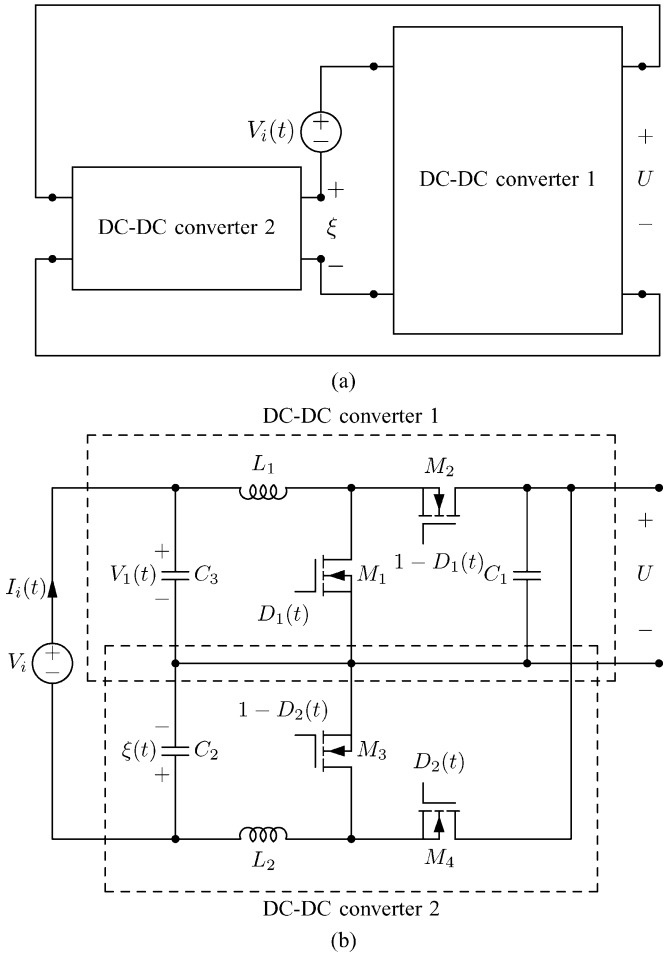


Fig. 3. Rectifierless ac–dc converter circuit: (a) general configuration [5] and (b) specific circuit choice with the boost and buck converters realizing the two constituent dc–dc converters.

This implies that U must be greater than the amplitude of the input ac voltage E and the overall conversion is a step-up operation. Since the conversion ratio of dc–dc converter 1 is equal to $1/(1 - D_1(t))$, the relationship between $U, V_i, D_1(t)$, and $D_2(t)$ is given by

$$U = \frac{V_i}{1 - D_1(t) - D_2(t)}. \tag{2}$$

A. Reduction of Circulating Power

The topology used for PFC converter implementation has a drawback in conversion efficiency due to circulation power. It has been shown in [5] that the circulating power is equal to $4\xi/\pi E$ times the output power P_o when stacking voltage ξ is kept constant. This means that the minimum circulating power flows around dc–dc converters 1 and 2 is $4P_o/\pi$ since ξ must be greater than E. To reduce the circulating power, we propose to add a time varying component, which is in anti-phase to V_i, to the stacking voltage in order to provide "just enough"stackup dc voltage during the negative cycle. It can be done by equating the duty cycle of M_1 and M_4, i.e., $D_2(t) = D_1(t) = D(t)$. Under this condition, the stacking voltage $\xi(t)$ as well as the

output voltage U and the input voltage to dc–dc converter 1 can be derived as follows.

$$U = \frac{V_i}{1-2D(t)} \text{ or } D(t) = \frac{1}{2}\left(1 - \frac{V_i}{U}\right) \tag{3}$$

$$\xi(t) = D(t)U = \frac{1}{2}(U - V_i) \tag{4}$$

$$V_1(t) = \xi(t) + V_i = \frac{1}{2}(U + V_i). \tag{5}$$

We can see that $\xi(t)$ contains a time varying component $V_i/2$, which is in antiphase to V_i. In addition, (5) shows that V_1 is always positive with $U > E$ and satisfies the basic requirement.

To derive the circulating power when the converter operates for PFC, we can assume that the input current I_i is controlled to follow the shape of the mains V_i with amplitude equal to $2P_o/E\eta_{\text{overall}}$,where η_{overall} is the overall efficiency of the converter, i.e.,

$$I_i = \frac{2P_o}{E\eta_{\text{overall}}} \sin 2\pi f_e t. \tag{6}$$

Then, the circulating power $P_{\text{circulate}}$ is given by [5]

$$\begin{aligned} P_{\text{circulate}} &= 2f_e \int_0^{1/2f_e} (V_i + \xi(t)) I_i .dt - P_o \\ &= \left(\frac{2U}{\pi E\eta_{\text{overall}}} - \frac{1}{2}\right) P_o. \end{aligned} \tag{7}$$

It can be seen that the minimum circulation power $(2/\pi - 1/2)P_o$ can be achieved when U is made close to E. The circulating power is reduced by a factor of 9.32 when compared with $4P_o/\pi$.

Obviously, if η is the efficiency of each constituent converter, the total loss due to the circulating power is

$$\text{loss}_{\text{circulate}} = 2P_{\text{circulate}}\left(\frac{1}{\eta} - 1\right). \tag{8}$$

Also, as power goes directly to the output through dc–dc converter 1, the loss is

$$\text{loss}_{\text{direct}} = P_o\left(\frac{1}{\eta} - 1\right). \tag{9}$$

Hence, the overall efficiency is

$$\begin{aligned} \eta_{\text{overall}} &= \frac{P_o}{P_o + \text{loss}_{\text{circulate}} + \text{loss}_{\text{direct}}} \\ &= \frac{P_o}{P_o + P_o\left(\frac{1}{\eta} - 1\right)\left(\frac{4U}{\pi E\eta_{\text{overall}}}\right)} \\ &= 1 - \frac{4U}{\pi E}\left(\frac{1}{\eta} - 1\right). \end{aligned} \tag{10}$$

Alternatively, we can write

$$\eta = \frac{1}{1 + \frac{\pi E}{4U}(1 - \eta_{\text{overall}})} \tag{11}$$

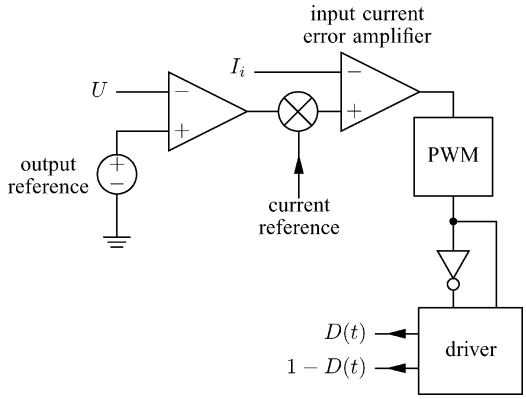


Fig. 4. Simplified schematic of the control circuit for power factor correction. Current reference is derived from V_i. Output reference is derived from the amplitude of V_i.

which can be used to estimate the constituent converter efficiency from the measured overall efficiency.

Remarks: From the foregoing discussion, the two converters seem to be processing power redundantly, doubling the overall converter size. However, using the proposed control of the circulating power, the net increase in the power processed by each converter is not significant. For instance, under the conditions of an anti-phase stacking voltage and the afore-described controlled output voltage, the maximum circulating power is about 13.67% of P_o. During the positive half cycle of the input voltage, converter 1 processes an average power of $1.1367P_o$, while converter 2 processes an average power of $0.1367P_o$. By symmetry, during the negative half cycle, converter 2 processes an average power of $1.1367P_o$ while converter 1 processes an average power of $0.1367P_o$ Therefore, each converter processes $0.6367P_o$, and the whole converter thus processes an average power of $1.2733P_o$. The overall increase of the converter size is not doubled, but only about 27.33%.

B. Control Circuit Realization for PFC

The simplified control circuit shown in Fig. 4 is used for the PFC control. The input current error amplifier forces the input current to follow the reference derived from V_i. The reference voltage for regulating the output voltage U is made proportional to the input voltage amplitude. This makes U decrease with E and reduces the ratio U/E at low ac voltage input which helps to reduce circulation power derived in (7). The theoretical basis of the control possibility has been discussed in [2],[6].

III. Experimental Results

A PFC converter using the proposed topology has been built for verification. The operating switching frequency is 50 kHz. The output voltage was made to vary with the input mains amplitude as described in the previous section. The current sensing has been implemented indirectly as shown in Fig. 5. Since the input current is proportional to the differential voltage across the sensing resistors R_{s1} and R_{s2}, it can be obtained using a differential amplifier as shown in Fig. 5. All MOSFETs are IRFB18N50. Also, the input filter takes the form of a standard

TABLE I
EXPERIMENTAL RESULTS

Test	Input Voltage	Output Voltage U	Output Power P_o	Measured Efficiency η_{overall}
1	90 V (rms)	174.4 V	100 W	**93.8** % (with circulating power control)
2	90 V (rms)	382.6 V	100 W	87.3 % (without circulating power control)
3	230 V (rms)	380.2 V	100 W	**94.5** % (with circulating power control)

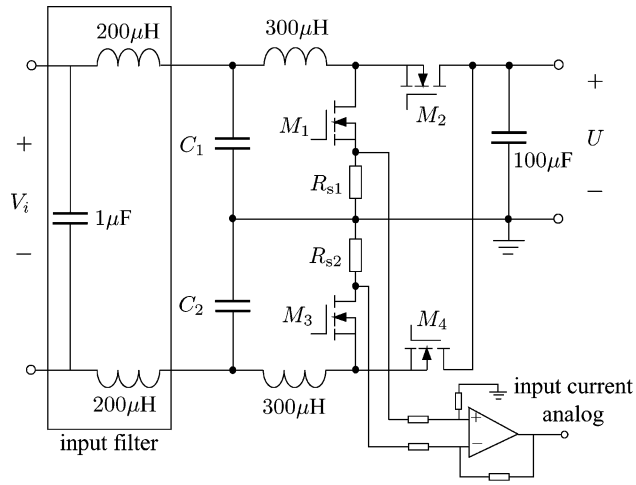


Fig. 5. Experimental circuit showing input current sensor and input filter. The current sensing circuit makes use of the property that the input current is proportional to the differential voltage across R_{s1} and R_{s2}.

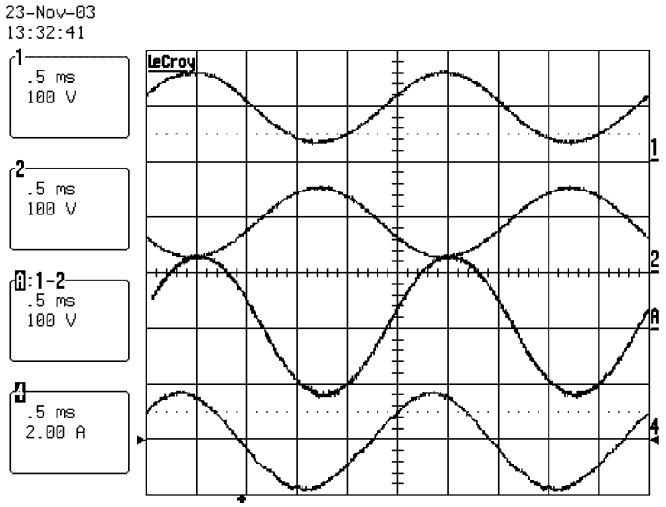


Fig. 7. {Waveforms of V_1 (Ch1), $\xi(t)$ (Ch2), V_i (ChA), and I_i (Ch4), for input voltage 90 V (rms) and line frequency 400 Hz.

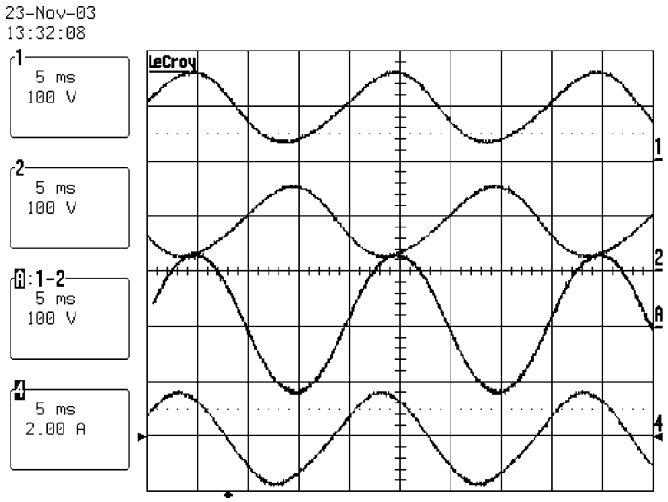


Fig. 6. Waveforms of V_1 (Ch1), $\xi(t)$ (Ch2),V_i (ChA), and I_i (Ch4), for input voltage 90 V (rms)and line frequency 50 Hz.

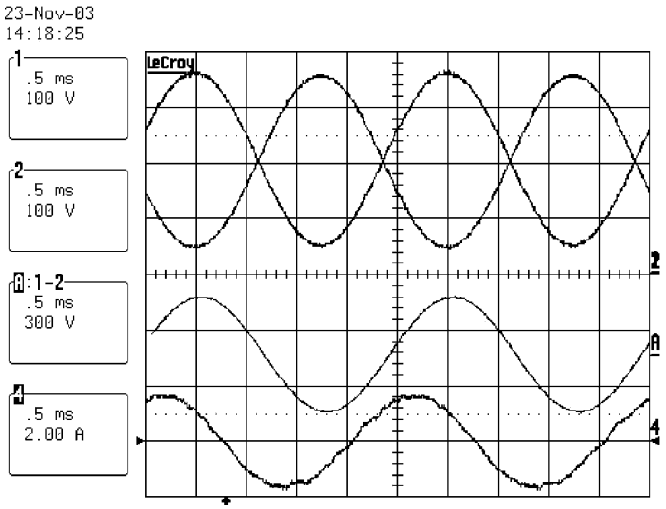


Fig. 8. Waveforms of V_1 (Ch1), $\xi(t)$ (Ch2),V_i (ChA) and I_i (Ch4), for input voltage 230 V (rms) and line frequency 400 Hz.

differential-mode filter, which consists of two 200 μH inductors and a 1 μF capacitor.

Some test results are shown in Table I. From the results of Test 1 and using (11), we can estimate the constituent converter efficiency η, i.e., $\eta = 96.6\%$. We can check consistency with the results of Test 2. Assuming $\eta = 96.6\%$ for Test 2 (without circulating power control), we get the overall efficiency as 86.5%, which agrees with the measured one. Test 3 repeats Test 2 with a different set of input and output voltages.

Fig. 6 shows the operating waveforms of $V_1, \xi(t), V_i$, and I_i. We can see that $\xi(t)$ is in anti-phase to V_i and its magnitude reduces when V_i is positive in order to reduce the circulation power.

Figs. 7 and 8 show the operating waveforms at 400-Hz mains frequency and no significant distortion has been found. Fig. 9 is the blow-up waveforms of V_i and I_i, and no crossover distortion has been observed even when a noticeable phase lead of the input current due to the input filter is present at 230-V, 400-Hz input.

Fig. 10 show the operating duty cycle at different values (0 V and 300 V) of V_i. The calculated (using (3)) and the measured duty cycles are in perfect agreement. At $V_i = 0$ the calculated

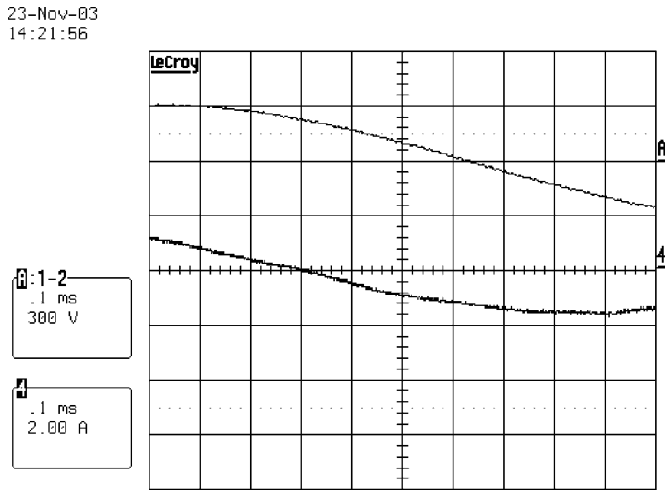
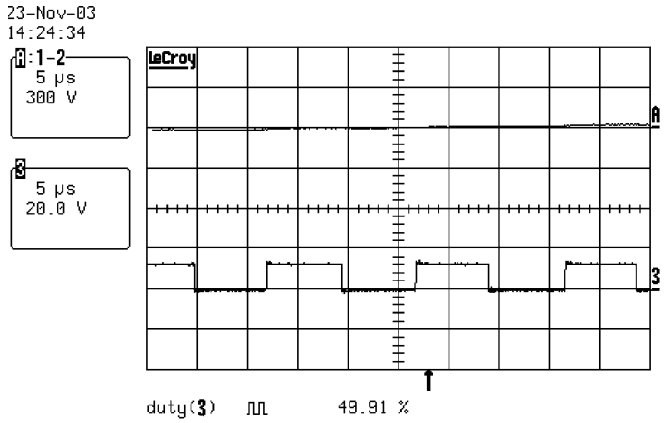
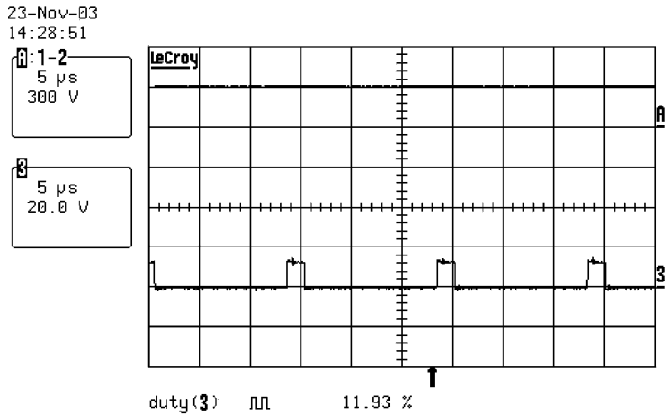


Fig. 9. Close-up view of waveforms of V_i (ChA) and I_i (Ch4), for input voltage 230 V (rms) and line frequency 400 Hz.



(a)



(b)

Fig. 10. Waveforms of V_i (ChA) and $D(t)$ (Ch3) at (a) zero crossing point and (b) input voltage 300 V.

and measured duty cycle are 0.5 and 0.499 while at $V_i = 300$ V the calculated and measured duty cycle are 0.105 and 0.119, respectively.

IV. Conclusion

An input rectifierless PFC converter with low input current distortion has been proposed and verified experimentally. It eradicates the crossover distortion due to the input rectifier and the phase lead of input current introduced by the filter and control circuits in conventional PFC converters, which is a significant problem at high mains frequencies. No distortion due to mode changing has been found since the converter allows bidirectional energy flow and all inductors work at continuous conduction mode at all times. An important design feature of this converter is that a control circuit has been designed to reduce the circulation power and provide higher conversion efficiency. This makes the proposed PFC converter suitable for airborne power systems requiring low input current harmonics with a relatively high mains frequency. Possible future work may proceed along the idea of rectifierless configurations [7] as well as other practical design tradeoff considerations [8]. Finally, it should be pointed out that the two-converter configuration described in this paper represents a minimal converter configuration that can be used to emulate any input impedance, not limited to pure resistance [9].

References

[1] R. Redl, "Power-factor-correction in single-phase switching-mode power supplies," *Int. J. Electron.*, vol. 77, no. 5, pp. 555–582, May 1994.

[2] C. K. Tse, "Circuit thoery of power factor correction in switchingconverters," *Int. J. Circuit Theory Appl.*, vol. 31, no. 2, pp. 157–198, Mar. 2003.

[3] J. Sun, "Demystifying zero-crossing distortion in single-phase PFC converters," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2002, pp. 1109–1114.

[4] K. de Gusseme, D. M. V. de Sype, A. P. van den Bossche, and J. A. Melkebeek, "Sample correction for digitally controlled boost PFC converters operating in both CCM and DCM," in *Proc. IEEE Appl. Power Electron. Conf. Expo*, Feb. 2003, pp. 389–395.

[5] C. P. Liu, C. K. Tse, N. K. Poon, B. M. H. Pong, and Y. M. Lai, "Synthesis of input-rectifierless AC-DC converters," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 176–182, Jan. 2004.

[6] C. K. Tse and M. H. L. Chow, "Theoretical study of switching converters with power factor correction and output regulation," *IEEE Trans. Circuits Syst.*, vol. 47, no. 7, pp. 1047–55, Jul. 2000.

[7] A. Ikriannikov and S. Ćuk, "Direct ac-dc conversion without input rectification," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 1999, pp. 181–186.

[8] C. Zhou and M. Jovanović, "Design trade-offs in continuous current-mode controlled boost power-factor correction circuits," in *Proc. High Freq. Power Conv. Conf.*, Apr. 1992, pp. 209–220.

[9] J. C. P. Liu, C. K. Tse, N. K. Poon, M. H. Pong, and Y. M. Lai, "General impedance synthesizer using minimal configuration of switching converters," in *Proc. Eur. Conf. Circuit Theory Design*, Cork, Ireland, Aug. 2005, pp. 1–4.

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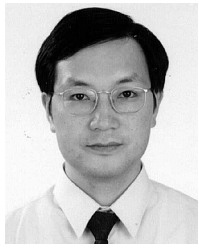

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