<table>
<thead>
<tr>
<th>Title</th>
<th>Effects of NO annealing and GaOxNy interlayer on GaN metal-insulator-semiconductor capacitor with SiO2 gate dielectric</th>
</tr>
</thead>
<tbody>
<tr>
<td>Author(s)</td>
<td>Lin, LM; Lai, PT</td>
</tr>
<tr>
<td>Issued Date</td>
<td>2007</td>
</tr>
<tr>
<td>URL</td>
<td><a href="http://hdl.handle.net/10722/44749">http://hdl.handle.net/10722/44749</a></td>
</tr>
<tr>
<td>Rights</td>
<td>This work is licensed under a Creative Commons Attribution-NonCommercial-NoDerivatives 4.0 International License.; Journal of Electrochemical Society. Copyright © Electrochemical Society, Inc.; Reproduced with permission from Journal of Electrochemical Society, 2007, v. 154 n. 3, p. G58-G62. Copyright 2007, The Electrochemical Society. Permission is not needed if figures and/or tables from one ECS publication will be reused in another forthcoming ECS publication</td>
</tr>
</tbody>
</table>
Effects of NO Annealing and GaO\textsubscript{N} Interlayer on GaN Metal-Insulator-Semiconductor Capacitor with SiO\textsubscript{2} Gate Dielectric

L. M. Lin and P. T. Lai
department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong

As wide-bandgap III-V material, GaN has brought great interest to optical applications: high-efficiency light-emitting diodes, ultra-violet photodetectors, and laser diodes. Based on the advantages of high critical electric field (up to 3 MV/cm) and low thermal generation rate, GaN is also suitable for fabricating high-power and high-temperature devices, such as metal-semiconductor field-effect transistors (MISFETs), metal-insulator-semiconductor field-effect transistor (MISFET), and high-electron-mobility transistors (HEMTs). Although AlGaN/GaN heterostructures have been extensively studied, concern remains regarding the quality of the GaN/MISFET stack, which is a concern for practical applications. In this work, we report on the results of our investigation of NO annealing of GaN/MISFETs, and discuss the effects of NO annealing on the performance of GaN/MISFETs. We found that NO annealing of GaN/MISFETs improves the performance of GaN devices, with a reduction in leakage current and an increase in breakdown field. These improvements are attributed to the formation of a GaO\textsubscript{N} interlayer, which reduces the leakage current and improves the breakdown field. This work provides new insights into the use of NO annealing for improving the performance of GaN devices.

Results and Discussion

SIMS — The SIMS results of the four samples are shown in Fig. 1a-d. The top 5 nm signals are omitted due to the instability of SIMS signals at the sample surface. The curves have been adjusted along the x-axis due to the difference in dielectric thickness, thus providing a clearer comparison. There are similar peak intensities of SiO\textsubscript{2}, SiN, GaN, and GaO\textsubscript{N} for the NS-N2, S-N2, and NS-NO samples in the transition region, while the intensity variations vs depth for the NS-NO sample are gradual with no elements piling up at the interface. It has been reported that the diffusivity (D) of Ga in SiO\textsubscript{2} is about 2 to 6 orders of magnitude higher than those of B, P, Al, Sb in SiO\textsubscript{2}. This high diffusivity makes it possible to implant Ga through a 5000 Å SiO\textsubscript{2} layer into the underlying Si, and then a 30 min annealing at 800°C in N\textsubscript{2}, resulting in significant diffusion of the implanted Ga (D = 2.9 × 10\textsuperscript{-15} cm\textsuperscript{2}s\textsuperscript{-1}) at 800°C. Si can diffuse into GaN to a distance of about 30 Å (D = 1.9 × 10\textsuperscript{-17} cm\textsuperscript{2}s\textsuperscript{-1}, calculated based on the values in Ref. 17). In brief, Ga can diffuse in SiO\textsubscript{2} about 100 times faster than Si in GaN. Therefore, we can conclude that Ga out-diffusion into SiO\textsubscript{2} is the main reason for the formation of SiO\textsubscript{2} on the surface of the GaN layer. The NS-NO sample has characteristics quite different from the
other three: (i) the intensities of SiO$_2$ and SiN gradually decrease from the surface of the dielectric to the interface. (ii) the intensity of GaN gradually increases from the surface to the interface, (iii) the GaO intensity remains high from the surface to the GaN substrate. The above three characteristics clearly demonstrate that a large amount of Ga has outdiffused into the SiO$_2$ dielectric. The reason why the NS-NO sample has much more Ga diffusing into SiO$_2$ compared with the same structure annealed in N$_2$ (NS-N2) should be because the N and O decomposed from NO can have chemical reaction with Ga ions, and thus Ga ions have higher chance to diffuse into the dielectric under the oxidizing ambient. The diffused Ga could damage the lattice structure of SiO$_2$ and produce defects, which trigger large leakage current. However, according to the S-NO sample, many fewer Ga ions diffuse into the SiO$_2$ dielectric. This should be associated with the presence of the GaO$_x$N$_{2-x}$ interlayer because Ga-O and O-N bonds are much more stable than Ga-N bonds under the oxidizing ambient. Moreover, the peak intensity of SiN in the transition layer is even lower than those of the two samples annealed in nitrogen. This is probably related to the fact that the N released from NO can react with the Si near the SiO$_2$/GaN interface to form Si oxynitride, which can block the nitrogen out-diffusion from the GaN substrate more effectively than SiO$_2$.

Positive oxide charges.— Although the SIMS profiles of the NS-NO and S-NO samples are quite different, a common feature is a significant reduction of positive oxide charges induced by the NO annealing. Figure 2a and b shows the high-frequency capacitance-voltage (HF C-V) characteristics of the four samples, and Table I presents the device parameters extracted from the HF C-V curves (average values from six sample points).

The oxide thickness is calculated from the oxide capacitance $C_{ox}$, which is approximated by the maximum value in the accumulation region. After annealing, the films become denser and their thicknesses calculated from $C_{ox}$ are a little bit smaller than the original 40 nm. For the samples NS-N2, S-N2, and S-NO, the interdiffusion mainly happens near the interface (Fig. 1), and thus would not have significant effect on their dielectric constants. As for the sample S-NO, although there is more interdiffusion (Fig. 1), its dielectric constant hardly changes due to little changes in its oxide thickness and $C_{ox}$. The chemical compositions of the four oxide films have little changes after annealing, and therefore, the dielectric constant used for calculation is taken to be that of SiO$_2$ (3.9).

The capacitance at the flatband voltage is as follows

$$C_{fb} = \frac{C_sC_{ox}}{C_s + C_{ox}} \quad [1]$$

where

$$C_s = \varepsilon_{SiO_2}\varepsilon_0/\delta_0 \quad [2]$$

$$L_D = (kT \varepsilon_0\varepsilon_0/4\pi N_D)^{1/2} \quad [3]$$

$\varepsilon_{SiO_2}$ is the dielectric constant of SiO$_2$; $\varepsilon_0$ is the permittivity of free space; $L_D$ is the Debye length; $N_D$ is the actual carrier concentration (1.1 $\times$ 10$^{12}$ cm$^{-3}$) calculated from the measured capacitance; $k$ is the Boltzmann's constant, and $T$ is the measurement temperature.
(298 K). Oxide-charge density $Q_{ox}$ is determined from the shift of flatband voltage

$$V_{fb} = \phi_{Al,GaN} + \frac{Q_{ox}}{C_{ox}}$$

where $\phi_{Al,GaN}$ is the work-function difference between Al and GaN; $\chi$ is the electron affinity of GaN (4.07 eV); $n_i$ is the intrinsic carrier concentration of GaN at room temperature ($2.0 \times 10^{10}$ cm$^{-3}$); $E_g$ is the forbidden bandgap of GaN (3.4 eV). After the NO annealing, the HF C-V curve shifts right, resulting in the lowest oxide-charge density of $1.8 \times 10^{11}$ cm$^{-2}$ for the S-NO sample, followed by the NS-NO sample at $9.5 \times 10^{11}$ cm$^{-2}$, with $Q_{ox}$ of the former more than one order lower than those of the two NO-annealed samples.

During the SiO$_2$ sputtering process, high-energy Ar$^+$ ions bombard the SiO$_2$ target and knock off its molecules. First, the SiO$_2$ molecules have many dangling bonds. Second, these high-energy molecules to be deposited on the GaN wafer can break the GaN bonds, thus creating more dangling bonds. These dangling bonds of the Si or Ga ions should be the reason for the large $Q_{ox}$ of the two NO-annealed samples (NS-N2 and S-N2). However, through the NO annealing for the NS-NO and S-NO samples, sputtered SiO$_2$ can also achieve low oxide-charge density, which should be due to the N and O decomposed from NO forming bonds with the Si or Ga ions.

**Border traps.**—Oxide traps close to the interface which can communicate with the semiconductor are called border traps, whose density ($Q_{bt}$) can be calculated by the following formula

$$Q_{bt} = C_{ox} \Delta V_{FB}/d$$

where $\Delta V_{FB}$ is the hysteresis at flatband between opposite sweeping directions of gate voltage; $d$ is the distance in the oxide above the GaN surface ($\sim 30$ Å). The hysteresis is due to the difference in gate biases at which electrons fill the traps and escape from the traps, or the difference between the capture and emission times of the border traps. In Table 1, it can be seen that after the NO annealing, the border traps are reduced for both the NS-NO and S-NO samples. The NS-NO sample achieved the lowest border-trap density of $1.2 \times 10^{12}$ cm$^{-3}$, which should be related to the decrease of oxide charges after the NO annealing, as mentioned in the previous section.

**Interface traps.**—Interface-trap density is calculated based on the HF C-V curve by using the Terman method. Interface traps follow the change in gate bias and cause a stretch-out of the HF C-V curve. The ideal capacitance is calculated by the following equation

$$C_{ideal} = \frac{C_{ox}}{C_{ox} + C_{int}}$$

where surface capacitance $C_s$ is

$$C_s = \frac{C_{ox}}{\sqrt{2 \left( \frac{\varepsilon_{SiO_2}}{\varepsilon_{Si}} \right) + 1}}$$

with carrier concentration $N_d$ given by

$$N_d = \frac{2}{\varepsilon_{SiO_2} \varepsilon_{Si}} d (1/C_s)^2$$

As Fig. 3 shows, $N_d$ is fitted for the gate voltage ranging from $-15.2$ to $-16.3$ V based on the measured HF C-V curve of the S-N2 sample. Any fitting error is probably due to the nonuniformity of doping concentration or the interface traps. In order to compare the interface quality of different samples, the same $N_d (1.1 \times 10^{17}$ cm$^{-3}$) is used in all calculations. Figure 2a and b shows the difference between the ideal and measured C-V curves. The ideal curves are shifted along the x-axis because the interface-state density is not related to the shift of flatband voltage but only the shape.

**Table 1. Electrical and physical parameters of the GaN MIS capacitors extracted from the high-frequency C-V curves.**

<table>
<thead>
<tr>
<th>Sample</th>
<th>NS-N2</th>
<th>NS-NO</th>
<th>S-N2</th>
<th>S-NO</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{ox}$ (Å)</td>
<td>379</td>
<td>381</td>
<td>380</td>
<td>390</td>
</tr>
<tr>
<td>$V_{fb}$ (V)</td>
<td>$-13.4$</td>
<td>$-1.6$</td>
<td>$-14.4$</td>
<td>$-0.21$</td>
</tr>
<tr>
<td>$Q_{ox}$ ($\times 10^{11}$ cm$^{-2}$)</td>
<td>77.2</td>
<td>9.5</td>
<td>85.0</td>
<td>1.8</td>
</tr>
<tr>
<td>$\phi_{Al,GaN}$ (eV)</td>
<td>120</td>
<td>63</td>
<td>5.9</td>
<td>160</td>
</tr>
<tr>
<td>$E_g = E_V = 0.4$ eV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>($\times 10^{12}$ cm$^{-2}$ eV$^{-1}$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_{bt}$ ($\times 10^{12}$ cm$^{-3}$)</td>
<td>2.6</td>
<td>1.2</td>
<td>2.7</td>
<td>2.0</td>
</tr>
<tr>
<td>$J_{sta}$</td>
<td>65 mA/cm$^2$</td>
<td>1.2 mA/cm$^2$</td>
<td>1.2 mA/cm$^2$</td>
<td>1 mA/cm$^2$</td>
</tr>
<tr>
<td>$E_{bd}$ (MV/cm)</td>
<td>4.9</td>
<td>0.23</td>
<td>0.93</td>
<td>1.79</td>
</tr>
</tbody>
</table>


of the curve. The S-N2 sample has the smallest stretch-out from the ideal curve, indicating least interface traps among all the samples. The interface-trap distribution from 0.1 to 0.8 eV below the conduction band is shown in Fig. 4. Obviously, although the deep-level traps close to the midgap are hardly affected by thermally growing a Ga oxynitride interlayer or annealing in NO, the shallow traps close to the conduction band can be greatly suppressed. However, for the stacked sample annealed in NO, the shallow traps increase, probably due to excessive accumulation of nitrogen at the interface. Specifically, Table I shows that at 0.4 eV below the conduction band edge, the S-N2 sample achieves a low interface-trap density of $5.9 \times 10^{10}$ cm$^{-2}$, followed by the NS-NO sample with $6.3 \times 10^{11}$ cm$^{-2}$, $1.2 \times 10^{12}$ cm$^{-2}$ for the NS-N2 sample, and $1.6 \times 10^{12}$ cm$^{-2}$ for the S-NO sample. The relatively high interface-trap density of the NS-N2 sample should be related to sputtering-induced damage of crystalline structure and large amount of dangling bonds formed at the interface. The S-N2 sample has fewer interface traps, possibly due to the formation of a Ga$_2$O$_3$$_y$$_interlayer through oxidation before the sputtering deposition. This interlayer can work as a buffer layer to reduce the damage of the GaN surface caused by the ensuing sputtering. Moreover, because GaN has higher binding energy than Ga$_2$O$_3$$_y$, the Ga$_2$O$_3$$_y$ interlayer is more resistant to high-energy bombardment, thus forming a more passivated interface. The NO annealing has different effects on the stacked and nonstaked samples. For the nonstaked sample (NS-NO), it presents improved interface quality, which should be due to the N or O decomposed from NO forming bonds with the dangling bonds of the Ga or Si ions at the interface, and thus results in a much smoother interface. However, after the stacked sample is annealed in NO (S-NO), the interface traps increase significantly, implying that too many nitrogen and oxygen atoms (decomposed from NO) piling up at the interface could also introduce traps and deteriorate the performance of devices. It is believed that by reducing the NO concentration in annealing, shortening annealing time, or lowering annealing temperature, the SiO$_2$/Ga$_2$O$_3$/Ga$_2$N system annealed in NO could achieve fewer oxide charges as well as fewer interface traps.

Breakdown field ($E_{br}$) and leakage current.—Figure 5 shows the current vs electric-field ($I$-$E$) characteristic. The electric field is estimated by using the total equivalent thickness calculated from C$_{ox}$, with an error of about 5% due to the interlayer in the samples. The NS-N2 sample has the best $I$-$E$ characteristic and lowest leakage current through the gate dielectric. The $E_{br}$ of the PS-N2 sample is as high as 4.9 MV/cm ($\zeta_{leakage}=65$ $\mu$A/cm$^2$), followed by 1.79 MV/cm ($\zeta_{leakage}=1$ mA/cm$^2$) for the S-NO sample, 0.93 MV/cm ($\zeta_{leakage}=1.2$ mA/cm$^2$) for the S-N2 sample, and 0.23 MV/cm ($\zeta_{leakage}=1.2$ mA/cm$^2$) for the NS-NO sample. After annealing in NO, the leakage current of the NS-NO sample increased significantly due to a large amount of Ga outdiffused into the dielectric. However, for the sample with GaN$_x$$_interlayer$, improved $I$-$E$ characteristic was achieved by annealing in NO (the S-NO sample vs the S-N2 sample), which should be related to reduced oxide charges and defects in the dielectric. Compared with the nonstaked sample NS-N2, the stacked sample S-N2 presents degraded $I$-$E$ characteristic, which should be due to the negative effects of the thermally grown Ga$_2$O$_3$$_y$$_interlayer$. Stacked and nonstaked samples with thicker SiO$_2$ were also fabricated by sputtering. In Fig. 4, the 90-NS-N2 sample means 90 nm SiO$_2$ was deposited on GaN, while the 90-S-N2 sample had 90 nm SiO$_2$ deposited on the same GaN$_x$$_/Ga$_2$N$_2$ structure used earlier. Both samples were annealed in nitrogen at 800°C for 1 h after the SiO$_2$ deposition. When the thickness of the SiO$_2$ dielectric was increased to 90 nm, the negative effects brought by the GaN$_x$$_interlayer$ could be suppressed, resulting in little difference in the breakdown and leakage characteristics between the samples with or without the interlayer.

Figure 6 depicts the energy-band diagram for a GaN MIS capacitor with a positive gate bias, and the interlayer is simplified as Ga$_2$O$_3$ with a smaller conduction-band offset ($\Delta E_c=0.9$ eV) than SiO$_2$ ($\Delta E_c=2.3$ eV). For very thin interlayer, electrons can directly tunnel through it to the Ga$_2$O$_3$/SiO$_2$ interface. For thicker interlayer, the Fowler-Nordheim (FN) tunneling and thermionic emission dominate, and make the electrons jump to the conduction band of the Ga$_2$O$_3$$_interlayer$. Under the same electric field in the SiO$_2$ layer, the electrons at the GaN/SiO$_2$ interface have the highest barrier of 2.3 eV to overcome (Fig. 6a); the electrons after direct
Figure 6. (Color online) Energy-band diagram of gate dielectric on GaN. (a) SiO₂/GaN. (b) SiO₂/Ga₂O₃/GaN. Black balls represent the electrons when Ga₂O₃ is thin to have direct tunneling dominant; gray balls represent the electrons when Ga₂O₃ is thicker to have FN tunneling and thermionic emission dominant.

through the Ga₂O₃ interlayer see a lower barrier of 1.4 eV (solid arrow in Fig. 6b); and the electrons after FN tunneling through the Ga₂O₃ interlayer face the lowest barrier of less than 1.4 eV (dotted arrow in Fig. 6b). Therefore, we can deduce that the thinner the interlayer, the lower the leakage current because the existence of the interlayer lowers the barrier. For the NS-N2 sample, it should have the thinnest interlayer, which makes the dielectric conduction mechanism mainly decided by the SiO₂ layer. The NS-NO sample has Ga ions outdiffused into the SiO₂ layer to produce a thicker interlayer (see Fig. 1), and the resulting lower barrier leads to an increase of leakage current. If the SiO₂ thickness increases, the SiO₂ layer dominates the conduction mechanism, and thus the electrons will find it harder to go through the SiO₂ layer by the thermionic emission or FN tunneling. Therefore, we can conclude that by decreasing the interlayer thickness or increasing the SiO₂ thickness, the leakage current can be effectively reduced, which can be well supported by our experimental results.

Therefore, it is expected that through optimizing the thicknesses of SiO₂ and GaO₃Nₓ, low oxide-charge density, good interface quality, and high breakdown field could be simultaneously achieved.

Conclusions

NO annealing was applied on both SiO₂/GaN and SiO₂/GaO₃Nₓ/GaN MIS structures and turned out to effectively reduce fixed oxide charges by about one order. Nitrogen and oxygen atoms (decomposed from NO) forming bonds with the dangling Si or Ga in the gate dielectric was the main reason for the reduction of positive oxide charges. The NO annealing was also shown to suppress the border traps for the same reason. A very thin GaO₃Nₓ interlayer formed by thermal oxidation can improve the interface quality and achieve a low interface-trap density D_it of 5.9 × 10¹⁰ cm⁻². After the NO annealing, D_it of the SiO₂/GaN capacitor was reduced by about half due to the formation of a GaO₃Nₓ interlayer by the chemical reaction between GaN and NO. The D_it of the SiO₂/GaO₃Nₓ/GaN structure increased after the NO annealing, implying that too many nitrogen and oxygen atoms (decomposed from NO) piling up at the interface could also have deteriorated the interface quality. According to the breakdown field E_BL and leakage current characteristics, SiO₂/GaN capacitor annealed in nitrogen achieved the highest E_BL and lowest leakage current. After the NO annealing, E_BL was degraded for the sample without the GaO₃Nₓ interlayer, but improved for the sample with the interlayer. SIMS results reveal that the opposite phenomenon should be due to the formation of Si₃GaO₇N glass throughout the SiO₂ dielectric in the former, and the breaking of Ga out-diffusion by the interlayer in the latter. After increasing the SiO₂ thickness to 90 nm, the differences in E_BL and leakage characteristics between the stacked and non-stacked samples were negligible. Therefore, it should be possible that interface quality, oxide charges, and E_BL could be all improved through optimizing the SiO₂ thickness and NO-annealing conditions.

Acknowledgment

This work is supported by the RGC of HKSAR, China (project no. HKU 7163/03E). The authors wish to acknowledge K.M. Lau for providing the GaN wafers.

University of Hong Kong assisted in meeting the publication costs of this article.

References