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<tr>
<td><strong>Citation</strong></td>
<td>Journal Of Applied Physics, 2004, v. 96 n. 5, p. 2955-2960</td>
</tr>
<tr>
<td><strong>Issued Date</strong></td>
<td>2004</td>
</tr>
<tr>
<td><strong>URL</strong></td>
<td><a href="http://hdl.handle.net/10722/44721">http://hdl.handle.net/10722/44721</a></td>
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Modeling of temperature sensor built on thin silicon on insulator using advanced carrier-mobility model

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(Received 9 February 2004, Received 27 May 2004)

Based on the minority-carrier exclusion theory, an analytical model is developed to explain the operating principle of temperature sensors fabricated on thin silicon film. The model also takes into account the effects of temperature and carrier concentrations on carrier mobilities. Device simulation is used to verify the proposed model in terms of the carrier-concentration distribution in the minority-exclusion region, exclusion length, and the temperature dependence of the sensor resistance. Results show that the model is applicable for a sensor operating over a wide temperature range, provided that its bias current is not too high. © 2004 American Institute of Physics.

DOI: 10.1063/1.1774266

I. INTRODUCTION

At present, there is a growing demand for electronic devices that can function over a wide temperature range, for example, in the high-temperature compartments of automobiles and aircrafts. High-temperature sensors based on wide-band-gap semiconductors, such as SiC, diamond,

1,2

and fibers,

3

have been investigated in attempts to produce electronic devices that operate reliably even at high temperatures. However, it would still be a long time before wide-band gap semiconductor sensors can become cost-effective. Also, there are numerous problems for fiber sensors to be integrated into a single-chip system. Therefore, the development of high-temperature sensors based on the prevalent silicon and related technologies is still attracting a lot of attention.

Silicon devices are normally only suitable for operating below temperatures of 250°C due to the excessive thermal generation of charge carriers at high temperatures.

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However, by introducing the spreading-resistance structure, the maximum operating temperature ($T_{\text{max}}$) of silicon temperature sensors can be significantly increased. The spreading-resistance temperature (SRT) sensor was introduced in 1982 and commercialized in 1983. This SRT sensor has a vertical structure as shown in Fig. 1(a), and can operate at temperatures from −65°C to 300°C. Later on, Hout and Middelhoek

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raised the $T_{\text{max}}$ of their SRT sensors to 400°C. Moreover, they developed a one-dimensional (1D) minority-carrier exclusion model to explain the principle of spreading resistance and the characteristics of the vertical temperature sensors.

7,8

Recently, the lateral temperature sensor in Fig. 1(b) fabricated by thin-film silicon-on-insulator (SOI) processing

9–11

was studied, and its $T_{\text{max}}$ ranges from 300°C to 450°C. Besides possessing a high working temperature, the lateral temperature sensor is also suitable for integration into a microchip due to its planar structure. The lateral temperature sensor presented here has a low-doping $n$ region with two electrodes forming ohmic contacts to the $n^+$ regions at both ends. When a current flows through the two electrodes, the minority-carrier exclusion effect will occur due to the presence of the high–low junction. Although device simulation can be used to estimate the sensor’s resistance vs temperature characteristics, a simple theoretical model is still needed to facilitate the design of the sensor. This work presents a...
physical model for the SOI temperature sensor, taking into account the minority-carrier exclusion effect, together with the temperature and carrier-concentration effects on carrier mobilities.

II. THEORY

The top view of the temperature sensor is shown in Fig. 2, where w is the width of the sensor and L is the length of the n region, with x as the distance from the n+n junction. Since the electron concentration \( n(x) \) of the n\(^+\) region \((x=0)\) is much higher than that of the n region \((0 \leq x \leq L)\), the hole concentration \( p(x) \) in the n\(^+\) region is much lower than that in the n region. When an electric field is applied along the positive x direction, minority carriers (holes) would flow along the x direction whereas majority carriers (electrons) would move in the opposite direction. Near the n\(^+\)n high–low junction \((x=0)\), holes in the n region are extracted by the electric field at a faster rate than those supplied by the n\(^+\) region due to the difference in hole concentration. Therefore, the hole concentration in the n region near the junction is reduced. If the electric field is strong enough, this hole concentration near the junction will be lowered to nearly zero, even at high temperatures. Then, the electron concentration can be restored to the original doping level due to the condition of space-charge neutrality. This is the essence of the minority-carrier exclusion in the n region next to the n\(^+\)n junction, where thermally generated carriers are effectively removed. Since the extrinsic carriers dominate the electrical conduction, the resistance of the sensor remains the same as that before thermal generation due to high temperatures. This also explains why the \( T_{\text{max}} \) of the sensor can be raised to higher values. Since the minority-carrier concentration does not really go to zero when exclusion occurs, a parameter \( \lambda \) is used to define the extent of exclusion. The exclusion regime is defined to be in effect when the minority-carrier concentration is reduced to \( \lambda N_D \), where \( N_D \) is the doping level of the n region.

The well-known carrier transport equations based on the drift-diffusion model are

\[
J_n = q \mu_n n E + kT \mu_n \nabla n, \quad J_p = q \mu_p p E - kT \mu_p \nabla p, \tag{2}
\]

where \( E \) is the electric field, \( k \) is the Boltzmann constant, \( T \) is the operating temperature, \( J_n \) and \( J_p \) are the electron and hole current densities, and \( \mu_n \) and \( \mu_p \) are the electron and hole mobilities, respectively. Assuming space-charge neutrality is observed in the n region, \( n = N_D + p \) and for uniform doping level, \( \nabla n = \nabla p \).

With \( J_n = J - J_p \) and mobility ratio \( b = \mu_n / \mu_p \), eliminating \( E \) from Eqs. (1) and (2) gives

\[
J_p = \frac{pJ - kT \mu_n (n + p) \nabla p}{bn + p}. \tag{3}
\]

Since the silicon film is very thin, the currents in the y and z directions can be assumed to be zero. In the carrier exclusion region, recombination can be ignored and the generation rate \( G \) is constant. The continuity equation can be written as

\[
\frac{dJ_p}{dx} = qG. \tag{4}
\]

Integrating both sides of Eq. (4) from 0 to \( x \) results in

\[
J_p = J_{p0} + qGx, \tag{5}
\]

where \( J_{p0} \) is the minority-carrier current density injected into the carrier-exclusion region at the n\(^+\)n junction \((x=0)\) and is normally negligible. Substituting Eq. (5) into Eq. (3), using \( n = p + N_D \) (space-charge neutrality) and \( J = I / (w t_{si}) \) \((t_{si} \) is the silicon-film thickness), and neglecting the diffusion term \( \nabla p \) within the exclusion region, we can rewrite Eq. (3) as

\[
p = \frac{qGbN_{Dp}x}{I / w t_{si} - q(b + 1)Gx}. \tag{6}
\]

By setting the condition for the carrier exclusion region as \( p = \lambda N_D \) \((\lambda \) is normally set to 0.1), the exclusion length at the n\(^+\)n junction can be calculated as

\[
x_{\text{ex}} = \frac{\lambda I}{w t_{si} [qGb + \lambda qG(b + 1)]}. \tag{7}
\]

Making use of Eq. (6) and \( n = p + N_D \), the resistivity of sensor is given by

\[
\rho = \frac{1}{nq \mu_n + p \mu_p} = \frac{I - qG(b + 1)w t_{si}x}{q \mu_n N_D I}, \tag{8}
\]

where the material parameters are

\[
G = \frac{1}{\tau N_D + 2n_i}, \quad \mu_n = 55.24 + \frac{1429.23 (\frac{T}{300})^{-2.3} - 55.23}{1 + (\frac{T}{300})^{-3.8} (\frac{n + p}{1.072 \times 10^{17}})^{0.75}}, \tag{9}
\]

In Fig. 2, the lateral temperature sensor on SOI. The J is the current density applied to the sensor, w is the width of the sensor, L is the length of the sensor (n region), and x is the distance from the n\(^+\)n junction. In this work, w is set to be 100 \( \mu \)m whereas L is set to be 10 \( \mu \)m.
are 4.73 temperature coefficients for the energy band gap $T$. The excess-carrier lifetime $\tau$ of the temperature sensor at 300° C for bias currents of 0.1 mA, 1 mA, 10 mA, and 0.1 mA. The dotted line $\lambda N_D$ defines the threshold level for minority-carrier exclusion. In this work, the film doping level $N_D$ is $1 \times 10^{15}$ cm$^{-3}$. The threshold level is defined to be one-tenth of the doping level ($\lambda = 0.1$). When the minority-carrier (hole) concentration falls below this level, the minority-carrier exclusion occurs.

$$\mu_p = 49.7 + \frac{\text{479.37} \left( \frac{T}{300} \right)^{-2.2} - 49.7}{1 + \left( \frac{T}{300} \right)^{-3.7} \left( \frac{n + p}{1.606 \times 10^{17}} \right)^{0.7}}, \quad (10)$$

and

$$n_1 = \sqrt{N_c N_v e^{-E_g/2kT}},$$

$$E_g = E_g(300 \text{ K}) + \alpha \left[ \frac{300^2}{300 + \alpha} - \frac{T^2}{T + \beta} \right],$$

$$N_c = N_c(300 \text{ K}) \left( \frac{T}{300} \right)^{3/2},$$

$$N_v = N_v(300 \text{ K}) \left( \frac{T}{300} \right)^{3/2}.$$  

The excess-carrier lifetime $\tau$ is taken to be 0.1 $\mu$s and the temperature coefficients for the energy band gap ($\alpha$ and $\beta$) are $4.73 \times 10^{-4}$ eV/K and 636 K, respectively. Finally, the resistance of the sensor can be calculated as

$$R = \int_0^L \frac{p(x)}{w} t_{si} dx = \int_0^L \frac{I - qG(b + 1)w_{si}x}{w_{si}q\mu_n N_D} dx. \quad (11)$$

III. RESULTS AND DISCUSSIONS

With $L$ of 10 $\mu$m, $w$ of 100 $\mu$m, and $t_{si}$ of 0.1 $\mu$m, the distribution of minority-carrier concentration along the $x$ direction under different bias currents can be calculated from Eq. (6). The hole distributions in a SOI device at 300° C for different bias currents are plotted in Fig. 3. The dotted line defines the threshold level for minority-carrier exclusion, which occurs in the region where the hole concentration falls below this level. In this region, the electron concentration drops back to nearly the same as the original doping level because of space-charge neutrality. If the carrier exclusion region is longer, the device needs a higher temperature to produce more electron and hole pairs in order to switch to intrinsic conduction, implying a higher $T_{\text{max}}$. From Fig. 3, it can easily be seen that when the current is larger, the exclusion length is larger and hence $T_{\text{max}}$ is higher. When the bias current is at 0.1 $\mu$A, the hole concentration is higher than the threshold level within the entire $n$ region. This means that carrier exclusion does not occur if the bias current is too small, and $T_{\text{max}}$ at this bias current should be far below 300° C. When current is increased to 1 $\mu$A, carrier exclusion starts to occur near the $n^+n$ junction up to a distance of 2.5 $\mu$m. $T_{\text{max}}$ will be a little higher than that for 0.1 $\mu$A, but still much lower than 300° C. When the bias current is larger than 10 $\mu$A, carrier exclusion covers the entire $n$ region, and $T_{\text{max}}$ at this high current bias will be higher than 300° C.

Equation (7) evaluates the temperature dependence of the exclusion length under different bias currents as illustrated in Fig. 4. This is another way to display the relation between the carrier exclusion effect and $T_{\text{max}}$. The temperature at which the carrier exclusion length (solid lines) intersects the length of the sensor (dotted line) represents the exact temperature that the carrier exclusion region covers the entire $n$ region of the sensor and is approximately equal to the $T_{\text{max}}$ of the sensor at a given bias current. For instance, the intersection point of 0.1 $\mu$A is 210° C. When the temperature is below 210° C, say 200° C, the carrier exclusion length is larger than the length of the sensor. This means that the device needs more thermally generated electron-hole pairs to overwhelm the extrinsic carriers, and thus $T_{\text{max}}$ should be higher than 200° C. For temperature above 210° C, say 220° C, the carrier exclusion length is smaller than the length of the sensor, implying that part of the device has a lot of excess carriers. Therefore, $T_{\text{max}}$ should be lower than 220° C at a current bias of 0.1 $\mu$A. Similar trends are also found for the other three bias currents, and $T_{\text{max}}$ at different bias currents calculated by this method are as shown in Table I.

The integrand in Eq. (11) depends not only on the distance $x$ but also on the carrier mobilities $\mu_n$ and $\mu_p$, which are in turn functions of $p(x)$ in Eq. (6). Due to this complexity, the sensor’s resistance has to be calculated by numerical

![FIG. 3. Calculated minority-carrier concentration profiles across the temperature sensor at 300° C for bias currents of 0.1 $\mu$A, 1 $\mu$A, 10 $\mu$A, and 0.1 mA. The dotted line $\lambda N_D$ defines the threshold level for minority-carrier exclusion. In this work, the film doping level $N_D$ is $1 \times 10^{15}$ cm$^{-3}$. The threshold level is defined to be one-tenth of the doping level ($\lambda = 0.1$). When the minority-carrier (hole) concentration falls below this level, the minority-carrier exclusion occurs.](image1)

![FIG. 4. Calculated carrier exclusion length for the temperature sensor with bias currents of 0.1 $\mu$A, 1 $\mu$A, 10 $\mu$A, and 0.1 mA. The $N_D$ is $1 \times 10^{15}$ cm$^{-3}$. The dotted line shows the length of the sensor.](image2)
method, which consumes much computer time and sometimes could have convergence problems. In the following description, different methods are proposed to simplify the calculation while maintaining acceptable accuracy.

A. Case 1

Since the intrinsic carrier concentrations are relatively low for temperatures not far beyond $T_{\text{max}}$, the charge-dependent term $n+p$ in the mobility formula can be approximated by $N_D$, and thus $\mu_n$ and $\mu_p$ can be considered to be constant throughout the $n$ region (this will be later supported by Case 5). As a result, the resistance of the sensor in Eq. (11) can be analytically calculated as

$$R = \frac{L}{q\mu_nN_D^\text{wt}_l} - \frac{G(b+1)L^2}{2\mu_nN_DI}. \quad (12)$$

The first term is the well-known formula for a simple diffused resistor, and it increases with temperature due to variation in $\mu_n$. In the second term, $G$ accounts for the thermal generation of carriers, whereas $I$ produces the carrier exclusion effect. The combined effects on the characteristics of resistance vs temperature are as plotted in Fig. 5. The same characteristics simulated using the 2D device simulator PISCES are also included for comparison. Figure 5 shows that higher current induces stronger carrier exclusion effect, thus resulting in higher $T_{\text{max}}$. The $T_{\text{max}}$ calculated and simulated at different bias currents are also included in Table I for comparison. When the bias current is smaller than 0.1 mA, there is little difference among the $T_{\text{max}}$ calculated by the three methods. However, large discrepancies exist when the bias current is over 0.1 mA. The reason is that when the bias current is large, the minority-carrier injection current density $J_{\text{gr}}$ in Eq. (5) can no longer be ignored. This carrier injection can increase the carrier concentrations in the $n$ region and thus lower its resistance as shown in Fig. 5.

B. Case 2

The carrier mobilities calculated by Eqs. (9) and (10) show that when the temperature increases from 30°C to 600°C, their ratio $b$ only changes from 2.8 to 2.6. Therefore, $b$ can be further simplified as a constant and take on its room-temperature value of 2.8. Since $\mu_n$ and $\mu_p$ are considered as constants throughout the $n$ region, Eq. (12) is still applicable for this case. The new characteristics of resistance vs temperature are as shown in Fig. 6, illustrating that the mobility ratio hardly affects the resistance.

C. Case 3

Owing to the approximations used in the model derivation, there exists a singularity ($x_0$) in the hole-concentration distribution described by Eq. (6). When $x=x_0=I/[q(b+1)GwL_{\text{sil}}]$, $p$ will approach infinity. Since $p$ is negative for $x>x_0$, the integration range in Eq. (11) has to be adjusted from 0 to $x_{\text{up}}$, and Eq. (12) becomes

$$R = \frac{x_{\text{up}}}{q\mu_pN_D^\text{wt}_l} - \frac{G(b+1)x_{\text{up}}^2}{2\mu_pN_D^2I}, \quad (13)$$

where $x_{\text{up}} = \min(L,x_0)$. As can be observed in Fig. 7, there is a little effect of $x_0$ on the resistance for temperatures below $T_{\text{max}}$. This also confirms that the region from 0 to $x_0$ governs the resistance of the sensor when carrier exclusion effect occurs. For temperatures beyond $T_{\text{max}}$, Eq. (13) gives a more realistic resistance-temperature characteristics than Eq. (12) by removing all the negative carrier concentrations.

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**TABLE I.** $T_{\text{max}}$ calculated by three methods for the temperature sensor at different bias currents

<table>
<thead>
<tr>
<th>Bias currents</th>
<th>$T_{\text{max}}^{(1)}$($^\circ\text{C}$) from Fig. 4</th>
<th>$T_{\text{max}}^{(2)}$($^\circ\text{C}$) from Eq. (8)</th>
<th>$T_{\text{max}}^{(3)}$($^\circ\text{C}$) from PISCES</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1 $\mu$A</td>
<td>210</td>
<td>210</td>
<td>230</td>
</tr>
<tr>
<td>1 $\mu$A</td>
<td>260</td>
<td>260</td>
<td>230</td>
</tr>
<tr>
<td>10 $\mu$A</td>
<td>350</td>
<td>360</td>
<td>330</td>
</tr>
<tr>
<td>0.1 mA</td>
<td>460</td>
<td>510</td>
<td>430</td>
</tr>
</tbody>
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**FIG. 5.** Resistance-temperature curves for the temperature sensor with bias currents of 0.1 $\mu$A, 1 $\mu$A, 10 $\mu$A, and 0.1 mA. The $N_D$ is $1 \times 10^{15}$ cm$^{-3}$. Solid symbols show the results calculated by the 2D device simulator PISCES. Hollow symbols are the results calculated by the 2D device simulator PISCES.

**FIG. 6.** Effects of temperature-sensitive carrier-mobility ratio ($b=\mu_p/\mu_n$) on sensor resistance at bias currents of 0.1 $\mu$A, 1 $\mu$A, 10 $\mu$A, and 0.1 mA. The $N_D$ is $1 \times 10^{15}$ cm$^{-3}$. Dotted lines show the results with the effect of temperature on $b$. Solid symbols show the results without the effect of temperature on $b$ ($b$ is set at its room-temperature value of 2.8).
D. Case 4

As mentioned in Case 3, $p$ in Eq. (6) rises rapidly to a very large value before becoming negative. But in reality, $p$ cannot be higher than its equilibrium value $p_0$, which is defined as

$$p_0 = n_0^2/n_0 = \frac{n_0^2}{\frac{1}{2}[N_D + \sqrt{N_D^2 + 4n_0^2}]}$$  \hspace{1cm} (14)$$

where $n_0$ is the equilibrium electron concentration. If $x_{p0}$ is defined as the location where $p$ in Eq. (6) increases to $p_0$, then

$$x_{p0} = \frac{p_0d}{(qGbn_D + qG(b + 1)p_0)wt_{si}}$$  \hspace{1cm} (15)$$

For $x$ larger than $x_{p0}$, $p$ in Eq. (6) is larger than $p_0$ and so is set equal to $p_0$. The resistivity determined by Eq. (8) for this region becomes

$$\rho_0 = \frac{b}{\mu_n N_d^2 + \mu_n(1 + b)p_0}$$  \hspace{1cm} (16)$$

With $x_{max} = \min(L, x_{p0})$, Eq. (11) becomes

$$R = \frac{1}{w t_{si}} \left[ \int_0^{x_{max}} \rho(x)dx + \int_{x_{max}}^L \rho_0 dx \right] = \frac{x_{max}}{\mu_n N_d^2 w t_{si}} - \frac{G(b + 1)x_{max}^2}{2\mu_n N_d} \frac{b}{w t_{si} N_d + \mu_n(1 + b)p_0}
\times(L - x_{max}).$$  \hspace{1cm} (17)$$

From Fig. 8, a big difference is found when the bias current is low (e.g., for $0.1 \mu A$, $T_{max}$ is $20^\circ$C higher when considering $x_{p0}$). For a lower bias current, since the carrier exclusion effect is weak, the hole concentration at high temperature given by Eq. (6) is much higher than $p_0$ for most of the integration range, given that $x_{p0}$ is much smaller than $L$. Hence, the results calculated by Eq. (12) differ from those calculated by Eq. (17) due to the significance of the last term in Eq. (17). For higher bias currents in the range of $1 \mu A$ to $0.1 mA$, the two methods give similar $T_{max}$, but different resistance values only at high temperatures beyond $T_{max}$. This is because when the bias current is large, the carrier exclusion effect is strong and the hole concentration at high temperature is normally lower than the equilibrium level $p_0$ over most of the integration range from 0 to $L$. Therefore, $x_{p0}$ is normally larger than $L$ or very close to $L$, and hence there is no big difference between Eq. (12) and Eq. (17).

E. Case 5

With the inclusion of the effect of carrier concentrations on carrier mobilities, an iteration method is required to solve for $p$ in Eq. (6), $p_{b0}$, $p_{p0}$, and then $R$ in Eq. (17). In this calculation, the initial guesses of $b$ and $R$ are 2.8 and 100 k$\Omega$, respectively, and the maximum errors of $b$ and $R$ are both set at 1%. Figure 9 shows that the carrier-concentration dependence of carrier mobilities has little effect on the sensor resistance for all bias currents. The reason is that when the temperature is lower than $T_{max}$, the carrier exclusion effect dominates. The hole concentration is negligible and the electron concentration is nearly equal to the doping level over the entire n region. This leads to the small effect of the

![Fig. 7. Effects of carrier-concentration singularity on sensor resistance at bias currents of 0.1 $\mu A$, 1 $\mu A$, 10 $\mu A$, and 0.1 mA. The $N_D$ is 1 $\times 10^{15}$ cm$^{-3}$. Dotted lines are the results with negative values in the carrier-concentration profile inside the sensor, whereas solid lines show the results with negative concentrations removed.](image1)

![Fig. 8. Effects of equilibrium carrier concentrations on sensor resistance at bias currents of 0.1 $\mu A$, 1 $\mu A$, 10 $\mu A$, and 0.1 mA. The $N_D$ is 1 $\times 10^{15}$ cm$^{-3}$. Solid lines show the results with the equilibrium values in the carrier-concentration profile inside the sensor, whereas dotted lines are the results without the equilibrium concentrations.](image2)

![Fig. 9. Effects of carrier concentration-sensitive mobilities on sensor resistance at bias currents of 0.1 $\mu A$, 1 $\mu A$, 10 $\mu A$, and 0.1 mA. The $N_D$ is 1 $\times 10^{15}$ cm$^{-3}$. Solid lines are the results with carrier mobilities dependent on carrier concentrations, whereas dotted lines show the results without this dependence.](image3)
carrier concentrations on the carrier mobilities. On the other hand, when the temperature is higher than $T_{\text{max}}$, the effect of temperature overwhelms the effect of the carrier concentrations on the carrier mobilities, thus dominating the temperature dependence of the sensor resistance.

In summary, Eq. (12) is a simple and reasonably accurate formula for describing the sensor resistance for temperatures below $T_{\text{max}}$, which covers the normal operating temperature range of the sensor.

IV. CONCLUSION

An analytical device model is developed to explain the characteristics of the temperature sensor built on thin-film SOI. This model shows that at higher bias currents, the device has higher maximum operating temperature due to larger minority-carrier exclusion length. Compared with the results from the device simulator PISCES, this model is accurate for bias currents below 0.1 mA. However, for larger bias currents, $T_{\text{max}}$ calculated by the proposed model is larger than that simulated by PISCES due to the fact that high-current carrier injection at the $n^+n$ junction is neglected. When the bias current is low, a two-region model is proposed to improve the resistance model, and reasonable results are achieved. The carrier-mobility ratio and carrier-mobility dependence on carrier concentrations are found to have little effects on the device resistance for temperatures below $T_{\text{max}}$.

In summary, the device model presented here can be used to help understand the principle of the minority-carrier exclusion effect and guide the design of temperature sensors built on thin silicon film for high-temperature applications.

ACKNOWLEDGMENTS

This work is financially supported by the RGC grant of Hong Kong and the CRCG grant of the University of Hong Kong.