Interface Trap Generation by FN Injection under Dynamic Oxide Field Stress

T. P. Chen, Stella Li, S. Fung, and K. F. Lo

Abstract— Interface trap generation under dynamic (bipolar and unipolar) and dc oxide field stress has been investigated with the charge pumping technique. It is observed that regardless of stress type, whether dc or dynamic (bipolar or unipolar), and the polarity of stress voltage, interface trap generation starts to occur at the voltage at which Fowler–Nordheim (FN) tunneling through the oxide starts to build up. For positive voltage, interface trap generation is attributed to the recombination of trapped holes with electrons and to the bond breaking by the hydrogen (H and H^+) released during stressing. For negative voltage, in addition to these two mechanisms, the bond breaking by energetic electrons may also contribute to interface trap generation. The frequency dependence of interface trap generation is also investigated. Interface trap generation is independent of stressing frequency for unipolar stress but it shows a frequency dependence for bipolar stress.

Index Terms— Integrated circuit reliability, MOS devices, MOSFET's, semiconductor device reliability, silicon materials/devices.

I. INTRODUCTION

VERY large scale integration (VLSI) technology requires smaller devices with thinner silicon dioxide films. Thin silicon dioxide films tend to be used at higher electric fields, since voltage scaling is not well advanced. It is well known that the high electric field across the oxide leads to trap generation both in the bulk of the oxide and at the oxide/substrate interface [1]–[8]. The trap generation in oxide and at the interface has been investigated intensively. However, most high field stress have been performed with dc voltage. Even for interface trap generation under dc oxide field stress, some controversial results have been reported. For example, in [1], [8], it was reported that interface trap generation doesn't depend on the stress voltage polarity, but in [7], it was observed that interface trap density generated by negative voltage stress is much higher than that by positive voltage stress. On the other hand, there has been relatively little information concerning trap generation at the interface under dynamic stress. Interface trap generation under dynamic stress conditions has been investigated in previous studies [15]–[18]. Rosenbaum *et al.* [15] observed that interface trap generation under bipolar stress is larger than that under unipolar stress. They also observed that, interface trap density saturates quickly under

unipolar stress, but it continues to increase under bipolar stress. However, Chaparala *et al.* [17] observed a continuous increase in interface trap density with stress time for unipolar stress. Interface trap generation under bipolar stress has been found to increase first and then decrease with stress frequency with a maximum at around 2 kHz [16]. It is believed [16] that interface traps are generated by the recombination of trapped holes with electrons. However, the electrons flowing through the oxides may also break the bonds and generate traps at the interface [6].

In this study, interface trap generation under the dc and dynamic (bipolar and unipolar) oxide field stress has been investigated with the charge pumping technique. It is observed that, regardless of stress type, whether dc or dynamic (unipolar or bipolar), or polarity of the stress voltage, interface trap generation starts to occur at the voltage at which the Fowler–Nordheim (FN) tunneling of electrons into the oxide starts to build up. This gives a direct evidence for the relationship between interface trap generation and FN tunneling. The mechanisms for interface trap generation, including the recombination of trapped holes with electrons, the bond breaking by energetic electrons, and the bond breaking by the hydrogen (H and H^+) released during stressing are discussed. On the other hand, the frequency dependence of interface trap generation for both bipolar and unipolar stresses is also investigated.

II. EXPERIMENTAL

The devices used in these experiments were polysilicon gate n-channel MOSFET's fabricated on p-substrates in a manufacturing facility with a 0.5-μm CMOS technology. The gate length and width are 0.5 μm and 50 μm, respectively, the junction depth of both the source and the drain is 0.2 μm, and the thickness of the gate oxide is 110 Å.

During the pulsed unipolar and bipolar, and dc stresses, the stress voltage was applied to the gate electrode while the substrate, drain and source were grounded. In the following descriptions, we use V_s to represent the amplitude of the stress voltage. A square voltage waveform was used for both the bipolar and unipolar stresses. For bipolar stress, the stress voltage was a symmetric bipolar square wave with $+V_s$ during positive half-cycle and $-V_s$ during the negative half-cycle. Unipolar stress was divided into two subgroups: the positive unipolar stress (i.e., the voltage was maintained at $+V_s$ during one half-cycle and at 0 V during the next half-cycle.) and the negative unipolar stress (i.e., the voltage was maintained at $-V_s$ during one half-cycle and at 0 V during the next half-cycle.). The dc stress was also divided into positive
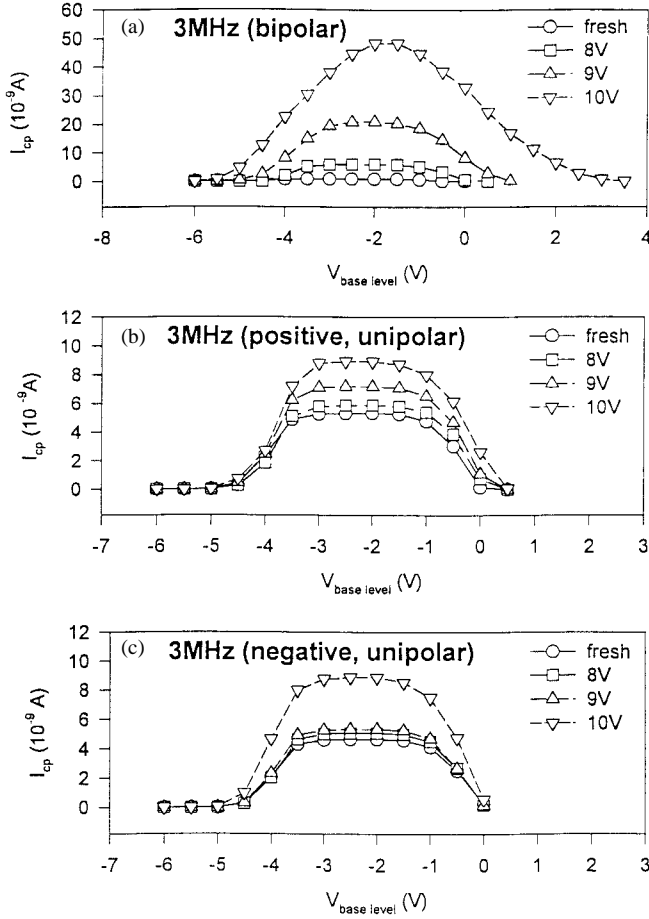
Fig. 1.　Evolution of charge pumping current after bipolar or positive and negative unipolar stresses at the frequency of 3 MHz. At each voltage amplitude V_s (= 8, 9 and 10 V), a stress of 20 min was performed on the same devices, and then the charge pumping current was measured. (a) Bipolar, (b) positive unipolar, and (c) negative unipolar.
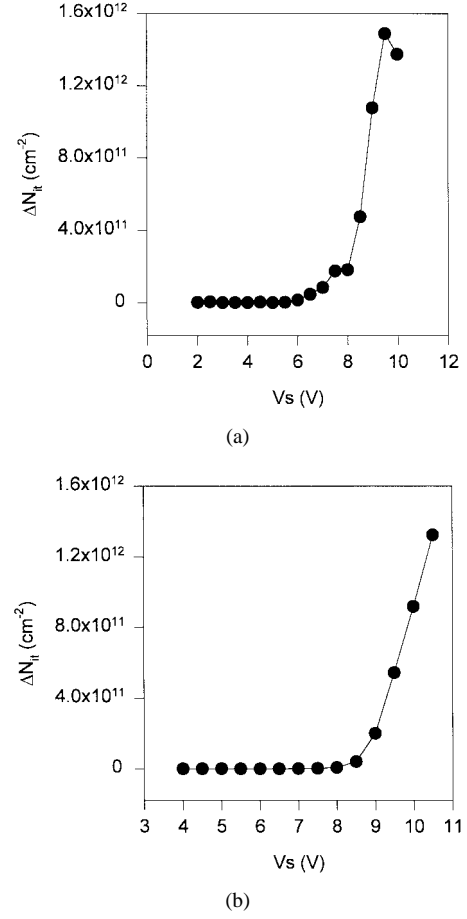

Fig. 2.　Interface trap generation by (a) bipolar stress at the frequency of 3 MHz and by (b) negative dc stress; voltage amplitude V_s was increased with a step of 0.5 V, and at each V_s a stress of 20 min was performed on the same devices. $\Delta N_{it} = N_{it}(V_s) - N_{it}(V_s - 0.5 \text{ V})$.

and negative voltage stresses. For the measurement of gate current I_g, the substrate, drain and source were grounded. I_g was measured as the gate voltage V_g was swept from 0 V to a positive or negative voltage with a sufficiently low sweep rate. The gate current measurement was performed on fresh devices. Charge pumping measurements were carried out with a Tektronix AFG 5101 programmable function generator and a Keithley programmable electrometer. The measurement frequency was 300 kHz, the amplitude 4 V, and source and drain were grounded. The interface trap density for fresh devices obtained from the charge pumping measurements was of the order of 10^{10} cm^{-2}. All the stresses and measurements were performed at room temperature.

III. RESULTS AND DISCUSSION

Devices were stressed by applying dc or dynamic (bipolar and unipolar) voltages with different amplitude V_s to their gates. V_s was normally increased from 2 to 11 V in steps of 0.5 V. At each V_s, a device was stressed for 20 min. The charge pumping measurements were carried out before and after stress at each V_s. As an example, the evolution of charge pumping current after bipolar or positive and negative unipolar stresses at the frequency of 3 MHz is shown in Fig. 1. Note

that the bipolar and positive and negative unipolar stresses were performed on different devices. A 20-minute stress was carried out at each stress voltage V_s (= 8, 9, and 10 V), and then the charge pumping current was measured. The charge pumping current was observed to start to increase at $V_s \approx 6$ V for bipolar, positive unipolar and positive dc stresses and at $V_s \approx 8$ V for negative unipolar and negative dc stresses. These observations are independent of the frequency of the bipolar and unipolar pulses. As the measurement frequency is 300 kHz, the near-interface oxide traps do not respond fast enough and thus only the interface traps contribute to the charge pumping current [9]. Thus the change of charge pumping current can be translated to the change of interface trap density (N_{it}). As the device under test was stressed at each stress voltage V_s (V_s was increased in a step of 0.5 V) for 20 min, $\Delta N_{it}(V_s) = N_{it}(V_s) - N_{it}(V_s - 0.5 \text{ V})$ represents the increase of interface trap density caused by each stress at V_s. As an example, the change of the interface trap density after the bipolar stress at a frequency of 3 MHz or negative dc stress at each V_s, i.e., $\Delta N_{it}(V_s) = N_{it}(V_s) - N_{it}(V_s - 0.5$ V) is shown in Fig. 2. It is evident in Fig. 2 that interface trap density starts to increase at about 6 V and at about 8 V for bipolar and negative dc stresses, respectively.
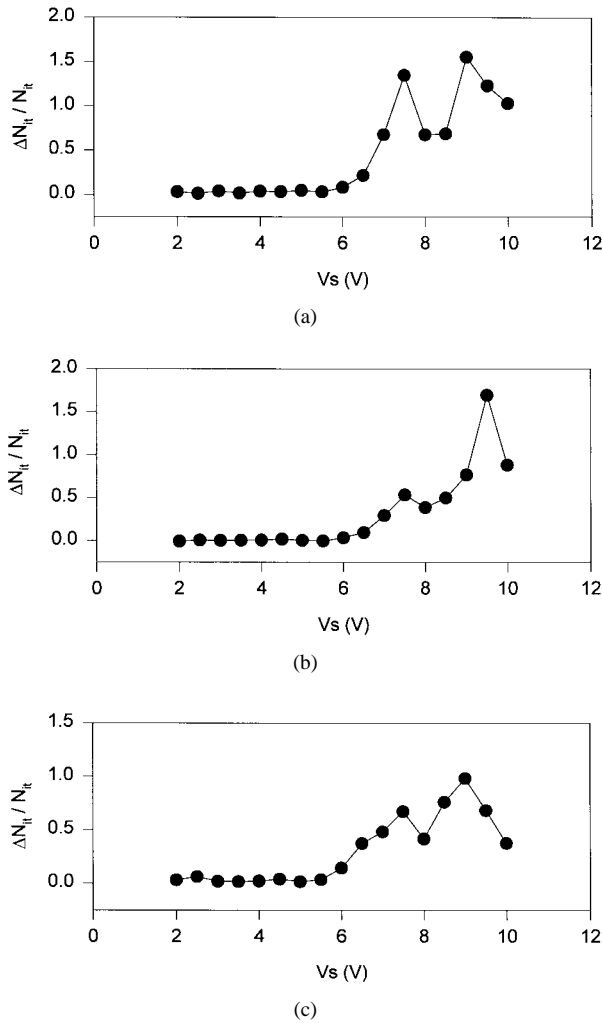
(a)

(b)

(c)

Fig. 3. $\Delta N_{it}/N_{it}$ as a function of V_s for bipolar stress at the frequencies of (a) 300 Hz, (b) 30 kHz, and (c) 3 MHz. Voltage amplitude V_s was increased with a step of 0.5 V, and at each V_s a stress of 20 min was performed on the same devices. N_{it} represents the interface trap density before the stress at each V_s, i.e., $N_{it}(V_s - 0.5$ V), and $\Delta N_{it} = N_{it}(V_s) - N_{it}(V_s - 0.5$ V).

To show the fine features of ΔN_{it} as a function of V_s clearly, $\Delta N_{it}(V_s)$ is normalized to N_{it} at the voltage of $(V_s - 0.5$ V), i.e., $\Delta N_{it}(V_s)/N_{it}(V_s - 0.5$ V) , or $\Delta N_{it}/N_{it}$ for simplicity. As discussed below, the plotting of $\Delta N_{it}/N_{it}$ helps to distinguish the interface trap generation by positive voltage during the positive half-cycles from that by negative voltage during the negative half-cycles in bipolar stress. $\Delta N_{it}(V_s)$ may become saturated or decrease as V_s (and stress time) increases further. The saturation or decrease of ΔN_{it} is possibly due to the factor that injected current decreases because of decrease of cathode field due to electron trapping in the oxide. On the other hand, N_{it} increases continuously with V_s. Therefore, the plotting of $\Delta N_{it}/N_{it}$ will create peak structures. As shown below, both dc and unipolar stresses have only one peak in the plots of $\Delta N_{it}/N_{it}$, but bipolar stress has two peaks. The two peaks are due to the interface trap generation during the positive and negative half-cycles in the bipolar stress. Fig. 3 shows $\Delta N_{it}/N_{it}$ as a function of V_s for bipolar stress with different frequencies. As can be seen in Fig. 3, for all the frequencies, $\Delta N_{it}/N_{it}$ starts to increase at $V_s \approx 6$ V and
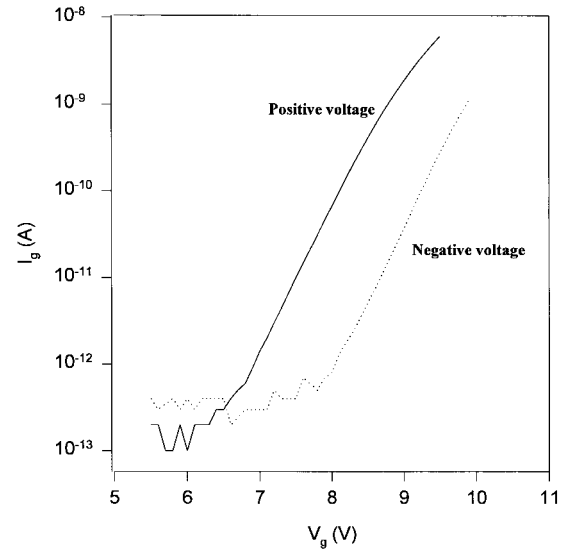

Fig. 4.   Gate current I_g as a function of gate voltage V_g. The measurement was carried out on fresh devices.

reaches a maximum at $V_s \approx 7.5$ V. Then it drops down but starts to increase again at $V_s \approx 8$ V. $\Delta N_{it}/N_{it}$ increases with V_s continuously until it reaches another maximum, and then it drops down again. Such a picture indicates that there are two processes in two different ranges of V_s involved in the interface trap generation during bipolar stress. As shown below, this is related to FN injection at positive and negative voltages during positive and negative half-cycles, respectively.

For the same magnitude of applied voltage, the electric field strength in the oxide film is different for positive and negative voltages. The electric field in the oxide film E_{ox} is evaluated as follows. For inversion, E_{ox} is obtained by taking into account the flat-band voltage V_{FB} and the substrate potential $2\phi_F$($q\phi_F$ is the energy difference between the midgap position and the Fermi level in the bulk of the substrate) as [7]

$$E_{ox} = (V_g - V_{FB} - 2\phi_F)/t_{ox} \qquad (1)$$

where V_g is the voltage applied to the gate and t_{ox} is the thickness of the oxide film. For accumulation, E_{ox} is defined as [7]

$$E_{ox} = (V_g - V_{FB} - 0.55 + \phi_F)/t_{ox}. \qquad (2)$$

As the substrate is p type, positive voltage corresponds to the inversion while the negative voltage corresponds the accumulation. The values of V_{FB} and ϕ_F are −1.36 and 0.48 V, respectively, for the 110-Å oxide film grown on the p-type substrate. If we take an electric field of 6 MV/cm across the oxide film as the criterion of the start of FN tunneling [7], using (1) and (2) we can estimate that the FN tunneling current starts to build up at $V_g = 6.2$ V for positive gate voltage and at $V_g = -7.9$ V for negative gate voltage. Fig. 4 shows the gate current I_g as a function of the gate voltage V_g for positive and negative voltages for a fresh device. It is shown that the FN tunneling current starts to build up at around 6 V for positive voltage and at around −8 V for negative voltage. This agrees with the estimate given above.
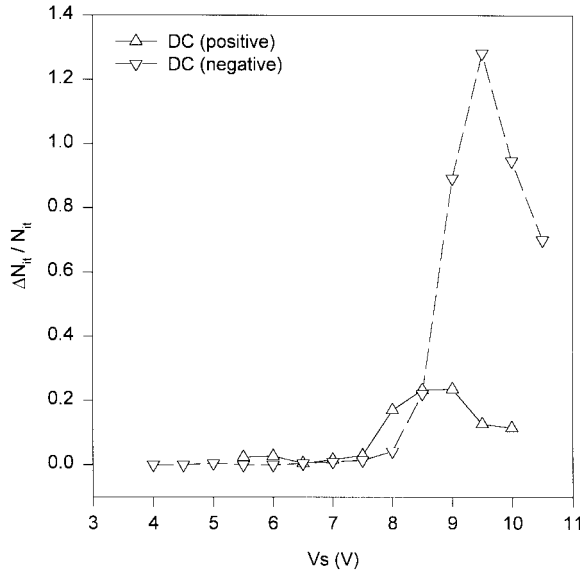
Fig. 5. $\Delta N_{it}/N_{it}$ as a function of V_s for positive and negative dc stresses. The stress procedures and time are the same as those in Fig. 3.
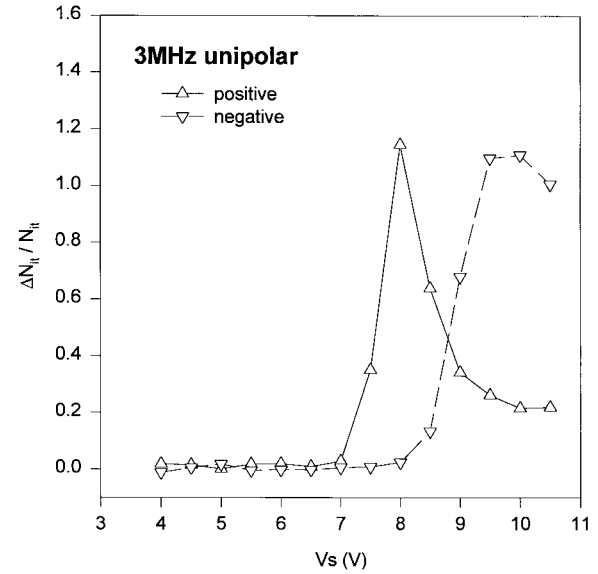

Fig. 6. $\Delta N_{it}/N_{it}$ as a function of V_s for positive and negative unipolar stresses. The stress procedures and time are the same as those in Fig. 3.

For bipolar stress, a positive voltage $+V_s$ is applied to the gate during one half-cycle (the positive half-cycle) but a negative voltage $-V_s$ is applied to the gate during another half-cycle (the negative half-cycle). From the above discussions, it is clear that, for V_s less than ~ 6 V, no FN tunneling takes place during either the positive or the negative half-cycles; for V_s larger than ~ 6 V but less than ~ 8 V FN tunneling can take place during only the positive half-cycles; and for V_s larger than ~ 8 V FN tunneling can take place during both the positive and negative half-cycles.

Comparing Fig. 3 with Fig. 4, we find that, the first start of the increase of $\Delta N_{it}/N_{it}$ at $V_s \approx 6$ V corresponds to the start of FN tunneling at about 6 V for positive voltage, while the second start at $V_s \approx 8$ V corresponds to the start of FN tunneling at about -8 V for negative voltage. Therefore, the features of $\Delta N_{it}/N_{it}$ versus V_s shown in Fig. 3 are related to FN injection during positive and negative half-cycles. In other words, for bipolar stress, for V_s less than ~ 6 V, there is no FN injection taking place during both positive and negative half-cycles and thus there is no interface trap generation; for V_s larger than ~ 6 V but less than ~ 8 V, interface traps are generated by FN injection during only positive half-cycles; for V_s larger than ~ 8 V, interface traps are generated during both positive and negative half-cycles as FN injection can take place during both the half-cycles. It is evident from Fig. 3 that, in both the ranges of ~ 6 V $< V_s < \sim 8$ V and of $V_s > \sim 8$ V, $\Delta N_{it}/N_{it}$ first increases with V_s but decreases after it reaches a maximum. Such a feature can also be observed in positive and negative dc and unipolar stresses, as shown below.

In contrast to bipolar stress under which interface trap may be generated by both positive and negative voltages, dc and unipolar stresses may lead to interface trap generation by only one polarity of voltage, i.e., by either positive voltage or negative voltage. In other words, for dc and unipolar stresses, only one feature corresponding to FN injection under either positive voltage or negative voltage should be observed in

the plots of $\Delta N_{it}/N_{it}$ versus V_s. This has been confirmed by experiment. Fig. 5 shows $\Delta N_{it}/N_{it}$ as a function of V_s for positive and negative dc stresses. It is again observed that, $\Delta N_{it}/N_{it}$ starts to increase at the V_s values at which the FN tunneling current starts to build up, and it increases with increasing V_s until it reaches a maximum and then it decreases. For positive and negative unipolar stresses, it is also observed that the start of interface trap generation corresponds to the start of the building up of FN tunneling current and that $\Delta N_{it}/N_{it}$ increases with V_s first and then decreases after it reaches a maximum. Fig. 6 shows the change of $\Delta N_{it}/N_{it}$ with V_s for positive and negative unipolar stresses. Note that, the thickness of the gate oxide may be slightly different for different devices and thus the voltage at which FN tunneling current start to build up may be slightly different, and this will have some influence on the plots of $\Delta N_{it}/N_{it}$ versus V_s.

The above observation that interface trap generation starts at the voltage at which FN tunneling current start to build up agrees with the result reported in [6]. In [6], the interface trap generation data with different fluence through the oxide can be extrapolated to a voltage at which the tunneling current is first detectable. From the above discussions, it can be firmly concluded that, regardless of bipolar, unipolar or dc stresses, or the polarity of voltage, the start of interface trap generation is well related to the onset of FN injection. For positive voltage, electrons are injected from the Si substrate and the gate is the anode; for negative voltage, electrons are injected from the gate and the Si substrate is the anode. Fig. 7 shows ΔN_{it} as a function of V_s for negative and positive voltages under dc [Fig. 7(a)] and unipolar [Fig. 7(b)] stresses. It is evident in this figure that, regardless of dc or unipolar stresses, ΔN_{it} by negative voltage is much larger than that by positive voltage at higher oxide field. This agrees with the result reported in [7].

Rosenbaum *et al.* suggested that interface traps are generated by the recombination of trapped holes generated during stressing with electrons [16]. We believe that, in addition to
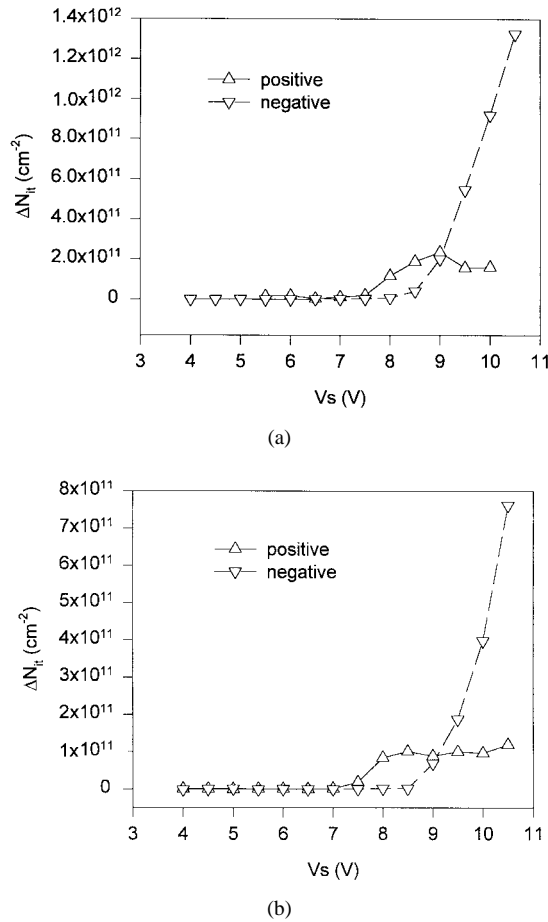
Fig. 7. ΔN_{it} as a function of V_s for (a) positive and negative dc stresses and (b) positive and negative unipolar stresses. Actually, Figs. 5–7 come from the same experimental data.

Fig. 8. Schematic energy band diagram for FN injection under (a) negative voltage and (b) positive voltage.

this mechanism, other mechanisms such as the bond breaking by energetic electrons and by the hydrogen (H and H^+) released during stressing may also contribute to interface trap generation. As shown in Fig. 8(a) for negative voltage, electrons are injected from the gate by tunneling into the oxide conduction band. Electrons gain energy with a distribution from the oxide field [10], [11]. Those electrons which reach the SiO_2/Si interface lose their energy as they drop to the conduction band of the silicon. Part of the energy is converted to interface trap generation as the chemical bonds at the interface are broken by the energetic electrons. Of course, the recombination of the trapped holes generated during stressing with electrons, and the release of hydrogen (see discussions below) may also create interface traps for negative voltage stress. On the other hand, as shown in Fig. 8(b) for positive voltage, electrons are injected from the substrate by tunneling, and they also gain energy from the oxide field. The release of energy of the electrons at the poly-Si/SiO_2 interface will generate electron-hole pairs in the poly-Si, and the holes will be injected into the oxide. Holes may be also generated inside the oxide via impact ionization [16]. Some of the holes drift to the SiO_2/substrate interface (the cathode) under the influence of the electric field, and the recombination of the holes with electrons leads to trap generation at the interface. For both negative and positive voltage stresses, the holes generated
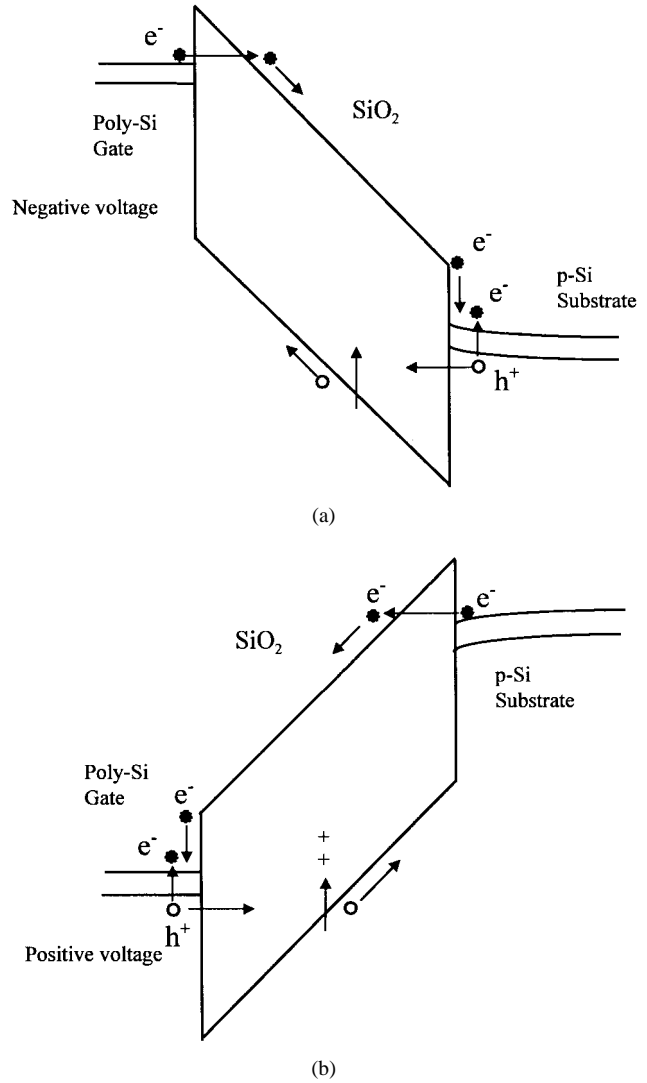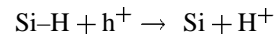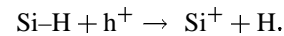
during stressing may react with the Si–H bonds in the SiO_2 layer and the reaction may occur according to one of the following processes [12]
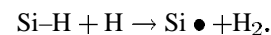
$$Si\text{–}H + h^+ \rightarrow Si + H^+$$

or

$$Si\text{–}H + h^+ \rightarrow Si^+ + H.$$

The released hydrogen atoms (H^+ and H) may move to the SiO_2/substrate interface where they can break a Si–H bond and create an interface trap Si• according to one of the following processes [13]:

$$Si\text{–}H + H^+ + e^- \rightarrow Si \bullet + H_2$$

or

$$Si\text{–}H + H \rightarrow Si \bullet + H_2.$$
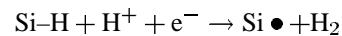
This trap generation model based on the release of hydrogen has been used to explain the post-stress interface trap generation induced by hot carriers [13] and by FN injection [14].
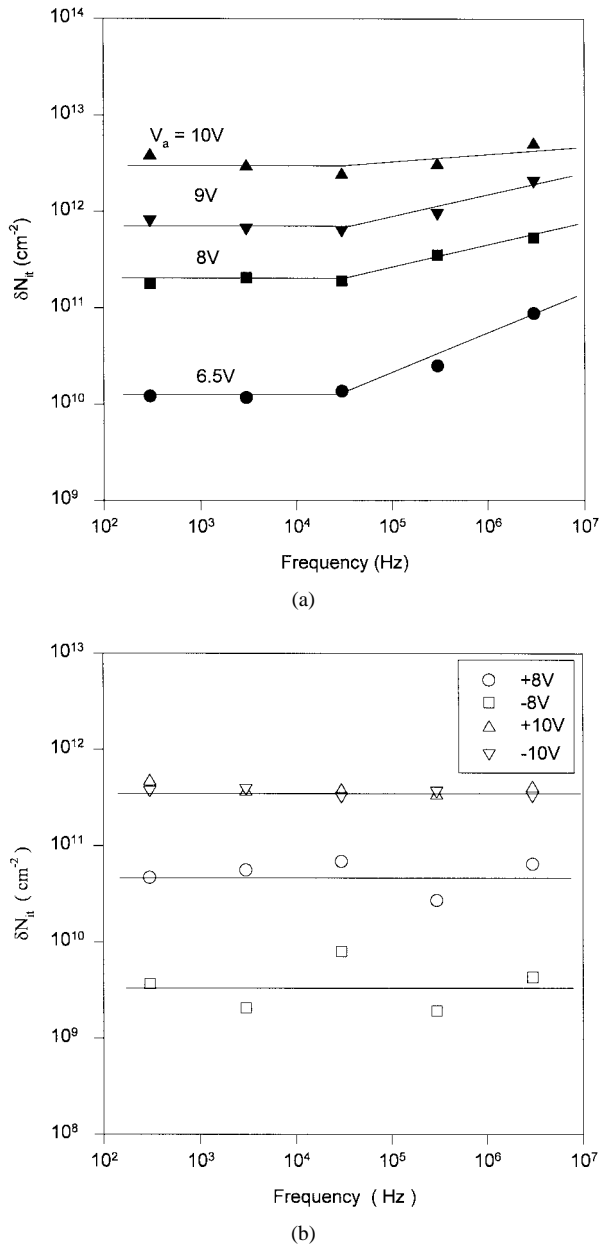
Fig. 9. Interface trap generation as a function of stressing frequency at different V_s for bipolar stress [Fig. 9(a)] and unipolar stress [Fig. 9(b)]. δN_{it} represents the difference between the interface trap density of fresh devices and the interface trap density after a stress at a given frequency and at a voltage amplitude for 20 min. Each stress was carried out on different devices.

Here, it is reasonable to assume that the release of hydrogen may also create some interface traps during the stress period, however, it is difficult to estimate how much the process contributes to the total interface trap generation.

The frequency dependence of interface trap generation for bipolar and unipolar stresses was also investigated. Fig. 9 shows the interface trap generation as a function of frequency at different amplitude V_s of bipolar [Fig. 9(a)] or unipolar [Fig. 9(b)] pluses. Note that δN_{it} shown in Fig. 9 represents the difference between the interface trap density of fresh devices and the interface trap density after the stress at a given frequency and a voltage amplitude for 20 min. Each stress was carried out on different devices. For bipolar stress, as

shown in Fig. 9(a), the frequency dependence of interface trap generation can be divided into two regions: 1) for frequency less than 30 kHz, interface trap generation is essentially independent of frequency; and 2) for frequency larger than 30 kHz, δN_{it} increases linearly with frequency but such a frequency dependence becomes weaker as the amplitude V_s increases. The frequency dependence observed here is different from that reported by Rosenbaum *et al.* [15]. They observed that, for the bipolar stress ($E_{ox} = 11.6$ MV/cm and stress time = 1 or 10 s), interface trap generation first increases with frequency but then decreases with a maximum at around 2 kHz. This disagreement is not understood at this stage. On the other hand, for unipolar stress, as shown in Fig. 9(b), interface trap generation is independent of frequency, being different from the situation of bipolar stress mentioned above. Such a difference is also not understood exactly, and further research is required.

As can be seen in both Figs. 1 and 9, bipolar stress has higher interface trap generation. This observation is consistent with that reported in [15], [16]. In the above discussions, we have already shown that interface traps can be generated by both positive and negative voltage stresses. Thus it is clear that, in contrast to unipolar stress which produces interface traps for only one-half cycle, bipolar stress can produce interface traps for the entire cycle. Actually, Rosenbaum *et al.* [15], [16] have pointed out that the bipolar N_{it} enhancement is nothing more than a reflection of the fact that current flows for one-half cycle under unipolar stress and for the entire cycle under bipolar stress. On the other hand, Fig. 9 shows that interface trap generation increases as the stress voltage increases. Chaparala *et al.* [17] also observed that interface trap generation under negative unipolar stress increases as the oxide field increases. This may be due to the fact that the current flowing through the oxide increases as the oxide field increases.

IV. CONCLUSIONS

This work demonstrates that interface trap generation under the stresses of dc and dynamic (bipolar and unipolar) oxide field can easily be monitored by charge pumping measurement. Regardless of stress type, dc or dynamic (unipolar or bipolar), and the polarity of the stress voltage, interface trap generation starts to occur at the voltage at which the FN tunneling through the oxide starts to build up. While the interface trap generation by positive (or negative) voltage is observed in the experiments of positive (or negative) dc and unipolar stresses, the interface trap generation by both positive and negative voltages during positive and negative half-cycles is also clearly observed in the bipolar experiments. For positive voltage, interface trap generation is attributed to the recombination of trapped holes with electrons and to the bond breaking by the hydrogen (H and H$^+$) released during stressing. For negative voltage, in addition to these two mechanisms, the bond breaking by energetic electrons may also contribute to interface trap generation. The frequency dependence of interface trap generation is also investigated. Interface trap generation is found to be independent of stressing frequency for unipolar stress. However, for bipolar stress, although interface trap

generation is essentially independent of frequency at lower frequencies (less than 30 kHz), it increases with frequency at higher frequency (larger than 30 kHz).

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