Interface Properties of NO-Annealed N_2O-Grown Oxynitride

P. T. Lai, J. P. Xu, and Y. C. Cheng, *Member, IEEE*

***Abstract*— The oxide/Si interface properties of gate dielectric prepared by annealing N_2O-grown oxide in an NO ambient are intensively investigated and compared to those of O_2-grown oxide with the same annealing conditions. Hot-carrier stressings show that the former has a harder oxide/Si interface and near-interface oxide than the latter. As confirmed by SIMS analysis, this is associated with a higher nitrogen peak concentration near the oxide/Si interface and a larger total nitrogen content in the former, both arising from the initial oxidation in N_2O instead of O_2.**

***Index Terms*—Gate dielectrics, hot-carrier stress, MOS devices, MOSFET's, nitridation, oxide/Si interface, oxynitrides.**

I. Introduction

CURRENTLY, for satisfying the needs of scaled MOSFET's, a high-quality thin gate dielectric is desired because the properties of conventional SiO_2 films are not acceptable for these very small-sized transistors [1]–[3]. As an alternative gate dielectric, oxynitrides have drawn considerable attention due to their superior performance and reliability properties over conventional SiO_2 [4]–[8]. However, NH_3-nitrided oxides suffer from hydrogen-related electron trapping problems [5], [6] while N_2O-based oxides require a much higher thermal budget for sufficient nitrogen incorporation [9], [10]. To avoid these disadvantages of NH_3 and N_2O, nitric oxide (NO) has been proposed as a dielectric-growth/anneal ambient to obtain high-quality ultra-thin dielectric films [8], [11]–[16]. Furthermore, NO annealing of an initial oxide grown in pure oxygen is preferred to prepare oxynitride with sufficient thickness in a reasonable growth time, considering the self-limiting nature of the growth process in an NO ambient. Recent studies show that if the initial oxide is grown in N_2O instead of O_2 and then annealed in an NO ambient, suppressed boron penetration and poly-gate depletion can be achieved [17]. In this work, by studying its hardness against various kinds of hot-carrier bombardments, it is further demonstrated that oxide/Si interface properties of the NO-annealed N_2O-grown oxynitride are also superior. The physical mechanisms involved are analyzed by considering interfacial nitrogen profile determined by secondary ion mass spectroscopy (SIMS).

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II. Experimental

The n-channel MOSFET's and MOS capacitors used in this study were fabricated on p-type (100) silicon wafers with a resistivity of 6–8 Ω-cm by a self-aligned n^+ polysilicon gate process. Gate oxides were grown in a conventional horizontal furnace in either dry O_2 or pure N_2O ambient at 950 °C to the same thickness of 70 Å. Then, they were annealed in a pure NO ambient at 950 °C for 30 min (denoted as ONO for O_2 growth and N2ONO for N_2O growth, respectively) to achieve better oxide/Si interface qualities. Final oxide thickness measured by C-V technique was 82 Å for ONO sample and 74 Å for N2ONO sample. Control sample with a film thickness of 80 Å was thermally grown also at 850 °C in dry O_2 (denoted as OX). All gate oxides finally received an *in situ* N_2 anneal at 950 °C for 20 min. Several kinds of stresses were applied on the transistors and capacitors to study their interface and charge trapping characteristics:

1) maximum-substrate-current stress at $V_D = 8$ V, $V_G = 3.5$ V;
2) Fowler–Nordheim (FN) constant-current stress with electron injection at 10 mA/cm^2 from the substrate;
3) low-V_G hot-hole stress at $V_D = 8$ V, $V_G = 1$ V on the transistors;
4) FN constant-current stress with electron injection at -10 mA/cm^2 from the gate of the capacitors, and the oxide/Si interface as the collecting electrode and the site of heavier damage.

Device performances were characterized by the changes of peak linear transconductance (ΔG_m), threshold voltage (ΔV_T), and subthreshold slope (ΔS) of the nMOSFET's, and increase in mid-gap interface-state density (ΔD_{itm}), and change in gate voltage (ΔV_G) during stressing with a constant current density on the MOS capacitors. Two channel length/width (L/W) ratios of the MOSFET's (1.2 μm/24 μm and 100 μm/100 μm) were used with the latter for the stress (2) to eliminate edge effects, while the area of the capacitors was 10^{-4} cm^2. All measurements were carried out under light-tight and electrically shielded condition.

III. Results and Discussions

Firstly, the hardness of the oxide/Si interface is evaluated by the increase of the mid-gap interface-state density obtained

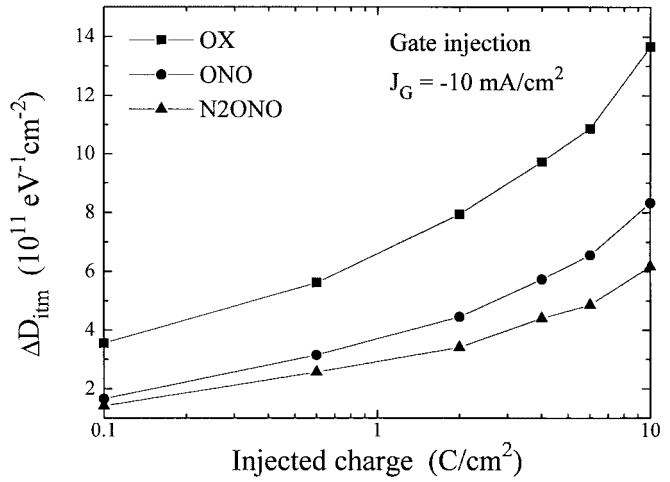


Fig. 1. Increase in midgap interface-state density (ΔD_{itm}) of MOS capacitors with different gate dielectrics under a constant-current stress of -10 mA/cm^2.

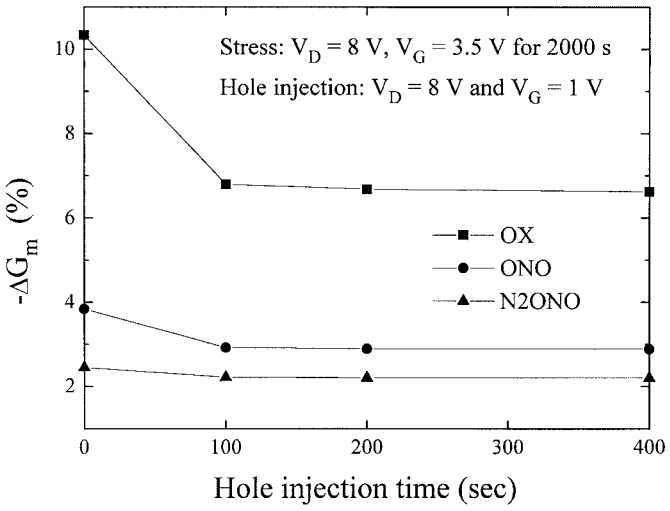


Fig. 2. Degradation of G_m after the maximum substrate-current stress at $V_D = 8$ V and $V_G = 3.5$ V for 2000 s (at zero injection time) and subsequent recovery of ΔG_m with hole injection at $V_D = 8$ V and $V_G = 1$ V on the transistors with W/L = 24/1.2 μm.

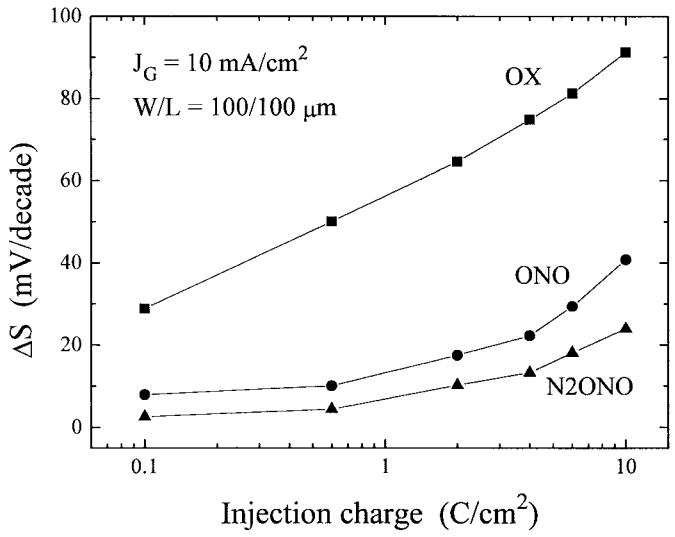


Fig. 3. Degradation of subthreshold slope (ΔS) under channel-hot-electron stress with a constant current density (10 mA/cm^2) and source/drain grounded, on the transistors with W/L = 100/100 μm.

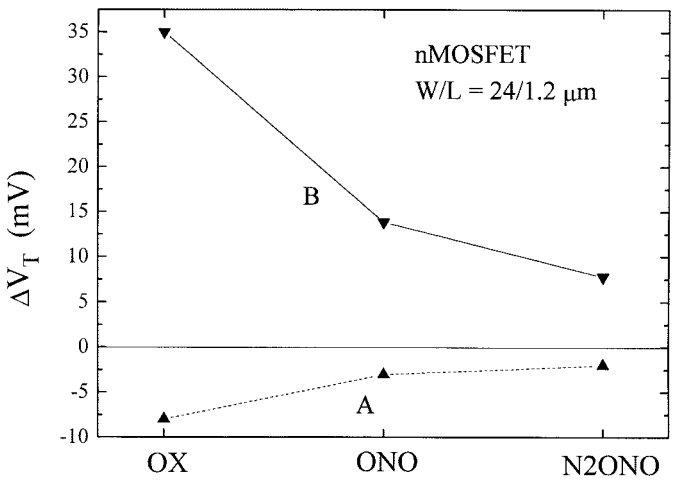
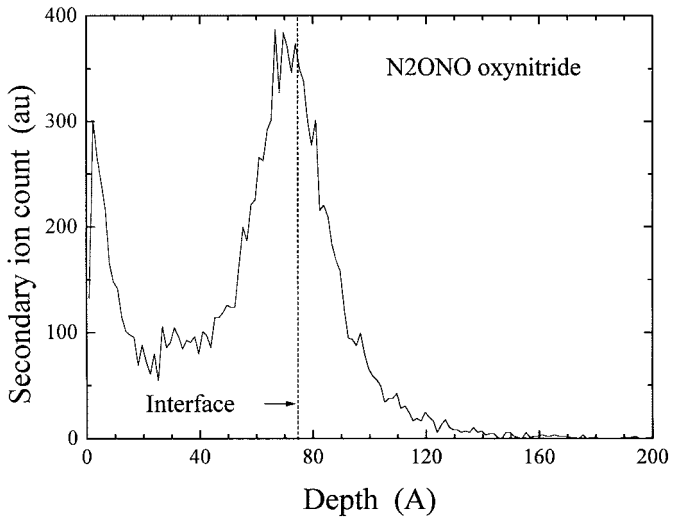


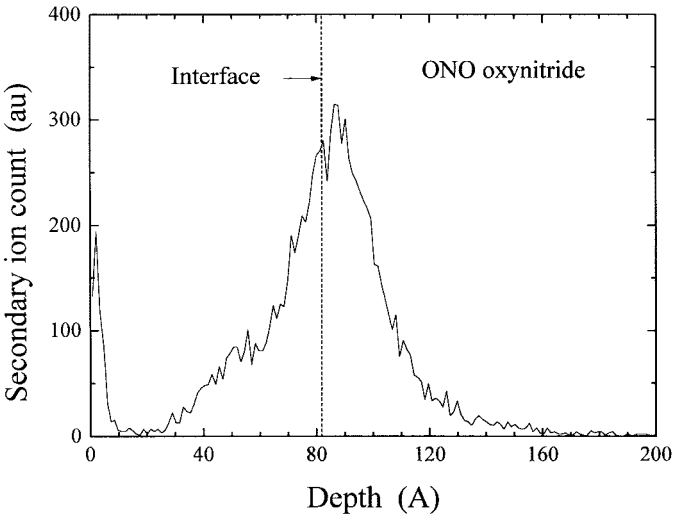
Fig. 4. Threshold voltage shift after a hot-hole stress at $V_D = 8$ V and $V_G = 1$ V for 2000 s (curve A) and subsequent short electron injection phase at $V_D = V_G = 8$ V for 20 s (curve B) on the transistors with W/L = 24/1.2 μm.

from high-low frequency C-V measurements, after a constant-current stress at -10 mA/cm^2 on the capacitors for different injection times. D_{itm} of fresh device is 4×10^{10} cm^{-2} eV^{-1} for OX sample and 7×10^{10} cm^{-2} eV^{-1} for the two nitrided samples. As shown clearly in Fig. 1, the two nitrided samples exhibit greatly suppressed creation of oxide/Si interface states as compared to OX sample due to interfacial nitrogen incorporation, with N2ONO sample slightly better than ONO sample. Furthermore, a maximum-substrate-current stress ($V_D = 8$ V and $V_G = 3.5$ V for 2000 s) is used to characterize the oxide/Si interface of the transistors (W/L = 24/1.2 μm). Since both electrons and holes are injected during this stress, a subsequent hole injection at $V_D = 8$ V and $V_G = 1$ V is employed to eliminate the effects of electron trapping near the interface on ΔG_m. Fig. 2 shows the post-stress ΔG_m (at zero injection time) and the change of ΔG_m with subsequent hole injection. It can be seen that both post-stress ΔG_m and its recovery due to the neutralization of near-interface trapped electrons by injected holes are smaller for N2ONO than ONO sample. This, on one hand, indicates that the oxide/Si interface of the former is harder than that of the latter, and on the other hand, electron trapping near the interface is also less for the former. In addition, a FN constant-current stress at 10 mA/cm^2 with source and drain grounded is also carried out on the transistors with W/L = 100/100 μm. As distinct from the above hot-carrier stress, which results in nonuniform degradation along the channel direction, FN electron-injection stress leads to a uniform damage in the gate oxide. Fig. 3 gives the degradations of subthreshold slope (ΔS) of the three devices under the FN stress with electron injection from the substrate ($V_G > 0$). Once again, a smaller ΔS for N2ONO sample than ONO sample is found.

Moreover, generation of neutral electron traps in N2ONO oxynitride is also greatly suppressed. Fig. 4 shows the threshold-voltage shift after a hot-hole stress at $V_D = 8$ V



(a)



(b)

Fig. 5. SIMS profiles of nitrogen for two oxynitrides: (a) N2ONO oxynitride, and (b) ONO oxynitride.

and $V_G = 1$ V for 2000 s (curve A) and a subsequent short electron-injection phase at $V_D = V_G = 8$ V for 20 s (curve B) on the transistors with W/L = 24/1.2 μm. Shifting of curve A to curve B is due to the compensation of trapped holes and filling of neutral electron traps by injected electrons. Thus the smallest ΔV_T for N2ONO sample implies the least neutral-electron-trap generation and hole trapping in the gate oxide of this device.

The above facts unanimously suggest that a double nitridation with N_2O oxidation followed by NO annealing can lead to a harder oxide/Si interface and near-interface oxide than a single NO nitridation. This is certainly related to their different nitridation mechanisms and thus different nitrogen distributions near the oxide/Si interface because it is believed that excellent endurance of oxynitride is due to the pile-up of nitrogen at the oxide/Si interface [18], [19]. The SIMS profiles of nitrogen for the two oxynitrides are shown in Fig. 5. It can be clearly seen that there is a higher nitrogen peak concentration (N_p) for N2ONO sample than ONO sample.

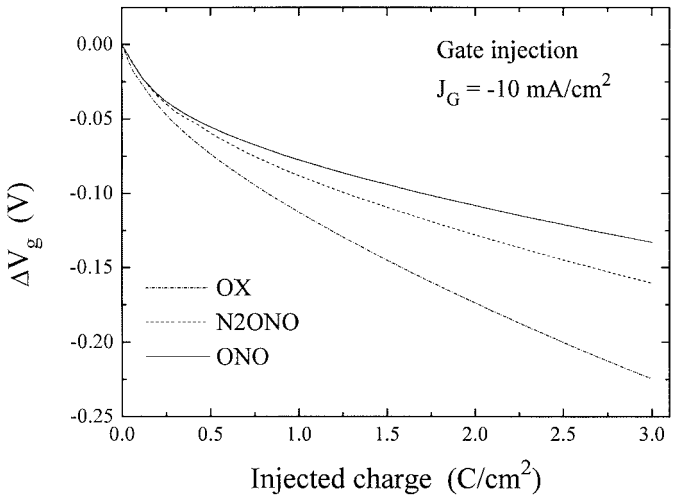


Fig. 6. Change in gate voltage of MOS capacitors under a constant-current stress of -10 mA/cm^2.

Moreover, the location of N_p is almost at the interface for N2ONO sample, while it is inside the Si substrate for ONO sample. Thus the total nitrogen content in N2ONO oxynitride is more than that in ONO oxynitride since the two nitrogen profiles have almost identical width at half of the N peak value (30 Å for N2ONO oxynitride and 32 Å for ONO oxynitride). This results in the formation of more strong Si-N and N-O bonds in N2ONO oxynitride than in ONO oxynitride, and thus a harder interface and near-interface oxide. For N2ONO oxynitride, the higher N_p is due to additional incorporation of nitrogen during the N_2O oxidation and the N_p position is determined by the combined effect of N_2O and NO nitridations, with resulting N_p of N_2O nitridation inside the oxide [20] while subsequent NO nitridation moving the peak toward the oxide/Si interface by depleting nitrogen in the oxide bulk and accumulating nitrogen at the oxide/Si interface. Also the smaller thickness increase of N2ONO oxynitride (4 Å) than that of ONO oxynitride (12 Å) after NO annealing implies that better oxidation resistance can be obtained when the initial oxide is grown in N_2O ambient, which is also one of reasons for its higher N_p.

Finally, as a supplemental evaluation, electron trapping properties of the three samples are characterized by the change in gate voltage (ΔV_G) to maintain a constant-current density of -10 mA/cm^2 on the capacitors. As shown in Fig. 6, the electron trapping property of N2ONO oxynitride is slightly poorer than that of ONO oxynitride. This is associated with more nitrogen in the bulk of N2ONO oxynitride than ONO oxynitride, because bulk nitrogen degrades the breakdown characteristics of oxynitrides which are related to electron trapping [20]. The more bulk nitrogen in N2ONO oxynitride should come from the N_2O furnace oxidation, which results in nitrogen incorporation throughout almost the whole oxide [20]. Fortunately, the bulk nitrogen can be reduced by the NO annealing through a possible reaction [21]:

$$\text{Si-N-Si} + \text{NO} \rightarrow \text{Si-O-Si} + \text{N}_2.$$

As demonstrated in Fig. 5(a), nitrogen concentration is indeed rather low in a large portion of the oxide after the NO

annealing. It is expected that if the NO-annealing time is properly optimized, the remaining bulk nitrogen can become negligible.

IV. Summary

Compared to NO-annealed O_2-grown oxide, NO-annealed N_2O-grown oxynitride shows better oxide/Si interface and near-interface oxide qualities. As a result, longer endurance of the latter against hot-carrier stresses is observed. This is attributed to higher interfacial nitrogen concentration and total nitrogen content resulting from the double-nitridation process. On the other hand, more nitrogen in the bulk of the former is responsible for its slightly poorer electron-trapping properties, which can be removed by optimizing the NO-annealing step, and thus minimizing the bulk nitrogen content without decreasing the interfacial nitrogen concentration. Higher nitrogen concentration at the interface is also beneficial to resist dopant penetration through the gate oxide, especially in p^+ poly-gate p-MOSFET's of dual-gate CMOS technologies. Therefore, NO-annealed N_2O-grown oxynitride could be a highly reliable gate dielectric for future-generation MOS devices.

References

[1] K. Naruke, S. Taguchi, and M. Wada, "Stress induced leakage current limiting to scale down EEPROM tunnel oxide thickness," in *IEDM Tech. Dig.*, 1988, p. 424.

[2] P. Olivo, T. N. Ngyyen, and B. Ricco, "High-field-induced degradation in ultrathin SiO_2 films," *IEEE Trans. Electron Devices*, vol. 35, p. 2259, 1988.

[3] R. Moazzami and C. Hu, "Stress-induced current in this silicon dioxide films," in *IEDM Tech. Dig.*, 1992, p. 92.

[4] T. Hori, H. Iwasaki, and K. Tsuji, "Electrical and physical characteristics of ultrathin reoxidized nitride oxides prepared by rapid thermal processing," *IEEE Trans. Electron Devices*, vol. 36, p. 340, 1989.

[5] P. Pan, "Characteristics of thermal SiO_2 films during nitridation," *J. Appl. Phys.*, vol. 61, p. 284, 1986.

[6] Z. H. Liu, H.-J. Wann, P. K. Ko, C. Hu, and Y. C. Cheng, "Effects of N_2O anneal and reoxidation on thermal oxide characteristics," *IEEE Electron Device Lett.*, vol. 13, p. 402, 1992.

[7] H. Fukuda, M. Yasuda, T. Iwabuchi, and S. Ohno, "Novel N_2O-oxynitridation technology for forming high reliable EEPROM tunnel oxide film," *IEEE Electron Device Lett.*, vol. 12, p. 587, 1991.

[8] J. Ahn, W. Ting, and D.-L. Kwong, "Furnace nitridation of thermal SiO_2 in pure N_2O ambient for ULSI MOS applications," *IEEE Electron Device Lett.*, vol. 13, p. 117, 1992.

[9] G. W. Yoon, A. B. Joshi, J. Kim, and D. L. Kwong, "MOS characteristics of NH_3 nitrided N_2O-grown oxides," *IEEE Electron Device Lett.*, vol. 14, p. 179, 1993.

[10] T. Hori, "Nitrided gate-oxide CMOS technology for improved hot-carrier reliability," *Microelectron. Eng.*, vol. 22, p. 245, 1993.

[11] Z.-Q. Yao, H. B. Harrison, S. Dimitrijev, Y. T. Yeow, and D. Sweatman, "High quality ultra thin dielectric films grown on silicon in a nitric oxide anbient," *Appl. Phys. Lett.*, vol. 64, p. 3845, 1994.

[12] Z.-Q. Yao, H. B. Harrison, S. Dimitrijev, and Y. T. Yeow, "The electrical properties of sub-5-nm oxynitride dielectrics prepared in a nitric oxide ambient using rapid thermal processing," *IEEE Electron Device Lett.*, vol. 15, p. 516, 1994.

[13] Y. Okada, P. J. Tobin, K. G. Reid, R. I. Hegde, B. Maiti, and S. A. Ajuria, "Furnace grown gate oxynitride using nitric oxide (NO)," *IEEE Trans. Electron Devices*, vol. 41, p. 1608, 1994.

[14] L. K. Han, D. Wristers, J. Yan, M. Bhat, and D. L. Kwong, "Highly suppressed boron penetration in NO-nitrided SiO_2 for p^+-polysilicon gate MOS device application," *IEEE Electron Device Lett.*, vol. 16, p. 319, 1995.

[15] M. Bhat, J. Kim, J. Yan, G. W. Yoon, L. K. Han, and D. L. Kwong, "MOS characteristics of ultrathin NO-grown oxynitrides," *IEEE Electron Device Lett.*, vol. 15, p. 421, 1994.

[16] Z.-Q. Yao, H. B. Harrison, S. Dimitrijev, and Y. T. Yeow, "Effects of nitric oxide anneling of thermally grown silicon dioxide characteristics," *IEEE Electron Device Lett.*, vol. 16, p. 345, 1995.

[17] C. Lin, A. I. Chou, K. Kumar, P. Chowdhury, and J. C. Lee, "Leakage current, reliability characteristics, and boron penetration of ultra-thin (32–36 Å) O_2-oxides and N_2O/NO oxynitrides," in *IEDM Tech. Dig.*, 1996, p. 331.

[18] T. Hori and H. Iwasaki, *J. Appl. Phys.*, vol. 65, p. 629, 1989.

[19] W. Ting, H. Hwang, J. Lee, and D. L. Kwong, *Appl. Phys. Lett.*, vol. 57, p. 2808, 1990.

[20] Y. Okada, P. J. Tobin, V. Lakhotia, W. A. Feil, and S. A. Ajuria, "Relationship between growth conditions, nitrogen profile, and charge to breakdown of gate oxynitrides grown from pure N_2O," *Appl. Phys. Lett.*, vol. 63, p. 194, 1993.

[21] N. S. Saks, and D. I. Ma, and W. B. Fowler, "Nitrogen depletion during oxidation in N_2O," *Appl. Phys. Lett.*, vol. 67, p. 374, 1995.

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