

# Improvement of SiGe oxide grown by electron cyclotron resonance using H<sub>2</sub>O vapor annealing

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(Received 13 June 1996; accepted for publication 16 August 1996)

The influence of low-temperature annealing in H<sub>2</sub>O vapor on electron-cyclotron-resonance (ECR) grown SiGe oxides is reported. Annealing the oxides in H<sub>2</sub>O vapor at 280 °C for 3 h 20 min, applied after annealing in forming gas at 450 °C for 30 min, has several important effects: It reduces oxide leakage current by up to four orders of magnitude, decreases the density of interface states, and results in a low fixed oxide charge density of  $-5.0 \times 10^{10} \text{ cm}^{-2}$  in comparison to those of the films subjected to annealing in forming gas only. In addition, higher cumulative dielectric breakdown fields up to 8 MV/cm have been achieved. From the results obtained it is evident that vapor annealing is beneficial for ECR-grown SiGe oxides. © 1996 American Institute of Physics. [S0003-6951(96)04543-3]

The development of a high-mobility SiGe *p*-channel metal–oxide–semiconductor field-effect transistor (*p*-MOSFET) is important since it allows one to reduce the size of the *p*-MOSFET in complementary metal–oxide–semiconductor (CMOS) circuit design. There have been several attempts to implement *n*-strained Si as a conducting channel;<sup>1,2</sup> however, the existence of parasitic low-mobility conduction channel in the buffer layer degrades the performance of such a device, and an additional graded SiGe layer is required to reduce the band discontinuity.<sup>2</sup> The use of SiGe as the conducting channel in a heterostructure eliminates this problem and gives the advantage of high hole mobility.<sup>3,4</sup> Recently, a SiGe channel *p*-MOSFET with electron–cyclotron-resonance (ECR) -grown gate oxide has been reported demonstrating higher peak hole mobility than that of a conventional Si *p*-MOSFET.<sup>5</sup> The values of the peak hole mobility for SiGe *p*-MOSFETs reported in the literature are comparable to those of strained Si/SiGe *p*-MOSFETs with the same Ge content.<sup>1,5</sup> The limits on the SiGe channel MOS transistor performance are mainly due to poor gate oxide. The thermal oxidation of SiGe in pure oxygen or steam has not been successful due to the nonstoichiometric oxide and formation of Ge-rich layers.<sup>6</sup> ECR plasma oxidation has been shown to be an efficient alternative method of SiGe oxide growth,<sup>7</sup> but the quality of these oxides is lower than that of the state-of-the-art thermal SiO<sub>2</sub> and therefore needs further improvement. Postannealing in forming gas is a conventional way of improving the bulk properties of SiO<sub>2</sub> as well as the SiO<sub>2</sub>/Si interface. Another effective method, low-temperature wet annealing, recently proposed by Sano *et al.*,<sup>8</sup> has been reported to improve the properties of the SiO<sub>2</sub>/Si interface and bulk SiO<sub>2</sub> formed by remote plasma chemical–vapor deposition. As a result, high-performance poly-Si thin-film transistors have been achieved.<sup>9</sup>

In this letter we apply the low-temperature wet annealing technique combined with forming gas annealing to the ECR-grown SiGe oxide. The properties of the SiGe oxide are significantly improved. The best results obtained for the samples after combined annealing in forming gas and in H<sub>2</sub>O vapor are the midgap interface state density of  $\sim 1.5$

$\times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  and the oxide fixed charge density of  $-5.0 \times 10^{10} \text{ cm}^{-2}$ .

SiGe samples were prepared by ultrahigh-vacuum (UHV) CVD (UHV/CVD) on a 0.0038–0.008 Ω cm *n*-type Si (100) substrate. The layer structure consists of a 1000 Å *n*-type Si buffer and a 1000 Å strained *n*-type Si<sub>0.85</sub>Ge<sub>0.15</sub> layer with doping concentration of  $2 \times 10^{17} \text{ cm}^{-3}$ . Samples were chemically cleaned as described in previous work<sup>7</sup> and dipped in 10% hydrofluoric acid for 15 s to leave a hydrogen passivated surface. Oxides were grown using the ECR microwave plasma source with a maximum power of 250 W at 2.45 GHz at different substrate temperatures (0–300 °C). Hydrogen plasma precleaning was used to remove the native oxide. The oxidation was performed under the substrate bias of +4 V which provides the optimal condition for ECR oxide growth.<sup>7</sup> Oxide thickness of 90–160 Å with a uniformity of 5% was measured by *ex situ* single-wavelength ellipsometry. The refractive index of films was found to be 1.42 at a wavelength of 632.8 nm. After the SiGe oxide was grown, the postannealing in forming gas was performed. The samples were annealed in forming gas with a rapid thermal

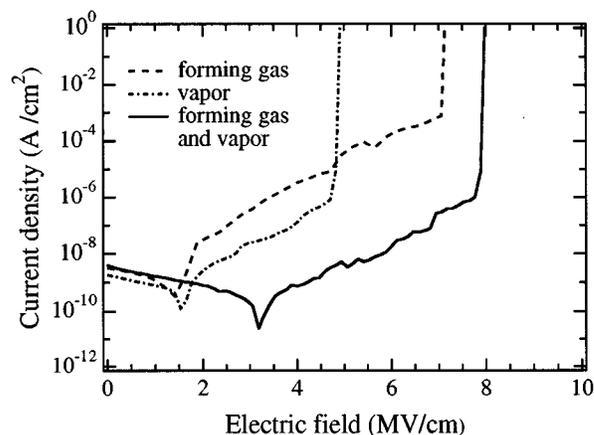


FIG. 1. Leakage current density as a function of oxide electric field for SiGe oxide ( $d_{\text{ox}}=90 \text{ Å}$ ) annealed (a) in forming gas at 450 °C for 30 min, (b) in H<sub>2</sub>O vapor at 280 °C for 200 min. (c) Combined annealing under the same conditions as in (a) and (b).

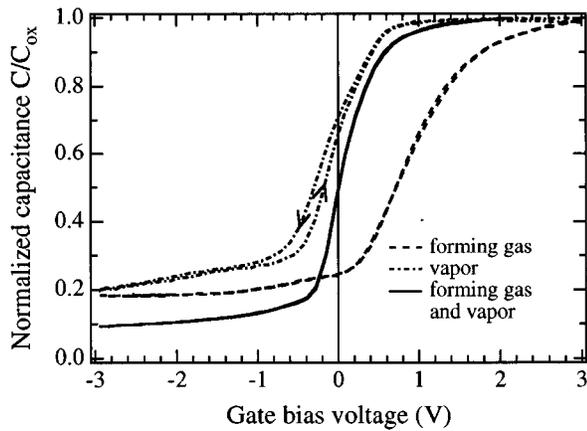


FIG. 2. High-frequency  $C-V$  curves for SiGe oxide annealed (a) in forming gas at 450 °C for 30 min, (b) in  $H_2O$  vapor at 280 °C for 150 min. (c) Combined annealing under the same conditions as in (a) and (b).

annealing Heat Pulse 210T-02 system at 450 °C for 30 min. A set of Al gate MOS capacitors with diameters of 100–400  $\mu\text{m}$  was thereafter formed using conventional vacuum evaporation. The vapor annealing was carried out with an electrically heated quartz furnace which was evacuated by a mechanical pump and back filled with  $H_2O$  vapor by heating de-ionized  $H_2O$ . Vapor pressure was controlled by the temperature of de-ionized  $H_2O$ . The furnace was kept at 280 °C for 100–250 min in  $H_2O$  vapor with pressure of 50 Torr during annealing.

The oxide properties of MOS capacitors were studied by measuring current–voltage ( $I-V$ ) as well as at high frequency (1 MHz) and quasistatic capacitance–voltage ( $C-V$ ) characteristics. Figure 1 shows the typical leakage current density as a function of the oxide electric field extracted from  $I-V$  curves for SiGe MOS capacitors with different annealing schemes. Oxide films subjected to combined annealing in forming gas and  $H_2O$  vapor exhibit significantly lower leakage current densities than samples annealed either in forming gas or in  $H_2O$  vapor. Very low values of leakage current densities for fields  $<4$  MV/cm indicate the reduction of leakage due to tunneling and better oxide quality. Annealing in  $H_2O$  vapor also increases the cumulative dielectric breakdown field to 8 MV/cm when combined with annealing in forming gas. The dielectric breakdown field increases with

wet annealing time and saturation seems to happen after  $\sim 200$  min of annealing. The best oxides were obtained by annealing in forming gas at 450 °C for 30 min followed by wet annealing at 280 °C for 200 min. Annealing temperatures from 100 to 400 °C were applied, but no clear dependence of oxide quality on temperature was observed, and temperatures below 200 °C were found to be ineffective. This is in agreement with the results observed in poly-Si,<sup>8,9</sup> which supports the idea of  $H_2O$  vapor having a catalytic effect on oxide film.

Figure 2 shows the high-frequency  $C-V$  curves for oxides annealed under different conditions. Typically, oxides annealed only in  $H_2O$  vapor demonstrate a hysteresis in the  $C-V$  curves due to the mobile charges, which decreases with annealing time and becomes negligible after  $\sim 200$  min of annealing. The samples annealed in forming gas followed by wet annealing exhibit a very low oxide fixed charge  $Q_f \sim -5.0 \times 10^{10} \text{ cm}^{-2}$  which is the lowest for SiGe oxides reported in the literature.<sup>7,10</sup> Wet annealing also shifts the  $C-V$  curves and results in a low flatband voltage of typically +0.2 V compared with +0.3–+0.5 V for the original sample preannealed in forming gas. The reduction of the flatband voltage and oxide fixed charge takes place for oxide films grown at any substrate temperatures, but the lowest values were found for the oxides grown at low (0–15 °C) substrate temperature. A summary of the oxide properties under different annealing conditions is shown in Table I. Annealing in  $H_2O$  vapor also reduces the stretchout of high-frequency  $C-V$  indicating the reduction of interface state density. From quasistatic  $C-V$  measurements the lowest interface state density is found to be  $D_{it} \approx 1.5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  at midgap which is comparable to the lowest values achieved earlier.<sup>5,7,10</sup>

The physical meaning of annealing in forming gas and  $H_2O$  vapor comes from the ability of hydrogen species to react with unsaturated silicon atoms at the oxide/semiconductor interface forming Si–H bonds. In the case of  $H_2O$  vapor annealing, Balk, Burkhardt, and Gregor<sup>11</sup> proposed that hydrogen is evolved by the reaction of the aluminum gate with  $H_2O$  by some reaction such as  $2\text{Al} + 3\text{H}_2\text{O} \rightarrow 6\text{H} + \text{Al}_2\text{O}_3$  to form atomic hydrogen ( $\text{H}_\cdot$ ) which diffuses to the interface and reacts with unsaturated silicon ( $\rightarrow \text{Si}_\cdot$ ) to eliminate an interface state:  $\text{H}_\cdot + \rightarrow \text{Si}_\cdot \leftrightarrow \text{Si-H}$ . The hydrogen–ambient forming gas

TABLE I. Electrical properties of ECR-grown SiGe MOS capacitors from  $C-V$  measurements for different annealing conditions.

Deposition temperature (°C)	Type of annealing	Aluminum deposition before or after vapor annealing	Fixed charge ( $10^{11} \text{ cm}^{-2}$ )	Breakdown field range (MV/cm)	Interface state density at midgap ( $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ )
15	forming gas		–2.5	4.9–6.3	3.2
15	vapor	before	–1.8	3.2–3.9	2.5
15	forming gas, vapor	before	–0.57	7.0–8.1	1.9
15	forming gas, vapor	after	–2.0	4.8–6.0	3.0
0	forming gas		–1.9	5.1–6.7	2.9
0	vapor	before	–1.3	3.5–4.5	2.1
0	forming gas, vapor	before	–0.43	7.5–8.8	1.4
0	forming gas, vapor	after	–1.7	4.9–6.2	2.7

annealing operates on similar principle, except that the hydrogen is supplied directly in the ambient, and the structure need not be metallized.<sup>12</sup> The fixed oxide charge is minimized by annealing because dangling silicon bonds react with the remaining oxidants that were dissolved in the deposited oxide and which diffuse toward the interface.<sup>13</sup>

To confirm the development of hydrogen species from the reaction of H<sub>2</sub>O with Al, the effect of H<sub>2</sub>O vapor annealing before and after metal deposition was compared. The samples with Al deposited after H<sub>2</sub>O annealing have an interface state density higher than for the samples with Al deposited before H<sub>2</sub>O annealing as shown on Table I. These results confirm that the reaction between Al and H<sub>2</sub>O is essential to produce hydrogen species that are able to reduce the interface state density. Atomic hydrogen H, OH group, and H<sub>2</sub>O are the major diffusion species with high diffusion constant values of  $D \sim 2 \times 10^{-7}$ ,  $10^{-9}$ , and  $10^{-13}$  cm<sup>2</sup>/s at 300 °C, respectively, for SiO<sub>2</sub>.<sup>14</sup> These diffusion coefficients are a good estimate for SiGe oxide and substantially higher than that of phosphorus ( $\sim 10^{-25}$  cm<sup>2</sup>/s), which was the doping material for SiGe and therefore exists in the oxide. The characteristic diffusion length is  $l = 2\sqrt{Dt} \sim 10^{-3}$  cm (at 300 °C,  $t = 1$  s) for the fastest diffusion element H which is three orders of magnitude larger than the oxide thickness. Thus, hydrogen and its species are the major components migrating into the oxide field. Nevertheless, Sano *et al.*<sup>8</sup> discovered from infrared-absorption spectra that H<sub>2</sub>O vapor annealing reduces the concentration of H<sub>2</sub>O and OH group in SiO<sub>2</sub>. The diffusion of hydrogen species seems to be the dominant process accountable for the improvement of the oxide quality.

In summary, we have presented the improvement of SiGe oxide grown by ECR using H<sub>2</sub>O vapor annealing.

H<sub>2</sub>O vapor annealing combined with forming gas annealing reduces the interface state density, the oxide fixed charge, and the leakage current, and also results in high cumulative dielectric breakdown fields.

This work was supported by the Joint Services Electronics Program under Contract No. DAAH04-94-G-0057 and National Science Foundation under Grant No. ECS-93-19987.

<sup>1</sup>K. Rim, J. Welsler, J. L. Hoyt, and J. F. Gibbons, IEDM Technical Digest, 1995, p. 517.

<sup>2</sup>S. Verdonckt-Vandebroek, E. F. Crabbe, B. S. Meyerson, D. L. Hareme, P. J. Restle, J. M. C. Stork, and J. B. Johnson, IEEE Trans. Electron Devices **41**, 90 (1994).

<sup>3</sup>K. Ismail, O. J. Chu, and B. S. Meyerson, Appl. Phys. Lett. **64**, 3124 (1994).

<sup>4</sup>D. K. Nayak, J. C. S. Woo, J. S. Park, K. L. Wang, and K. P. MacWilliams, Appl. Phys. Lett. **62**, 2853 (1993).

<sup>5</sup>P. W. Li, E. S. Yang, Y. F. Yang, J. O. Chu, and B. S. Meyerson, IEEE Electron Device Lett. **EDL-15**, 402 (1994).

<sup>6</sup>H. K. Liou, P. Mei, U. Gennser, and E. S. Yang, Appl. Phys. Lett. **59**, 1200 (1991).

<sup>7</sup>P. W. Li and E. S. Yang, Appl. Phys. Lett. **63**, 2938 (1993).

<sup>8</sup>N. Sano, M. Sekiya, M. Hara, A. Kohno, and T. Sameshima, Appl. Phys. Lett. **66**, 2107 (1995).

<sup>9</sup>N. Sano, M. Sekiya, M. Hara, A. Kohno, and T. Sameshima, IEEE Electron Device Lett. **EDL-16**, 157 (1995).

<sup>10</sup>I. S. Goh, J. F. Zhang, S. Hall, W. Eccleston, and K. Werner, Semicond. Sci. Technol. **10**, 818 (1995).

<sup>11</sup>P. Balk, L. V. Burkhardt, and L. V. Gregor, Proc. IEEE **53**, 2133 (1965).

<sup>12</sup>E. H. Nicollian and J. R. Brews, *Metal Oxide Semiconductor Physics and Technology* (Wiley, New York, 1982), p. 782.

<sup>13</sup>B. E. Deal, M. Sklar, A. S. Grove, and E. H. Snow, J. Electrochem. Soc. **114**, 266 (1967).

<sup>14</sup>See, for example, W. Stanley and R. N. Tauber, *Silicon Processing for the VLSI Era* (Lattice, Sunset Beach, CA, 1986), p. 262.