

Fast Detection of Instability in Sigma-Delta Modulators Based on Unstable Embedded Limit Cycles

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Abstract—As a sequel to a previous study (Wong and Ng) on the nonlinear dynamical behavior of low-pass, high-order (order > 2), single-bit $\Sigma\Delta$ modulators with distinct unit-circle noise transfer function zeros, this paper proposes a novel scheme for the fast detection of unstable operation in these modulators under general time-varying input. The scheme is based on the variation of unstable embedded limit-cycle fixed points (which form the bounds beyond which the modulator becomes unstable) versus modulator input amplitude. Deployment of the detection scheme requires simple analog components with possible simplification. The effectiveness of the scheme is demonstrated with numerical examples.

Index Terms—Delta-sigma ($\Delta\Sigma$) modulator, detection, fixed point, instability, limit cycle, recovery, sigma-delta ($\Sigma\Delta$) modulator.

I. INTRODUCTION

THIS PAPER is a sequel to Wong and Ng [1]. Despite the dc stability of a sigma-delta ($\Sigma\Delta$) modulator, it is unsafe to assume its stability under all types of ac (time-varying) input. In general, a dc-stable $\Sigma\Delta$ modulator is stable for slow time-varying input wherein the input signal approaches dc under the high oversampling ratio (OSR). In fact, in these cases, the modulator can often sustain input amplitudes higher than its dc input bound [2]. However, when the nature of the input is not known, stability can never be assured no matter what the input amplitude is. For example, the dc-stable, widely adopted second-order low-pass (LP) $\Sigma\Delta$ modulator can be driven to instability under certain ac input of small amplitudes [3], though the input signal is somehow contrived and unlikely to occur in nature. In practice, it is therefore important to efficiently detect instability of a $\Sigma\Delta$ modulator and subsequently restore its normal operation.

There are generally two conditions that lead to unstable modulator operation, namely, signal overload and modulator power up [4]. Both cases correspond to the state trajectories evolving toward infinity due to a transition state outside the appropriate positively invariant set (PIS) as depicted in [1]. Current research

to tackle instability of a $\Sigma\Delta$ modulator comprises the more sophisticated, adhoc solution that tracks the internal integrator outputs and provides external control through some digital logics. Examples include the switching control of Zourntos and Johns [5] intended for continuous-time loop filtering, the integrator local feedback method of Moussavi and Leung [6], the nonlinear filtering scheme of Thurston and Hawksford [7], and the “local nonlinear feedback loop” of Ho and Kuo [8] (note that this scheme actually works by limiting the input dynamic range and does not necessarily guarantee stability because instability can still be triggered by small input as mentioned). Drawbacks of these schemes are their complexity and nontrivial implementation of the control logics. The digital compensation and/or correction required in some of these schemes also hamper the binary format of the single-bit $\Sigma\Delta$ modulator output, making subsequent processing less elegant and more difficult.

Commonly used recovery schemes are to first check for instability, and then either to issue a global reset or limit the integrator outputs (e.g., [4] and [9]). Nonetheless, nonlinear limiting or clipping of internal integrators is prone to output distortion. This is because for low clipping levels, the integrators may be clipped even during normal operation, while high clipping levels will result in delayed remedy and therefore poor signal-to-noise ratio (SNR) at the output. In view of this, the instability detect-and-reset scheme is more favorable provided fast detection of unstable operation is viable. Two practically adopted detection schemes include: 1) unstable bit pattern search in the $\Sigma\Delta$ output bitstream and 2) comparison of integrator swings against certain thresholds [4, ch. 4, 5]. The method of searching for instability bit pattern, however, is flawed from the outset because once the pattern can be found, the modulator is already in its unstable mode. The second method faces the same problem as in the clipping scheme because it is hard to assign the triggering levels (thresholds) for stability recovery mechanism. The effectiveness of these schemes thus mainly relies on the algorithm for detecting instability. Currently, apart from simulation and linearized analyzes, there are no analytical results regarding the stable integrator swings of a general, high-order (order > 2) $\Sigma\Delta$ modulator, and when the appropriate recovery action, such as a global reset, should be taken. A theory and algorithm on the fast detection of unstable $\Sigma\Delta$ operation would be practically useful.

As an extension of the nonlinear dynamical analysis on a certain class of single-bit $\Sigma\Delta$ modulators in [1] [namely, LP high-order $\Sigma\Delta$ modulators with distinct unit-circle noise transfer function (NTF) zeros], a scheme is devised for detecting unstable operation in these modulators. The scheme is

Manuscript received December 18, 2002; revised December 15, 2003. This work was supported by the Hong Kong Research Grants Council and by the University Research Committee of The University of Hong Kong. This paper was recommended by Associate Editor G. Cauwenbergs.

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Digital Object Identifier 10.1109/TCSII.2004.831375

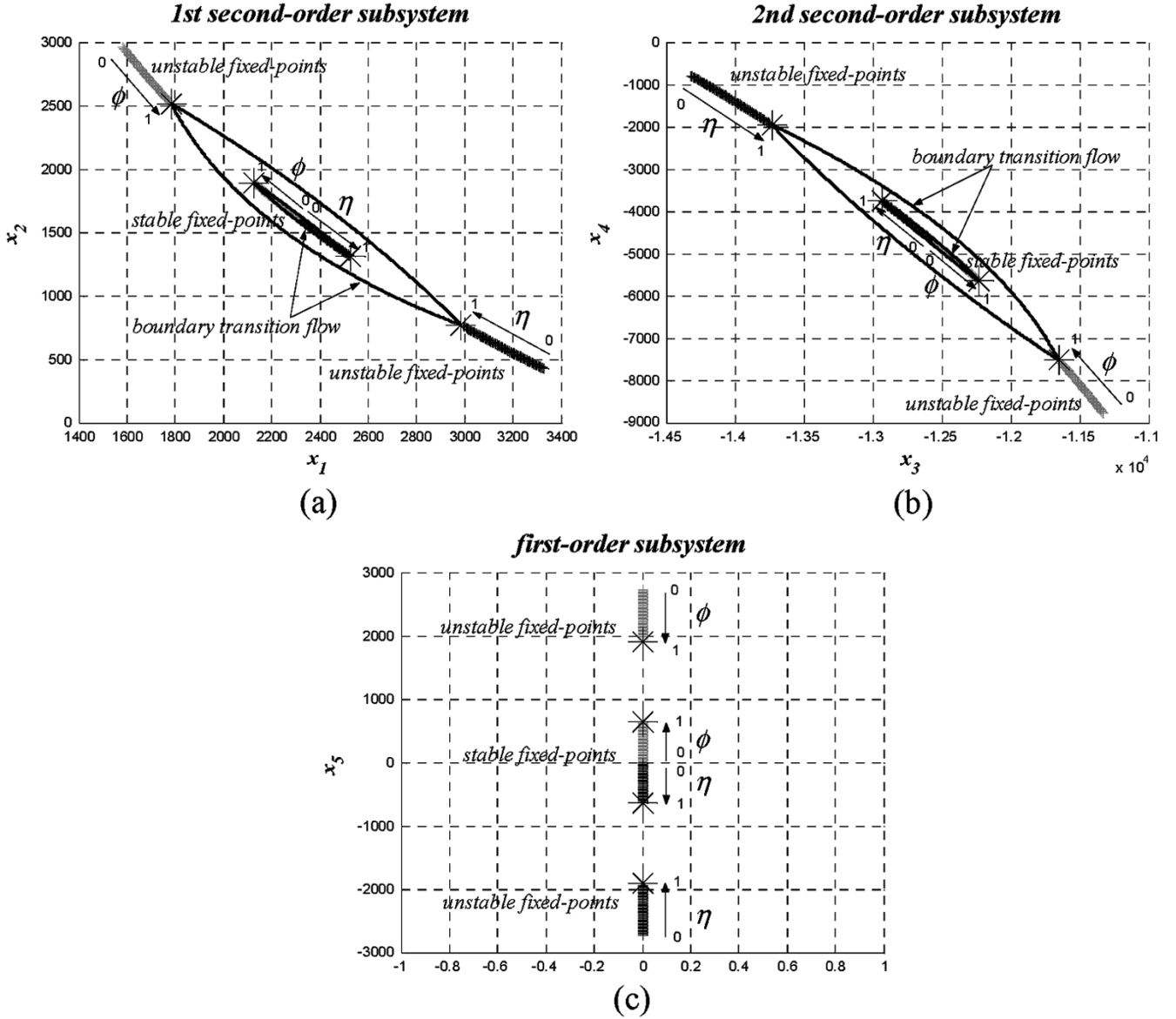


Fig. 1. Variation of fixed points against tilt factors for an example decomposed fifth-order $\Sigma\Delta$ modulator with optimized NTF zeros ($u = 0.48$, $\text{OSR} = 64$, maximum NTF gain = 1.5). The boundary transition flow is highlighted.

based on the variation of unstable embedded limit-cycle fixed points (which signify the bounds beyond which the state trajectory goes unstable) with the modulator input amplitude. Circuit implementation of the detection scheme can be simplified and only standard analog components are required. A novel feature of the scheme is that it exercises dynamic bounding of the states with respect to the input amplitude, i.e., the upper and lower bounds of the states are functions of the input. This ensures early detection of instability just upon its onset, which is critical when we consider that instability may be triggered by input amplitudes well below the dc bound. Consequently, the scheme prevents the “leaking” of unwanted tones into the output bit-stream and eliminates the need of digital compensation and/or correction (e.g., [9]) to remove the tones at later stages.

This paper is organized as follows. Section II reviews the embedded limit cycles obtained from the state-space decomposition of LP high-order single-bit $\Sigma\Delta$ modulators with distinct unit-circle NTF zeros. Attention is paid to the unstable limit

cycles beyond which the state trajectories become unbounded. Section III plots the variation of the theoretical state bounds against the input amplitude, thus leading to a scheme that detects instability upon its onset. The proposed scheme is then compared to the conventional bit pattern search scheme. Section IV discusses the simplification and circuit implementation of the scheme, followed by conclusion in Section V.

II. REVIEW OF CONTINUOUS-TIME EMBEDDED LIMIT CYCLES

Using the notations from [1], an LP high-order single-bit $\Sigma\Delta$ modulator having distinct NTF zeros on the unit circle can be represented by

$$\begin{cases} \rho \mathbf{x}^{(0)} = \mathbf{A}_z^{(0)} \mathbf{x}^{(0)} + \mathbf{b}_z^{(0)} u + \mathbf{a}_z^{(0)} v \\ y = b_0 u + \mathbf{d}_z^{(0)} \mathbf{x}^{(0)} \\ v = \text{sgn}(y) \end{cases} \quad (1)$$

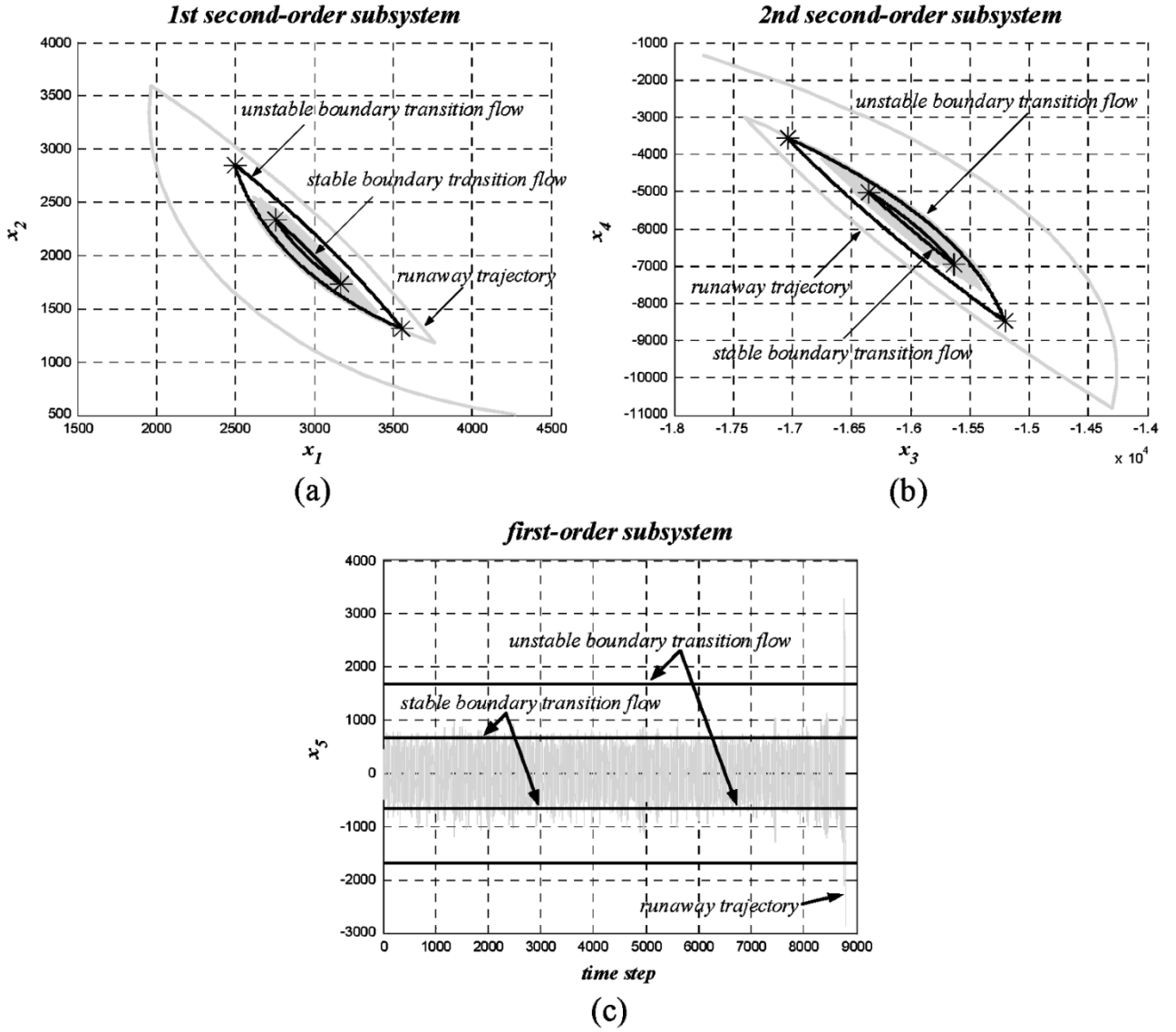


Fig. 2. Discrete state-trajectory plot for the example fifth-order $\Sigma\Delta$ modulator in Fig. 1 ($u = 0.61$ and zero initial condition, i.e., $\mathbf{x}^{(0)} = 0$). Instability occurs after about 8700 samples.

where $\rho = \mathbf{z} - 1$, $\mathbf{A}_z^{(0)}$, $\mathbf{b}_z^{(0)}$, $\mathbf{a}_z^{(0)}$, $\mathbf{d}_z^{(0)}$ and b_0 are the state matrices, u is the modulator input, v (either +1 or -1) is the quantizer output, and $\text{sgn}(\circ)$ is the sign function. It is shown that this system can be decomposed into second-order subsystems, plus an additional first-order subsystem for odd-order modulators. The transformation and translation relating the original state-vector $\mathbf{x}^{(0)}$ (the integrator outputs) to that in the transformed state space, \mathbf{x} , is quoted here

$$\mathbf{x} = (\mathbf{T}_d \mathbf{T}_R \mathbf{T}_n)^{-1} \mathbf{x}^{(0)} + \left[\frac{\tilde{\mathbf{A}}_c^{-1} \tilde{\mathbf{b}}_c}{0} \right] u. \quad (2)$$

Referring to [1], $\tilde{\mathbf{A}}_c^{-1} \tilde{\mathbf{b}}_c$ is a vector that contains the half-plane center information of all second-order subsystems, and the zero below the delimiter is only present in an odd-order modulator. Also, \mathbf{T}_d diagonalizes the transition matrix, \mathbf{T}_R transforms the state variables into real quantities, and \mathbf{T}_n rotates and scales the coordinate system of every subsystem such that the sum of their vertical coordinate components determines which half-plane,

corresponding to the two quantizer outputs, the trajectories are in.

In [1], Wang's embedded boundary transition flow [10], [11] is generalized to all types of transition flow with respect to the degree of penetration into the opposite half-plane, quantified by the positive and negative transition wedge tilt factors, ϕ and η , respectively [1, Sec. 2]. Fig. 1 shows an example fifth-order $\Sigma\Delta$ modulator in the transformed framework and illustrates the variation of the stable and unstable fixed points (also called foci and saddles in the second-order subsystems [12]) against different tilt factors. The worst case boundary transition flow limit cycles (corresponding to $\phi = \eta = 1$) are also highlighted. Fig. 2 shows the actual discrete trajectories going beyond the unstable fixed points and the associated limit cycles of the boundary transition flow, eventually losing stability. This is so because the Poincaré map analysis [1], [11] of these unstable fixed points results in eigenvalues of magnitudes greater than unity. The limit cycle thus formed will repel any state trajectory outside it while trajectories inside will generally be driven back to the inner stable

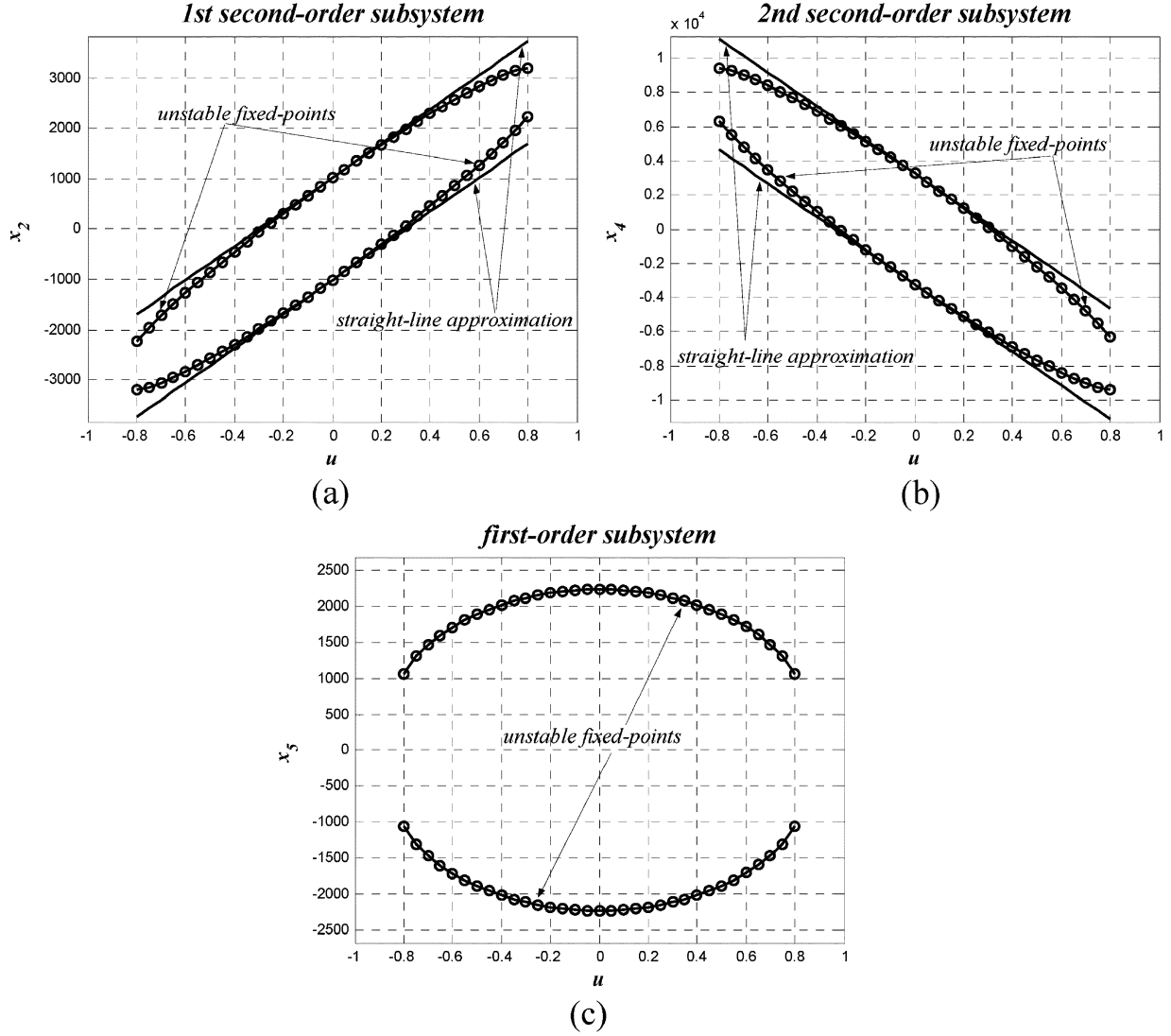


Fig. 3. Variation of unstable fixed points against the input u in the example fifth-order $\Sigma\Delta$ modulator.

limit cycles. In practice, the discrete nature of a $\Sigma\Delta$ modulator prevents its trajectories from falling exactly onto any embedded, continuous-time limit cycles. Adopting interpretation from [1], the discrete trajectories are constantly being attracted by different stable limit cycles but may still go unbounded, i.e., by-passing the unstable fixed points, due to extreme switching from one stable limit cycle to another. The figure also justifies the unstable boundary transition flow limit cycle as the worst case limit cycle because it is the most contracted one compared to others. Subsystem characteristics of other modulator orders show similar features, with the absence of the first-order subsystem in the case of even-order modulators.

III. INSTABILITY DETECTION

This section presents an instability detection scheme that theoretically detects unstable operation immediately upon its onset. Note that the unstable fixed points are functions of the input u . A set of loci can therefore be obtained when the unstable fixed points, in particular those of the unstable boundary transition flow, are plotted against u . Fig. 3 shows the case for the example

fifth-order $\Sigma\Delta$ modulator in Figs. 1 and 2. Since the change of state trajectory dynamics between opposite half-planes are determined by the vertical coordinate components of all subsystems [1, Sec. 3], stability can be inferred if the vertical components of all subsystems fall within the upper and lower bounds formed by the unstable fixed points of the boundary transition flow, e.g., x_2, x_4 , and x_5 of $\mathbf{x} = [x_1 \ x_2 \ \dots \ x_5]^T$ in our example, and x_2, x_4, \dots, x_N for a general N th-order modulator. In other words, instability can be detected when any one of these vertical coordinate components falls outside the bounds for a particular input u . A global reset or other recovery actions can then be issued to restore normal operation.

Fig. 4 shows the power spectra of the bitstream output in our fifth-order modulator example under a just-overloading sine wave of amplitude 0.62 situated at one quarter of the baseband. Fig. 4(a) is the spectrum without any recovery action and apparently the output is corrupted by erroneous tones. Fig. 4(b) and (c), respectively, shows the spectra for the proposed detection scheme and the traditional repetitive bit pattern search scheme, both coupled with a global integrator reset whenever instability is detected. It is seen that in this example, the proposed scheme

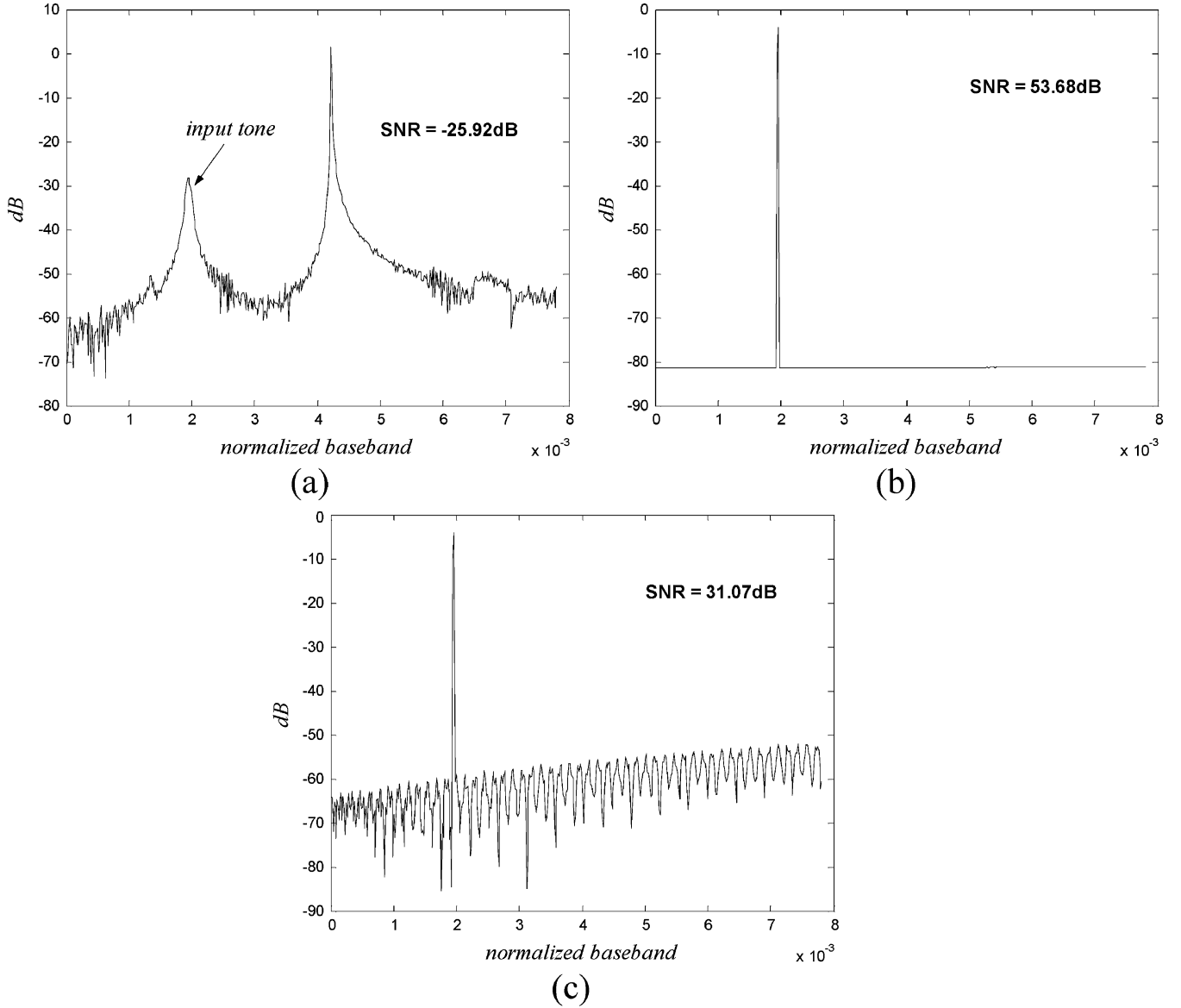


Fig. 4. FFT spectra of the bitstream output of the fifth-order $\Sigma\Delta$ modulator with a sine input (amplitude = 0.62, frequency = $(1/4)$ baseband). (a) No recovery schemes. (b) Proposed detect-and-reset scheme. (c) Pattern search detect-and-reset scheme triggered by 31 consecutive bits of the same sign.

outperforms the traditional one by more than 22 dB (>3.5 -bit resolution) in SNR. Due to the nature of the fast Fourier transform (FFT), the spectra in Fig. 4 measure the stationary, overall SNR. To investigate the dynamic SNR behavior versus time, a 2048-point Hanning window is slid across 2^{16} samples and the results are given in Fig. 5. It can be seen that the proposed scheme (also the simplified scheme that will be discussed) triggers one reset while the pattern search scheme triggers three. Other experiments also show that the proposed scheme is generally more effective in reducing unnecessary triggers, especially when the overloading level is just reached.

IV. IMPLEMENTATION AND SIMPLIFICATION

The realization of the detection scheme follows directly from (2) and is best illustrated through examples. The matrix $(\mathbf{T}_d \mathbf{T}_R \mathbf{T}_n)^{-1}$ contains only sparse elements. Also, only the even-number state variables (plus the last one for an odd-order

$\Sigma\Delta$ modulator) are involved since the check is performed only for the vertical coordinate components of every subsystem. For instance, in the case of the fifth-order modulator in Fig. 1 with optimized NTF zeros, maximum NTF gain 1.5, and OSR = 64, we obtain (3) shown at the bottom of the next page. Under the same set of constraints, a fourth- and a third-order modulator give (4a) and (4b) shown at the bottom of the next page. Now, say, to ensure x_2 in (3) falls within the bounds given by the unstable fixed-point loci, it is required that

$$\begin{aligned} \text{lower_bound}_i(u) &\leq x_1^{(0)} - 781.43x_3^{(0)} + 394995x_5^{(0)} \\ &\quad + 3327.6u \leq \text{upper_bound}_i(u) \end{aligned} \quad (5)$$

where $\text{upper_bound}_i(u)$ and $\text{lower_bound}_i(u)$ denote the upper and lower bounds of the i th subsystem, i.e., the bounds in Fig. 3(a) for the first second-order subsystem ($i = 1$) in (5). Direct implementation of this detection scheme is, however, hard to realize due to the nonlinear and curved nature of the

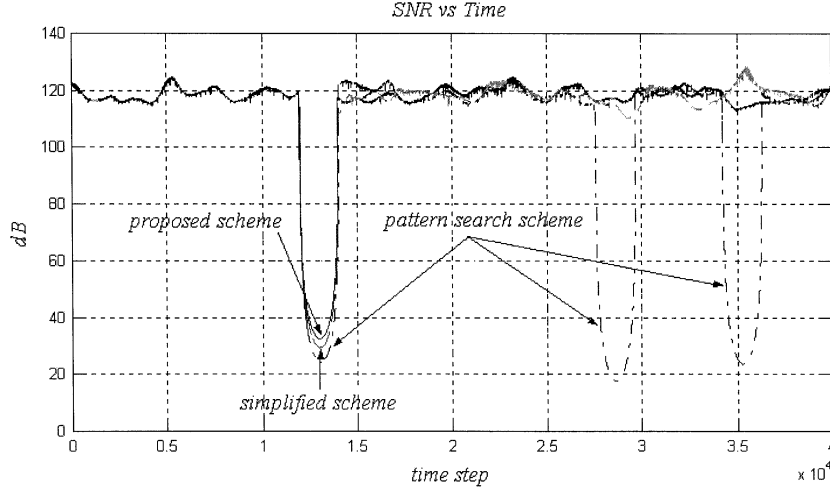


Fig. 5. Dynamic SNR performance for different detect-and-reset schemes (same input as in Fig. 4). The wide troughs are due to smearing effect of the FFT window, actual recovery of SNR takes just a few time steps, calculated by width of trough minus width of FFT window.

bounds' loci. This calls for approximation and simplification to the bounds. As is already shown in Fig. 3(a) and (b), this can be done by fitting straight lines tangent to the unstable fixed point loci. Subsequently, expressing $\text{upper_bound}_i(u)$ and $\text{lower_bound}_i(u)$ in their straight line equations, (5) reduces to

$$-1 \leq 9.836 \times 10^{-4} x_1^{(0)} - 0.7686 x_3^{(0)} + 388.51 x_5^{(0)} - 0.06019u \leq 1 \quad (6)$$

and similarly for the bounds in other subsystems. Moreover, only second-order subsystems need to be considered because simulation shows that unstable trajectories always cross the bounds in second-order subsystems prior to crossing those in the first-order subsystem. In fact, for the example in Fig. 4(b), the simplified, straight-line approximated detect-and-reset scheme suffers only less than half a bit of resolution loss compared to the original scheme.

In terms of hardware, the stability test in (6) can be incorporated into the modulator structure with additional gains, adders, comparators, and an OR gate. This is pictured in Fig. 6 for the fifth-order modulator in (3) in the popular cascade-of-resonators architecture. It should be noted that the original gain spread, namely, the ratio of the largest to the lowest gain (unbracketed numbers), is too large to be practical. By adjusting the gain stages after the switched capacitors, a scaled circuit (represented by bracketed gains) that attempts to equalize the root-mean-square values of all the capacitor outputs to about 0.4 is designed. The scaled circuit produces equivalent outputs as the unscaled prototype but the gain spread is now largely reduced for practical realization (in fact, gain spread can be further lowered by allowing larger capacitor swings). In Fig. 6, the two summing nodes before the comparators are usually implemented using operational amplifiers. This represents a tradeoff between fast instability detection and additional analog components (and thus power and area). The plots in Fig. 7 show the stationary SNR for

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \end{bmatrix} = \begin{bmatrix} -0.0222 & 22.488 & 17.383 & -17.573 & -8786.5 \\ 1 & 0 & -781.43 & 0 & 394.995 \\ 0 & 0 & -10.328 & 29.567 & 14.784 \\ 0 & 0 & 781.43 & 0 & -1.118.542 \\ 0 & 0 & 0 & 0 & 723.547 \end{bmatrix} \begin{bmatrix} x_1^{(0)} \\ x_2^{(0)} \\ x_3^{(0)} \\ x_4^{(0)} \\ x_5^{(0)} \end{bmatrix} + \begin{bmatrix} 4831.7 \\ 3327.6 \\ -26.185 \\ -9781 \\ 0 \end{bmatrix} u \quad (3)$$

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} = \begin{bmatrix} -0.0211 & 23.664 & 14.017 & -15.692 \\ 1 & 0 & -663.11 & 0 \\ 0 & 0 & -5.533 & 39.735 \\ 0 & 0 & 663.11 & 0 \end{bmatrix} \begin{bmatrix} x_1^{(0)} \\ x_2^{(0)} \\ x_3^{(0)} \\ x_4^{(0)} \end{bmatrix} + \begin{bmatrix} -854.73 \\ 2125.07 \\ 2205.16 \\ -14.524 \end{bmatrix} u \quad (4a)$$

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} -0.0190 & 26.306 & 13.153 \\ 1 & 0 & -691.77 \\ 0 & 0 & 691.77 \end{bmatrix} \begin{bmatrix} x_1^{(0)} \\ x_2^{(0)} \\ x_3^{(0)} \end{bmatrix} + \begin{bmatrix} -784.41 \\ -168.15 \\ 0 \end{bmatrix} u \quad (4b)$$

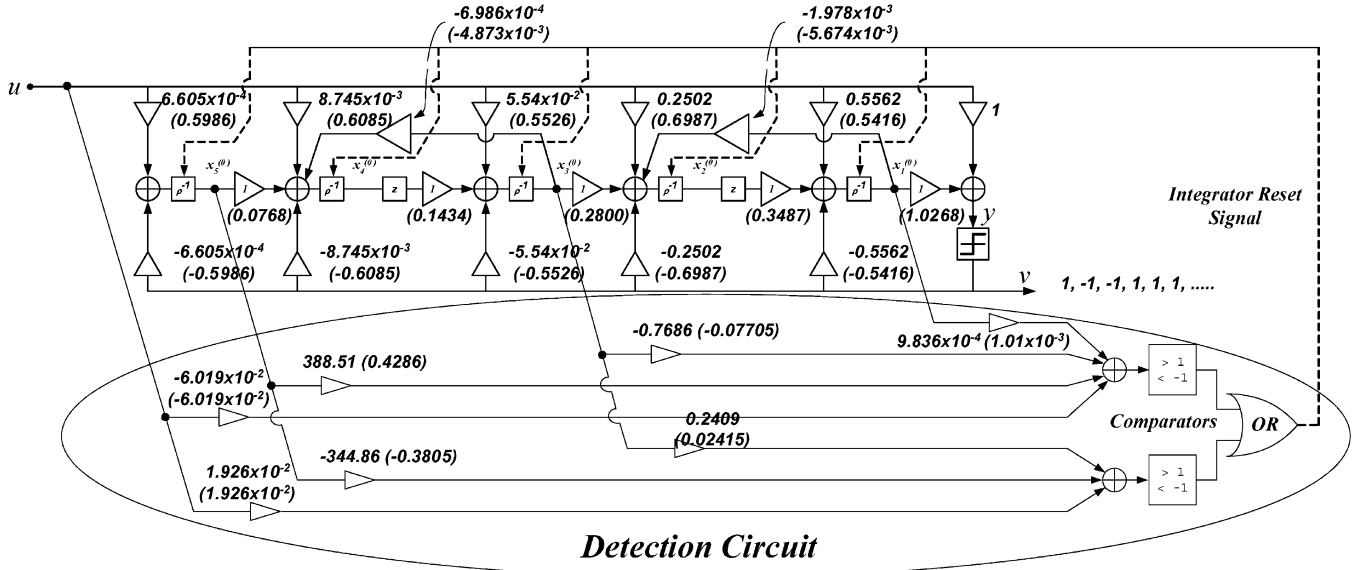


Fig. 6. Instability detection circuit (straight-line approximation) in the example fifth-order $\Sigma\Delta$ modulator. Bracketed gains denote scaled values for practical implementation.

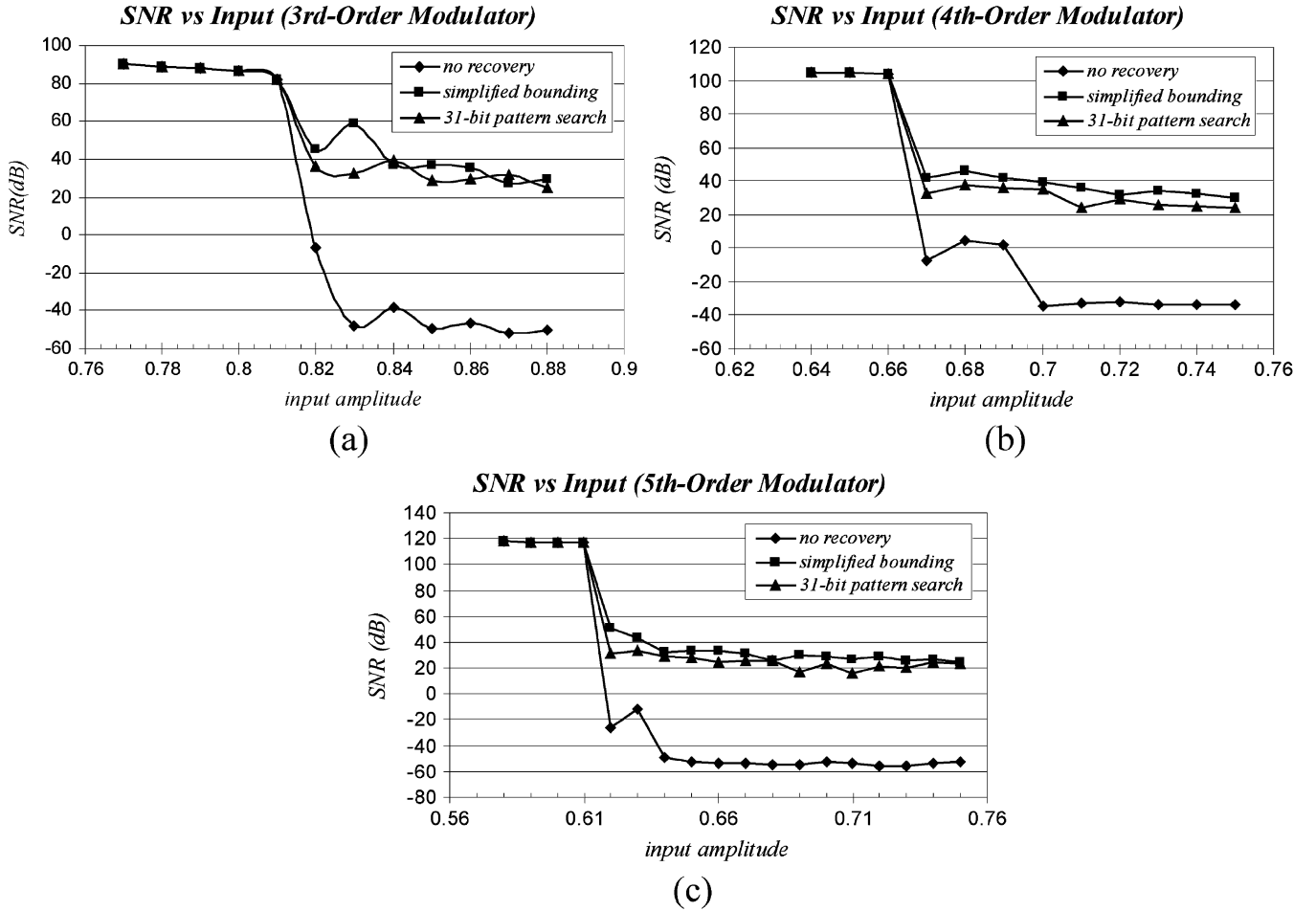


Fig. 7. SNR versus input amplitude of a sine wave located at one quarter of the baseband. (a) Third-order example. (b) Fourth-order example. (c) Fifth-order example.

the simplified scheme against that of the pattern search scheme in third-, fourth-, and fifth-order $\Sigma\Delta$ modulators for some overloading sine input, wherein a global reset is issued upon detection of instability. These results show consistent SNR improvement in

the simplified scheme (on average > 7 dB) over the pattern search scheme. A residual SNR of around 30 dB can be maintained even during unstable operation. Also, at the expense of some SNR loss, the detection circuit can be further simplified by detecting

the state boundedness of only one second-order subsystem. Examining Fig. 3, the discrepancy in the straight-line approximation is bigger at larger input magnitudes. While this is not a concern during normal operation when u is within its nominal range, a big momentary jump in u during power-up may result in a slower detection of instability. This can be circumvented by a forced reset just after start-up, or by combining the proposed scheme with digital pattern search to achieve robust detection.

In summary, by addressing the dependence of stability on both modulator input and integrator levels, the proposed (simplified) scheme reacts faster than conventional approaches that rely on modulator output and/or integrator levels.

V. CONCLUSION

This paper has presented an effective scheme for the fast detection of instability in an LP high-order single-bit $\Sigma\Delta$ modulator with distinct NTF zeros on the unit circle. The scheme is based on a strong theoretical ground wherein the idea of unstable fixed point loci of embedded limit cycles is utilized. Specifically, state-space trajectory bounds related to instability onset have been derived as a function of the modulator input amplitude. Faster instability detection comes at the expense of additional analog components in the hardware implementation, but simplification has been shown to be possible. Examples have demonstrated that the proposed scheme generally performs better than the conventional method of repetitive bit pattern search, and maintains a relatively high overall SNR even during unstable operation.

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