A Study on the Electrical Characteristics of InGaZnO Thin-Film Transistor with HfLaO Gate Dielectric Annealed in Different Gases

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Abstract

The effects of dielectric-annealing gas (O_2, N_2 and NH_3) on the electrical characteristics of amorphous InGaZnO thin-film transistor with HfLaO gate dielectric are studied in-depth, and improvements in device performance by the dielectric annealing are observed for each gas. Among the samples, the N_2-annealed sample has a high saturation carrier mobility of 35.1 $cm^2/V{\cdot}s$, the lowest subthreshold swing of 0.206 V/dec and a negligible hysteresis. On the contrary, the O_2-annealed sample shows poorer performance (e.g. saturation carrier mobility of 15.7 $cm^2/V{\cdot}s$, larger threshold voltage, larger subthreshold swing of 0.231 V/dec and larger hysteresis), which is due to the decrease of electron concentration in InGaZnO associated with the filling of oxygen vacancies by oxygen atoms. Furthermore, the NH_3-annealed sample displays the lowest threshold voltage (1.95 V), which is attributed to the increased gate-oxide capacitance and introduced positive oxide charges. This sample also reveals a change in the dominant trap type due to the over-reduction of acceptor-like border and interface traps, as demonstrated by a hysteresis phenomenon in the opposite direction. Lastly, the low-frequency noise of the samples has also been studied to support the analysis based on their electrical characteristics.

Keywords

Amorphous InGaZnO (a-IGZO), thin-film transistor (TFT), HfLaO, high-k, annealing gas.

1. Introduction

Amorphous InGaZnO (a-IGZO) thin-film transistors (TFTs) have been widely investigated for the application in the field of display technology due to their excellent electrical and physical characteristics, such as higher saturation carrier mobility (μ_{sat}, normally higher than 10 $cm^2/V{\cdot}s$) than amorphous silicon TFTs, superior uniformity of device performance compared with polycrystalline silicon TFTs, and better transparency to visible light than silicon-based devices [1], [2]. In addition, processing temperature below 400 °C is another advantage of a-IGZO TFTs [1].

However, it is still necessary to reduce the operating voltage of a-IGZO TFTs in order to meet the requirement of low energy consumption in novel portable devices. Accordingly, researchers tried to adopt various high-k materials as the gate dielectric in a-IGZO TFTs so that both high on-current and low threshold voltage (V_{TH}) can be guaranteed [3-5]. Nevertheless, the device performance of a-IGZO TFTs is also greatly affected by the film quality of the gate dielectric. As far as the film quality of high-k material is concerned, annealing at high temperature is one of the most effective methods for improving it [6]. However, little has been studied about the effects of annealing the high-k gate dielectric on the performance of a-IGZO TFTs.

In this work, the influence of post-deposition annealing (PDA) gas for the high-k gate dielectric on the electrical characteristics of a-IGZO TFTs is studied. Accordingly, three different annealing gases (oxygen, nitrogen and ammonia) have been adopted. In addition, a control sample without any annealing treatment on high-k gate dielectric is fabricated for comparison. In all the samples, HfLaO is selected as the gate dielectric due to its superior properties, including high dielectric constant, good thermal stability, low trap density and less Fermi-level pinning [7].

2. Experimental details

Fig. 1 shows the schematic diagram of a bottom-gate a-IGZO TFT with HfLaO gate dielectric. In this structure, P-type (100) silicon with a resistivity of 0.01 ~ 0.02 Ω·cm acts as both the substrate and gate electrode. Firstly, the conventional RCA (Radio Corporation of America) method was used to remove organic and ionic contaminants on the substrate. Secondly, deposition of a 40-nm HfLaO film was finished by means of a sputtering system with a radio-frequency (RF) power of 40 W and a metal target of HfLa (with 40% lanthanum). Moreover, the sputtering process was done in a mixed ambient of Ar plus O_2 (Ar : O_2 = 24 sccm : 6 sccm). Then, three samples were transferred into a furnace at 400 °C to receive an annealing treatment in an ambient of O_2, N_2 and NH_3, respectively for 10 min with a gas flow rate of 500 ml/min. Subsequently, the annealed samples together with a control sample (without annealing) received the deposition of a 60-nm IGZO active layer through RF sputtering from a ceramic target (Ga_2O_3 : In_2O_3 : ZnO = 1 : 1 : 1) in an Ar/O_2 mixed ambient. Then, a lift-off process was utilized to form the source/drain electrodes, which were composed of 20-nm Ti and 80-nm Au deposited by means of electron-beam evaporation. Finally, all the samples were annealed in a forming-gas (N_2 : H_2 = 95 : 5) ambient at 350 °C for 20 min so that the contact resistance of the source/drain electrodes can be reduced. In addition, metal-oxide-semiconductor capacitors were prepared to monitor the gate-oxide capacitance per unit area (C_{ox}). For each TFT device, the channel width (W) was 100 μm, and the channel length (L) was 20 μm. In addition, all the processing steps, except the annealings, were conducted at room temperature.

The current-voltage (I-V) of the TFTs and the 1-MHz capacitance-voltage (C-V) characteristics of the capacitors were measured by a HP 4145B semiconductor parameter analyzer and a HP4284A precision LCR meter, respectively. Furthermore, the low-frequency noise (LFN) of the TFTs was monitored by a Berkeley Technology Associates FET Noise

Analyzer Model 9603 combined with a HP 35665A Dynamic Signal Analyzer. Besides, the physical thicknesses of HfLaO and IGZO were measured by a multi-wavelength ellipsometer. All the measurements were conducted within a light-tight, electrically-shielded and room-temperature environment.

3. Result and discussions

Fig. 2 shows the transfer characteristics of the a-IGZO TFTs with different annealing gases (w/o annealing, O_2, N_2 and NH_3) for the HfLaO gate dielectric at a drain-to-source voltage (V_{DS}) of 5 V. Moreover, Fig. 2 (a) and Fig. 2 (b) refer to drain current (I_D) versus gate-to-source voltage (V_{GS}) and $I_D^{1/2}$ versus V_{GS}, respectively. Various electrical parameters of the devices, including μ_{sat}, V_{TH}, subthreshold swing (SS) and on-off current ratio (I_{on}/I_{off}), are extracted from Fig. 2 and listed in Table I. Among them, μ_{sat} and V_{TH} are calculated from a linear fitting to the plot of $I_D^{1/2}$ versus V_{GS}, which is based on the I-V equation for a field-effect transistor operating in the saturation region:

$$I_D = (\mu_{sat} C_{ox} W/2L)(V_{GS} - V_{TH})^2 \quad (1)$$

Compared with the control sample, each annealed sample possesses a steeper slope of $I_D^{1/2}$ versus V_{GS} in Fig. 2 (b), and accordingly a higher μ_{sat}. Also, V_{TH} is reduced by annealing the HfLaO gate dielectric in any of the three gases. Due to the improvements in μ_{sat} and V_{TH}, a higher on-current is observed in Fig 2 (a) for the three annealed samples, and correspondingly a larger I_{on}/I_{off} is achieved as well. Considering the fact that three different annealing gases have been adopted, it can be concluded that the improvement in electrical characteristics is partly attributed to the thermal effect of the annealing, which can induce the densification and/or surface modification of the HfLaO film. In addition, the subthreshold region shown in Fig. 2 (a) becomes steeper for the O_2- and N_2-annealed samples, and thus a smaller SS is obtained. This shows an effective suppression of trapping of channel electrons

due to the reduction of both the acceptor-like border traps (also called near-interface oxide traps) in HfLaO and the acceptor-like traps at the a-IGZO/HfLaO interface, further revealing the improvement in the film quality of HfLaO by the annealing.

However, among the annealed samples, the improvement in electrical characteristics is different. Firstly, it is observed that the O_2-annealed sample presents the lowest μ_{sat} (15.7 $cm^2/V{\cdot}s$), the highest V_{TH} (3.51 V) and the lowest I_{on}/I_{off} (2.5×10^6). It is believed that this lower device performance is ascribed to the incorporation of oxygen atoms into the HfLaO dielectric during the annealing in O_2. With more oxygen atoms, some oxygen vacancies ($\ddot{V}_O$) in HfLaO are filled. Moreover, oxygen atoms can diffuse through HfLaO into a-IGZO during the forming-gas annealing, thus filling up the oxygen vacancies in a-IGZO as well. It is well known that an oxygen vacancy tends to generate two free electrons as described by the defect equation of a-IGZO:

$$\text{a-IGZO} \rightarrow \frac{1}{2}O_2(g)\uparrow + \ddot{V}_O + 2e^- \qquad (2)$$

Accordingly, the filling of oxygen vacancies can decrease the electron concentration in a-IGZO, resulting in the degradation of electrical characteristics of TFTs [8]. Hence, although the improvement in device performance can be observed in the O_2-annealed sample as a result of the thermal effect during the dielectric annealing, the improvement is the smallest among the annealed samples. On the contrary, the inert N_2 ambient can effectively prevent the incorporation of oxygen during the annealing, thus avoiding the decrease of electron concentration in a-IGZO induced by the filling of oxygen vacancies. Therefore, the N_2-annealed sample has a higher electron concentration in a-IGZO than the O_2-annealed one. It is well known that for an n-type field-effect transistor, V_{TH} can be reduced by the increase of electron concentration in its semiconducting channel region. Also, an increase of electron concentration in a-IGZO is accompanied by a shift of the zero-gate-bias Femi level towards

the conduction band, resulting in the filling of a larger fraction of the acceptor-like a-IGZO/HfLaO interface traps and/or the acceptor-like traps in a-IGZO. Moreover, it is believed that a greater amount of acceptor-like border traps in HfLaO can also be filled by the increase of electron concentration in a-IGZO. As a result, the scattering of channel electrons by the traps can be further reduced, and correspondingly the carrier mobility can be increased [9]. Accordingly, the N_2-annealed sample possesses a higher μ_{sat} (35.1 $cm^2/V{\cdot}s$) and a smaller V_{TH} (3.29 V) than the O_2-annealing one, thus a larger I_{on}/I_{off} (5.1×10^6). Moreover, the increased filling of both border and interface traps in the N_2-annealed sample can also be revealed by its lower trap density N_t at/near a-IGZO/gate-dielectric interface than that of the O_2-annealed one, with N_t calculated from SS [10], [11]:

$$N_t = \left[\frac{SSlog(e)}{K_B T/q} - 1 \right] \frac{C_{ox}}{q} \qquad (3)$$

where k_B is the Boltzmann constant, q the electron charge, and T the temperature. Accordingly, N_t is 7.0×10^{12} cm^{-2}, 4.8×10^{12} cm^{-2} and 3.7×10^{12} cm^{-2} for the control, O_2- and N_2-annealed samples, respectively. Hence, the reduction of border and interface traps after dielectric annealing can be further demonstrated, and is more effective in the N_2-annealed sample than the O_2-annealed one. The C_{ox} of the O_2-annealed sample (0.264 $\mu F/cm^2$) is larger than that of the N_2-annealed one (0.241 $\mu F/cm^2$), which is due to the improved stoichiometry of the HfLaO gate dielectric after annealing in O_2. However, both values are smaller than that of the control sample, which is attributed to the formation of a SiO interlayer between HfLaO and the substrate during the annealing step. Accordingly, the effective oxide thickness (EOT) of the HfLaO dielectric is 13.0 nm, 13.1 nm and 14.3 nm for the control, O_2- and N_2-annealed sample, respectively.

As for the NH_3-annealed sample, the most noticeable property is the largest negative shift of V_{TH} among the annealed samples as shown in Fig. 2, and thus the smallest V_{TH} (1.95 V) is obtained. There are two factors which could contribute to such a large shift. On one hand, the nitrogen incorporation induced by the annealing in NH_3 can suppress the oxidation at the high-k material/substrate interface [12], and thus the growth of a low-k SiO interlayer between HfLaO and the silicon substrate, as supported by the highest C_{ox} (0.275 μF/cm^2) and the smallest EOT (12.6 nm) of the NH_3-annealed sample among the samples. As a result of the C_{ox} increase, the V_{TH} of the NH_3-annealed sample is reduced. Moreover, it is reported that positive charges can be introduced into oxide material by the active hydrogen dissociated from NH_3 [13], resulting in a further reduction of V_{TH}. In addition, it is found that the μ_{sat} of the NH_3-annealed sample (19.3 cm^2/V·s) is much lower than that of the N_2-annealed one, which should be due to the carrier scattering induced by the generated positive oxide charges. However, the highest I_{on}/I_{off} (6.0 ×10^6) among the samples can still be achieved by the NH_3-annealed sample due to the substantial reduction of V_{TH}.

As shown in Fig. 3, the hysteresis properties of the samples are also investigated based on the transfer characteristics under forward and reverse V_{GS} sweepings successively. ΔV_H, defined as the V_{TH} shift in the hysteresis loop, is extracted from Fig. 3 and listed in Table I. In Fig. 3 (a), the control sample exhibits an obvious clockwise hysteresis (ΔV_H = 1.78 V), which is attributed to the existence of a large amount of acceptor-like border and interface traps [14]. As shown in Fig. 3 (b) and Fig. 3 (c), the ΔV_H values of the O_2- and N_2-annealed samples are obviously reduced. Hence, it shows that dielectric annealing in O_2 or N_2 can effectively reduce the acceptor-like border and interface traps, which is consistent with the earlier discussion based on the subthreshold slope. Moreover, compared to the O_2-annealed sample (ΔV_H = 0.37 V), the N_2-annealed sample exhibits a negligible ΔV_H (-0.03 V), which reveals that the hysteresis could be almost completely eliminated by annealing the HfLaO gate

dielectric in N_2. Furthermore, the negative ΔV_H value of the N_2-annealed sample demonstrates that the dielectric annealing in N_2 can only reduce the acceptor-like, not donor-like, border and interface traps, and that the donor-like traps start to seize the dominant role as a result. As shown in Fig. 3(d), the NH_3-annealed sample (ΔV_H = -0.82 V) presents a hysteresis phenomenon in the opposite (counter-clockwise) direction, which clearly reveals a larger reduction of the acceptor-like traps and thus the dominant role of the donor-like ones. It is reported that nitrogen incorporation can create stronger bonds in oxide film by replacing the original weak oxygen-related bonds which can generate acceptor-like border and interface traps after being broken [15], [16]. This effect well explains the larger reduction of the acceptor-like border and interface traps observed in the NH_3-annealed sample than the N_2-annealed one. However, the NH_3-annealed sample shows a larger SS (0.315 V/dec) and higher N_t (7.4×10^{12} cm^{-2}) than the N_2-annealed sample, which could be attributed to the fact that the former has more donor-like border and interface traps.

As for the N_2- and NH_3-annealed samples, their unfilled donor-like border and interface traps can detrap electrons and/or trap holes under a negative gate bias at the beginning of forward V_{GS} sweeping. Consequently, the turn-off effect of TFT is weakened, and correspondingly a larger off-current at V_{GS} = -5 V shows up, as compared to the control and O_2-annealed samples. Moreover, this phenomenon is more obvious for the NH_3-annealed sample due to the existence of more donor-like border and interface traps induced by the NH_3 annealing. When the magnitude of the negative gate bias decreases for further forward V_{GS} sweeping, the unfilled donor-like border and interface traps in the N_2- and NH_3-annealed samples are reduced. So, the influence of donor-like traps on the turn-off effect becomes insignificant. Nevertheless, for the control and O_2-annealed samples, their dominant traps are acceptor-like, and thus there is no electron detrapping and/or hole trapping at the beginning

of forward V_{GS} sweeping. Therefore, the turn-off effect is not affected, as revealed by their smaller off-currents at V_{GS} = -5 V.

LFN measurement is conducted to compare the performance of the samples. As shown in Fig. 4, the normalized noise power spectral density (S_{iD}/I_D^2) is measured at a fixed gate overdrive voltage (V_{GS} - V_{TH}) of 3.0 V in the linear region (V_{DS} = 1.0 V) for each sample. Based on the measurement results, the Hooge's parameter (α_H), which reflects the level of LFN, is extracted according to the following equation:

$$S_{iD}/I_D^2 = \frac{\alpha_H q}{fWLC_{ox}|V_{GS}-V_{TH}|} \quad (4)$$

where f is the frequency, q the elementary electron charge [17], and is listed in Table I (12.1, 1.22, 0.08 and 0.16 for the control, O_2-, N_2- and NH_3-annealed samples respectively). It is reported that the LFN of MOSFETs is generally ascribed to the fluctuations of both carrier number and mobility induced by the traps in gate dielectric and at the interface of active layer/gate dielectric [18]. Since the noises of the annealed samples are smaller than that of the control sample, the effect of reducing acceptor-like border and interface traps by dielectric annealing is further supported. Furthermore, the N_2-annealed sample possesses smaller noise than the O_2-annealed one, indicating more effective reduction of acceptor-like border and interface traps, which is consistent with the previous analysis based on other electrical properties such as μ_{sat}, V_{TH}, SS and hysteresis. The NH_3-annealed sample also has relatively lower noise because of the effective reduction of acceptor-like border and interface traps by annealing HfLaO in NH_3. However, from the earlier analysis on the hysteresis property, a large amount of donor-like border and interface traps dominate the charge trapping in the NH_3-annealed sample, leading to a degradation of its noise performance as compared to the N_2-annealed sample.

Fig. 5 displays the output characteristics of the a-IGZO TFTs with different annealing gases for the HfLaO gate dielectric. N-type enhancement mode is clearly exhibited by each sample. Moreover, I_D increases linearly with V_{DS} in the region of low V_{DS}, and current saturation can be observed in the region of high V_{DS}. As a whole, the output current I_D can be increased by the dielectric annealing. In particular, the N_2- and NH_3-annealed samples, due to more prominent improvement in μ_{sat} and V_{TH}, present a larger output current than the O_2-annealed sample.

4. Conclusion

In this work, the impact of annealing gases (O_2, N_2 and NH_3) for HfLaO gate dielectric on the electrical characteristics of a-IGZO TFT has been investigated. It is found that the dielectric annealing, partly due to its thermal effect, can effectively enhance the device performance by improving the film quality of HfLaO, i.e. less acceptor-like border and interface traps. In particular, the inert N_2 ambient can avoid the decrease of electron concentration in a-IGZO associated with the filling of oxygen vacancies, resulting in a further reduction of acceptor-like border and interface traps by electron filling in the N_2-annealed sample. Accordingly, the N_2-annealed sample exhibits better performance (in μ_{sat}, V_{TH}, I_{on}/I_{off}, SS, hysteresis and output current) than the O_2-annealed one. Especially, both a high μ_{sat} (35.1 $cm^2/V{\cdot}s$) and negligible hysteresis (ΔV_H = -0.03 V) have been achieved by the N_2-annealed sample, and its SS and LFN are also the smallest among the samples. Furthermore, the lowest V_{TH} (1.95 V) is presented by the NH_3-annealed sample due to the combined influence of C_{ox} increase and generated positive oxide charges. Moreover, the dominant type of traps in the NH_3-annealed sample is different, which is due to over-reduction of acceptor-like border and interface traps as revealed by a hysteresis phenomenon in the opposite direction (ΔV_H = -0.82 V). In addition, the LFN measurement well supports the analysis about the reduction of acceptor-like border and interface traps based on other electrical properties.

Acknowledgements

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Captions:

Fig. 1. Schematic diagram of bottom-gate a-IGZO TFT with HfLaO gate dielectric.

Fig. 2. Transfer characteristics of the a-IGZO TFTs with different annealing gases (w/o annealing, O_2, N_2 and NH_3) for HfLaO gate dielectric at V_{DS} = 5 V: (a) I_D versus V_{GS}; (b) $I_D^{1/2}$ versus V_{GS}.

Fig. 3. Transfer characteristics of the a-IGZO TFTs measured under the forward (V_{GS} = -5 V to 10 V) and reverse (V_{GS} = 10 V to -5 V) sweepings with different annealing gases for HfLaO gate dielectric: (a) W/O-annealing; (b) O_2; (c) N_2; (d) NH_3.

Fig. 4. The plot of S_{iD}/I_D^2 versus frequency of the a-IGZO TFTs with different annealing gases (W/O-annealing, O_2, N_2 and NH_3) for HfLaO gate dielectric measured at V_{DS} = 1 V and V_{GS} - V_{TH} = 3 V.

Fig. 5. Output characteristics of the a-IGZO TFTs with different annealing gases for HfLaO gate dielectric: (a) W/O-annealing; (b) O_2; (c) N_2; (d) NH_3.

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Figure 1

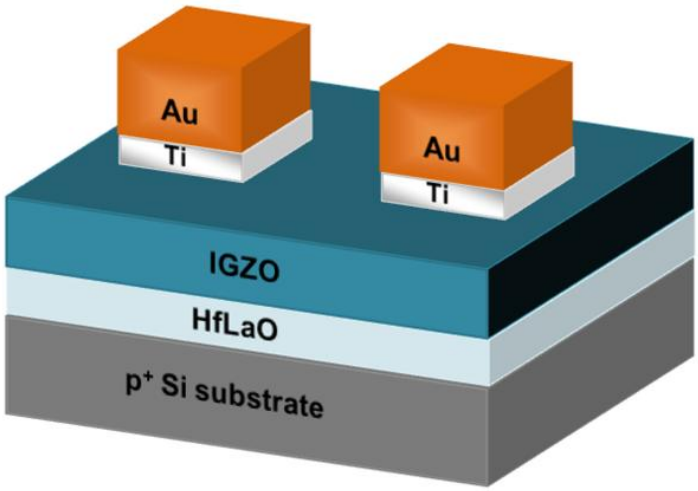

Fig. 1 by L. X. Qian

Figure 2

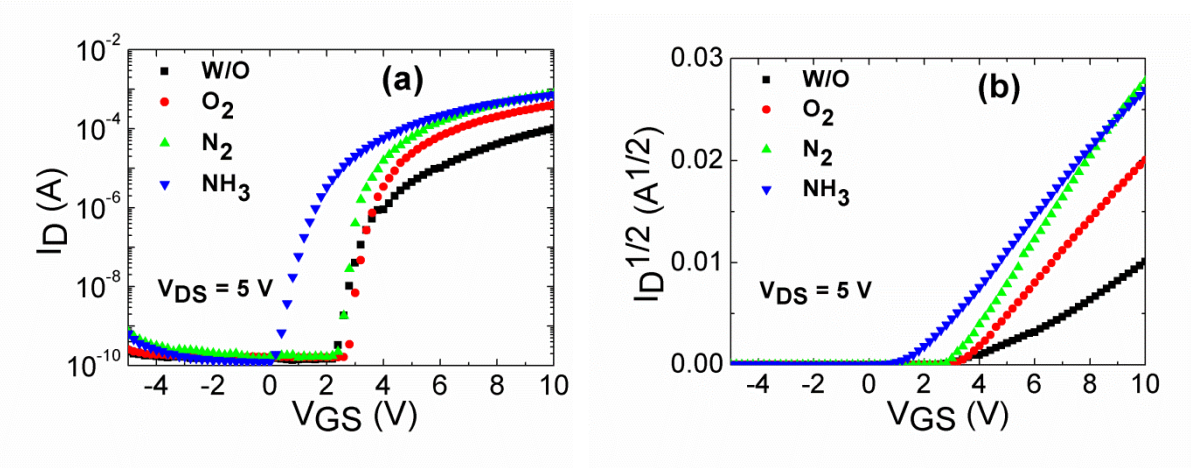

Fig. 2 by L. X. Qian

Figure 3

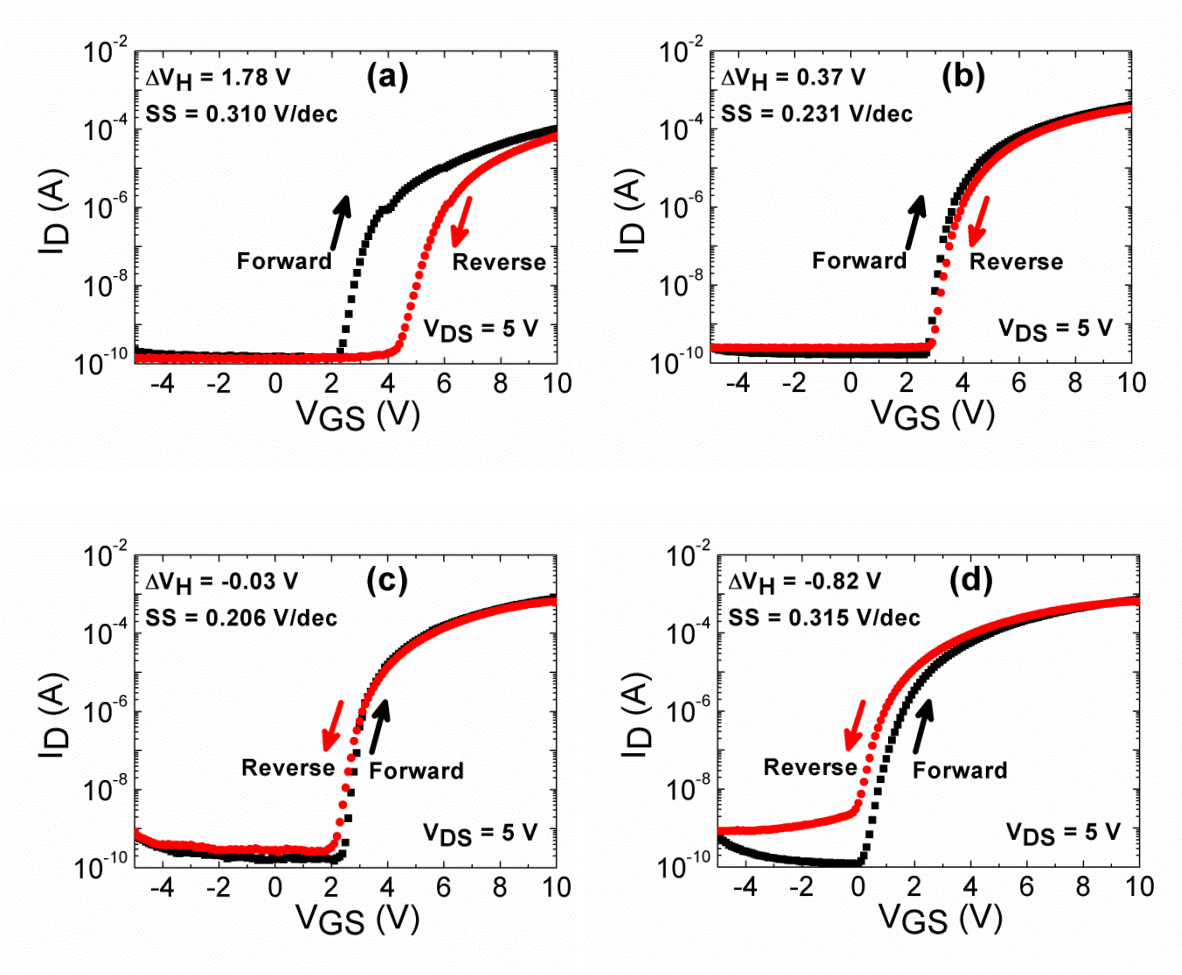

Fig. 3 by L. X. Qian

Figure 4

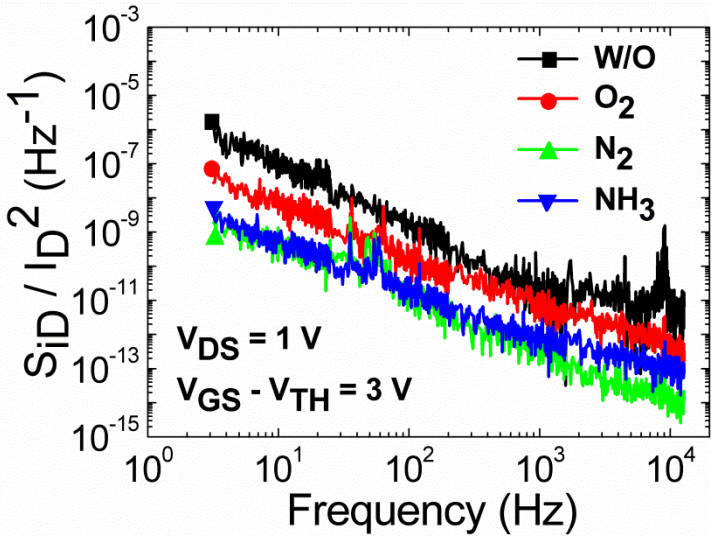

Fig. 4 by L. X. Qian

Figure 5

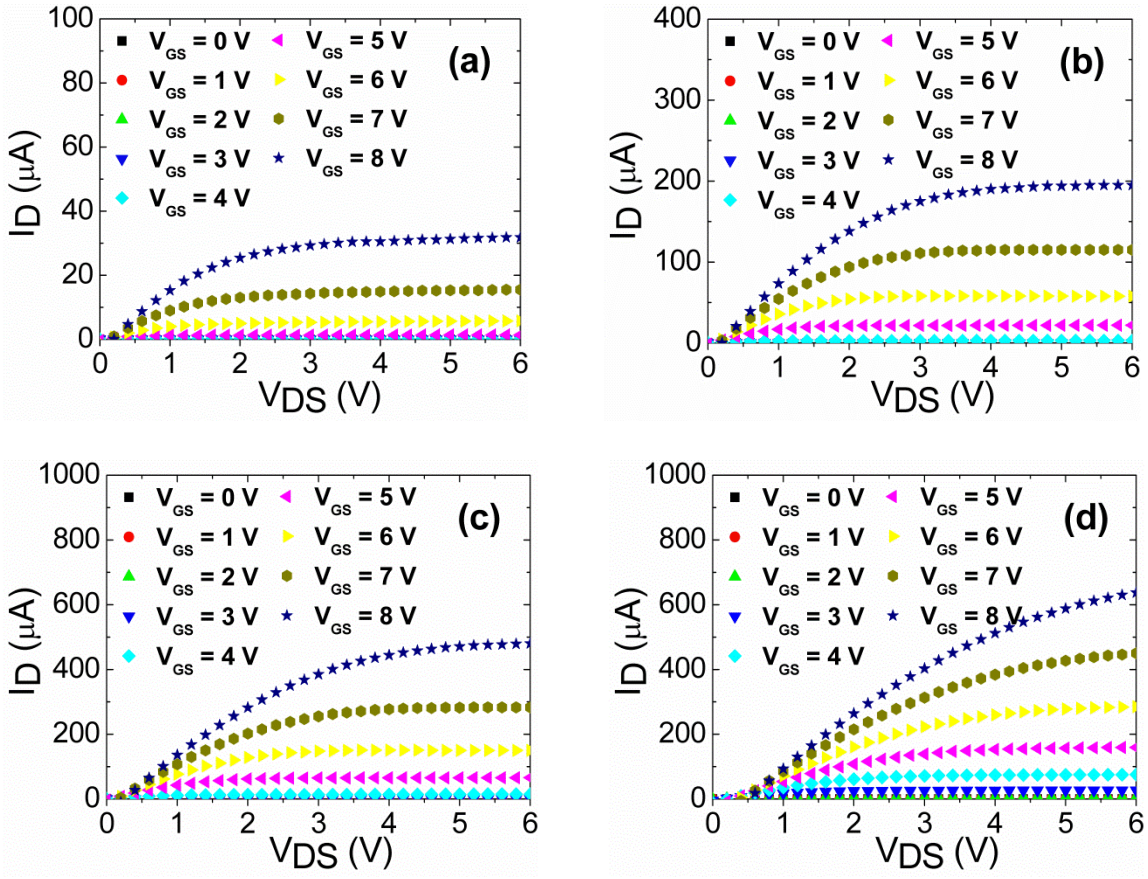

Fig. 5 by L. X. Qian

Table(s)

TABLE I
ELECTRICAL PARAMETERS EXTRACTED FROM THE CURVES IN FIG. 2, FIG. 3 AND FIG. 4

Annealing	μ_{sat} ($cm^2/V\cdot s$)	V_{TH} (V)	SS (V/dec)	N_t ($/cm^2$)	ΔV_H (V)	I_{on}/I_{off}	C_{ox} ($\mu F/cm^2$)	EOT (nm)	α_H
W/O	4.3	4.26	0.310	7.0×10^{12}	1.78	7.5×10^{5}	0.266	13.0	12.1
O_2	15.7	3.51	0.231	4.8×10^{12}	0.37	2.5×10^{6}	0.264	13.1	1.22
N_2	35.1	3.29	0.206	3.7×10^{12}	-0.03	5.1×10^{6}	0.241	14.3	0.08
NH_3	19.3	1.95	0.315	7.4×10^{12}	-0.82	6.1×10^{6}	0.275	12.6	0.16