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Improved Charge-Trapping Performance of Hf-doped SrTiO₃ for Nonvolatile Memory Applications

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The charge-trapping characteristics of Hf-doped SrTiO₃ have been studied based on Al/Al₂O₃/Hf-doped SrTiO₃/SiO₂/Si capacitors. The thermodynamic stability of the SrTiO₃ film is significantly improved by Hf incorporation, thus resulting in negligible formation of an interlayer at the Hf-doped SrTiO₃/SiO₂ interface, as confirmed by X-ray photoelectron spectroscopy and transmission electron microscopy. The memory device with Hf-doped SrTiO₃ as charge-trapping layer displays high speed at low operating voltage (a $V_{FB}$ shift of 1.9 V at +6 V, 100 μs) and good data retention (charge loss of 12.7% after $10^4$ s). Therefore, the Hf-doped SrTiO₃ film is a promising material as charge-trapping layer for high-performance nonvolatile memory applications.

Introduction

Metal-oxide-nitride-oxide-silicon (MONOS) nonvolatile memories with traps distributed in the dielectrics for charge storage have been considered as a better candidate than their conventional floating-gate counterpart due to their localized charge-storage and coupling-free properties. Intensive researches have been carried out to study high-$k$ dielectrics for substituting Si₃N₄ as charge-trapping layer (CTL) mainly due to the stronger scaling ability, lower operating voltage and higher charge-trapping efficiency. In our previous work, SrTiO₃ was demonstrated to be a promising CTL for low-voltage MONOS memory applications due to its high-$k$ value as well as large band offset with respect to the SiO₂ tunneling oxide (1). However, this memory device with SrTiO₃ as CTL displayed severe charge loss mainly due to its poor thermodynamic stability with SiO₂, which resulted in a thick non-stoichiometric interlayer at the SrTiO₃/SiO₂ interface. It was also found that this interlayer could be significantly suppressed by inserting HfON between SrTiO₃ and SiO₂, leading to better data retention (2). However, the insertion of HfON increases the processing complexity of the memory device. Additionally, the operating speed and operating voltage of the devices mentioned above need to be further improved (1)(2). Therefore, in order to achieve excellent performance for the SrTiO₃-based memory device with good retention as well as high speed at low operating voltage, this work aims to investigate the charge-trapping characteristics of Hf-doped SrTiO₃ made by co-sputtering technique.
Experiment

MONOS capacitor with an Al/Al₂O₃/Hf-doped SrTiO₃/SiO₂/Si structure was fabricated. SiO₂ as tunneling layer (TL) was grown on the p-type Si by thermal oxidation. Then, Hf-doped SrTiO₃ film as CTL was prepared by co-sputtering of Hf and SrTiO₃ targets in an Ar/O₂ mixed ambient. Following that, Al₂O₃ as blocking layer (BL) was deposited by atomic layer deposition using Al(CH₃)₃ and H₂O as precursors at 300 °C. Finally Al was evaporated and patterned as gate electrode, followed by forming-gas annealing at 300 °C for 20 min. The cross-sectional transmission electron microscopy (TEM) image of the completed MONOS device is shown in Figure 1(a).

Results and Discussion

Figures 1(b) and 1(c) show the Si 2p spectrum as well as the curve-fitting lines for Hf-doped SrTiO₃/SiO₂ and SrTiO₃/SiO₂ on Si substrate by X-ray photoelectron spectroscopy (XPS). Each curve-fitting line is assumed to follow the general shape of Lorentzian–Gaussian function. Both of the Si 2p spectra can be decomposed into two components, and correspond to SiO₂ tunneling oxide (103.6 eV) and Ti silicate (102.3 eV) at the CTL/TL interface formed by chemical reaction respectively (3)(4). Note that the area ratio of Si component corresponding to SiO₂ and silicate is 36 for the sample with Hf-doped SrTiO₃, which is much larger than that for the sample with pure SrTiO₃ (5.0), suggesting a much thinner interlayer at the interface achieved by Hf doping due to the good thermodynamic stability of hafnium oxide contacted with SiO₂ (5). This observation can be further confirmed by the TEM image in Figure 1(a) with no interlayer observed at the CTL/TL interface. Therefore, Hf incorporation can effectively improve the thermodynamic stability of SrTiO₃.

![TEM image of the MONOS device](image1.png)

*Figure 1. (a) TEM image of the MONOS device, and the thickness of BL/CTL/TL is 15.7 nm/4.3 nm/2.8 nm. (b) Si 2p spectrum of the Hf-doped SrTiO₃/SiO₂ on the Si substrate. (c) Si 2p spectrum of the SrTiO₃/SiO₂ on the Si substrate.*

Fig. 2 shows the program/erase (P/E) transient characteristics of the MONOS device with Hf-doped SrTiO₃ as CTL. As the operating voltage V_G increases from +6 V to +10 V with a pulse width of 1 ms, the V_FB shift (ΔV_FB) increases from 2.2 V to 5.3 V. The device shows higher ΔV_FB (5.3 V at V_G = 10 V, 1 ms) than the device with SrTiO₃ (ΔV_FB
= 3.2 V at $V_G = 10$ V, 1 ms) or SrTiO$_3$/HfON ($\Delta V_{FB} = 2.9$ V at $V_G = 10$ V, 1 ms) as CTL under the same operating conditions, even though the former has a thicker TL (2.8 nm) than the latter (2.0 nm) (2). This should be due to the better interfaces of the dielectric stack and more traps in the CTL induced by Hf incorporation in SrTiO$_3$, thus resulting in higher charge-trapping efficiency for the device with Hf-doped SrTiO$_3$. Moreover, the proposed device presents a high $\Delta V_{FB}$ of 1.9 V even at a low $V_G$ of +6 V for 100 μs under program state and a high $\Delta V_{FB}$ of 3.6 V at $V_G$ of -8 V for 100 μs under erase state, demonstrating its high P/E speeds with low-voltage operating ability.

![Figure 2](image1.png)

(a)

![Figure 2](image2.png)

(b)

Figure 2. (a) Program and (b) erase transient characteristics of the memory device with Hf-doped SrTiO$_3$ at various gate voltages.

Figure 3 exhibits the retention characteristics of the device with Hf-doped SrTiO$_3$ as CTL, which shows good data retention with low charge-loss rate (the charge loss rate $Q_{loss}$ after $10^4$ s is 12.7%). As shown in the inset of Figure 3, the device with Hf-doped SrTiO$_3$ exhibits similar $Q_{loss}$ as the one with SrTiO$_3$/HfON ($Q_{loss} = 12.3$ %), and both devices exhibit much better data retention than the one with SrTiO$_3$ ($Q_{loss} = 50.2$ %) (2). This should be mainly due to the suppressed formation of interlayer at the CTL/TL interface because the interlayer consumes part of the SiO$_2$ tunneling oxide (thus shortening the leakage path from the CTL to the substrate) and also traps in the non-stoichiometric interlayer usually facilitate charge loss via trap-assisted tunneling.
The charge-trapping characteristics of Hf-doped SrTiO\textsubscript{3} have been studied. The thermodynamic stability of the SrTiO\textsubscript{3} film can be improved by Hf incorporation. The memory device with Hf-doped SrTiO\textsubscript{3} as CTL displays high P/E speeds at low operating voltage and good data retention. Therefore, the Hf-doped SrTiO\textsubscript{3} film is a promising material as CTL for MONOS-type memory applications.

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