Negative gate-bias instability of ZnO thin-film transistors studied by current–voltage and capacitance–voltage analyses

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Effects of negative gate-bias stress on the electrical properties of ZnO thin-film transistors (TFTs) are investigated. Under negative gate-bias stress, the ZnO TFTs exhibit higher carrier mobility, larger OFF-state current, and a negative shift in threshold voltage with no significant change in subthreshold slope. The time dependence of threshold-voltage shift on various bias stress conditions can be described by a logarithmic equation. Based on the analysis of hysteresis behaviors in current–voltage and capacitance–voltage characteristics before and after the negative gate-bias stress, it can be clarified that the threshold-voltage shift is predominantly attributed to the trapping of positive charge carriers in the defect states at the gate-dielectric/channel interface or in the dielectric during the negative gate-bias stress. © *2014 American Vacuum Society*.
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I. INTRODUCTION

Recently, ZnO-based thin-film transistors (TFTs) have attracted considerable attention as alternatives to silicon-based TFTs due to their high carrier mobility, low processing cost, high transparency, and low-temperature processing as compared to conventional amorphous silicon and organic TFTs,[1–3] and thus are particularly suitable for driving high-resolution liquid-crystal displays and organic light-emitting-diode pixels.[4,5]

For switching or driving transistors in commercial active-matrix liquid-crystal displays (AMLCD) or active-matrix organic light-emitting-diode (AMOLED) flat-panel displays, it is crucial to overcome the problem of bias-voltage-dependent instability because any shift in the threshold voltage of the driving transistor under on- or off-bias stress conditions will cause a change in its output drain current, thus leading to variation in the brightness of the relevant pixel. Since the total stress time of the negative gate bias is more than 500 times that of the positive gate bias for AMLCD and AMOLED applications, device degradation due to negative gate-bias instability is a critical issue that must be addressed. So far, several studies on bias-induced instabilities in ZnO-based TFTs have reported deterioration in their electrical characteristics,[6,7] and some methods have been used to suppress the bias-induced instability, e.g., Hf, Sn, and Al dopings, annealing treatment in nitrogen ambient.[8,9] Moreover, several mechanisms have been proposed to explain the bias-induced instability, such as charge trapping or defect-state creation in the gate dielectric or at the gate dielectric/channel interface. However, since these mechanisms were developed only from the output and transfer characteristics of ZnO-based TFTs,[10,11] there are not enough experimental results to support these deductions. In this work, the electrical instabilities of radio-frequency (RF)-sputtered ZnO TFT are investigated under negative gate-bias stress. In particular, the mechanism of the threshold-voltage shift is further clarified based on the analysis of hysteresis behaviors in current–voltage and capacitance–voltage characteristics before and after the negative gate-bias stress.

II. EXPERIMENTAL SECTION

The characterization of the devices was performed on bottom-gate top-contact structure, where a heavily doped n-type silicon wafer acted as both the substrate material and gate contact. A 100 nm thick SiO_2 was formed as the gate-oxide layer by thermal oxidation, and a 110-nm ZnO active layer was deposited on the SiO_2 layer using RF magnetron sputtering with ceramic ZnO target (99.999%, purity). The sputtering process was carried out at a base pressure of 4×10^{-4} Pa, a substrate temperature of 300 °C, and a RF power of 60 W. The mixing gas ratio of O_2/Ar was 2/5 with a working pressure of 0.5 Pa. Aluminum was then thermally evaporated through a shadow mask to form the source/drain (S/D) electrodes of the transistor. The channel width (W) and length (L) of the device were defined as 600 and 50 μm, respectively.

The thicknesses of the silicon oxide and ZnO thin film were measured by spectroscopic reflectometer. X-ray diffraction measurements were performed using Cu–Ka radiation (*Bruker D8 ADVANCE* diffractometer). The electrical properties of ZnO TFT devices were measured in air using an Agilent 4156C semiconductor parameter analyzer. Capacitance–voltage (C-V) measurements were performed by using a conventional LCR meter (Agilent 4284A) before and after a fixed-bias stress. To evaluate the effects of the negative gate-bias stress on the electrical properties of the

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devices, their transfer characteristics needed to be measured periodically during the stress experiments, and fast measurements and a small number of measured points per transfer curve were required to minimize the influence of the measurement process on the overall bias stress experiments. Since the bias-stress instability was recoverable after removal of the bias for several hours,[12] to avoid the variations among different devices, all the bias-stress measurements were performed on the same device, and the device was kept in dark and dry air for more than 4 h during stress recovery according to relaxation measurement after stressing for our sample as shown in Fig. 5.

III. RESULTS AND DISCUSSION

Figure 1 shows the x-ray diffraction pattern of the RF-sputtered ZnO thin film. Only the ZnO (002) peak at $2\theta = 34.18°$ is observed, revealing that the film is polycrystalline with a hexagonal structure and a preferred orientation with the c-axis perpendicular to the substrate. The full width at half maximum (FWHM) of diffraction peak usually reflects the grain size in the material. According to the Sherrer formula $D = 0.89\lambda/(B \cdot \cos\theta)$ (where D is the grain size; λ is the wavelength *of* x-ray; B is FWHM of the (002) peak; and θ is the diffraction angle), the grain size of the ZnO film can be calculated to be about 40 nm.

In order to test the electrical instability of the ZnO TFT under negative gate-bias stress, various negative gate biases are applied to the gate electrode with the source and drain connected to the ground ($V_{DS} = 0$ V). Figure 2 shows the evolution of typical transfer characteristics of the ZnO TFT at drain voltage of 20 V after subjected to a negative gate-bias voltage of −20 V for different stress times at room temperature and the change of the gate leakage current before after stressing. It can be observed that there is a clear shift of the transfer curve in the negative direction, and the shift is from rapid to slow with increasing stress time. The OFF-state current increases with increasing stress time. This is because the negative gate bias can attract positively charged holes in ZnO to the ZnO/SiO_2 interface, and they are then trapped by the interface state. At the same time, the ionized oxygen vacancies (V_O^{2+}) in ZnO are also attracted by the negative gate bias to the ZnO/SiO_2 interface[13] and increase

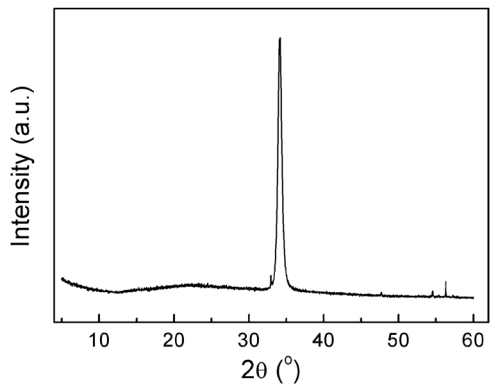

FIG. 1. Typical x-ray diffractogram of the RF-sputtered ZnO film.

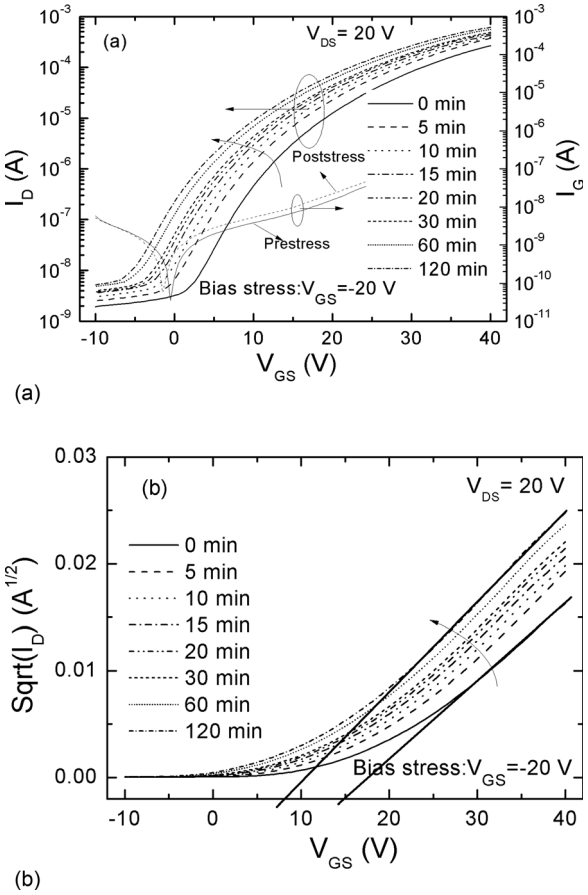

FIG. 2. Transfer characteristics of the ZnO TFT at drain voltage of 20 V for variable stress times under the gate-bias stress of $V_{GS} = -20$ V, and the change of the gate leakage current before and after stressing. (a) $\log(I_D)$–V_{GS} curve and I_G–V_{GS} curve and (b) $\mathrm{sqrt}(I_D)$–V_{GS} curve.

with increasing stress time, thus resulting in the increase of the OFF-state current. In addition, Fig. 2(a) also shows the change of the gate leakage current before and after stressing under the gate-bias stress of $V_{GS} = -20$ V for 120 min. It can be observed that there is a slightly increase in the gate leakage current after stressing, and the position of the minimum gate leakage current shifts toward negative direction.

In an effort to clarify the negative gate-bias-stress behavior, the effects of gate bias and stress time on the electrical properties of the device are investigated. Figure 3 shows the time dependence of threshold-voltage shift (ΔV_{th}) under different negative gate-bias stresses at room temperature. It is evident that the time dependence of ΔV_{th} follows a logarithmic time-dependence model for each bias stress, described elsewhere as symptomatic charge-trapping instabilities.[14] Charge trapping occurs when charge carriers from the semiconductor channel are captured by electrically active traps located at or near the semiconductor/dielectric interface and throughout the dielectric via tunneling or thermionic emission. The logarithmic time-dependence is defined as[15]

$$\Delta V_{th} \approx r_0 \ln\left(1 + \frac{t}{\tau_0}\right), \quad (1)$$

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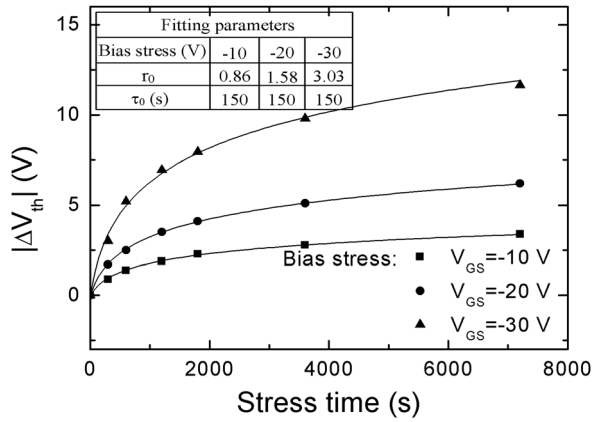

FIG. 3. Threshold-voltage shift as a function of stress time for different negative gate-bias stresses.

where r_0 is the decay rate constant; and τ_0 is the time constant of the decay.[16] This model provides a good fit to measured data, and fitting parameters are shown in Fig. 3. Therefore, the rate of the threshold-voltage shift decreases with increasing stress time because the trapped holes at the gate-dielectric/channel interface or in the dielectric can partially screen the applied electric field during the negative gate-bias stress.

Figure 4 shows the change in subthreshold slope (SS) with stress time for different gate-bias stresses. It can be seen that the subthreshold slope increases slightly (<2.5%) for various negative gate-bias stresses. The SS value is known to be influenced by the interfacial states between the gate insulator and channel layer in TFTs, and the density of trap states (N_t) at/near the interface can be calculated by[17]

$$N_t = \left[\frac{\mathrm{SS}\log(e)}{kT/q} - 1\right]\frac{C_i}{q}. \tag{2}$$

Therefore, it can be deduced that the creation of trap states at the interface in the device induced by the negative gate-bias stress is relatively slight. The subthreshold slope is relatively stable with the increase of stress time, indicating that the creation of extra defect states at the ZnO/dielectric interface and/or at the grain boundaries in the ZnO channel region is not significant, and charge trapping is the dominant instability mechanism.[18] However, any change in subthreshold slope only reflects changes of defect state in the upper part of the band gap. The only fact that the subthreshold slope is unchanged is not enough to prove that the creation of extra defect states is negligible. Figure 5 shows transfer characteristics of the ZnO TFT at drain voltage of 20 V for variable relaxation times after stressing for 120 min under the gate-bias stress of $V_{GS} = -20$ V. It can be seen from Fig. 5 that the gate-bias tress effect is recoverable, and degradation induced by the gate-bias stress is about 90% recovery after 120 min of relaxation. Therefore, the fact that the device recovers its initial state without any annealing procedure further suggests that trapped charge at the interface is the cause of device instability under the negative bias stress, because thermal annealing is usually necessary to remove any defects that may have been created during stressing.[19]

Normally, the increase of effective trap-state density results in a degradation of effective carrier mobility.[20] However, of greater interest is the apparent increase in carrier mobility with increasing stress time and stress voltage for the devices in this work as shown in Fig. 6. Here, the carrier mobility is deduced from the plot of square root of drain current (I_D) versus gate voltage (V_{GS}) in saturation region according to the following equation:

$$\mu = \frac{2LB^2}{WC_i}, \tag{3}$$

where $B = \partial(I_D)^{1/2}/\partial V_{GS}$ is the slope of the plot. For the gate bias of −30 V, the relative increase of the mobility ($\Delta\mu_s/\mu_0$) can be up to 80%. The reason is as follows: for a defective-channel TFT, part of the induced charge is trapped at defect states in the channel, the measured drift mobility (μ) could be expressed as[21]

$$\mu = \mu_n \frac{n_f}{n_i}, \tag{4}$$

where μ_n, n_i, and n_f are the band mobility, the sheet density of total induced electrons, and the sheet density of the free

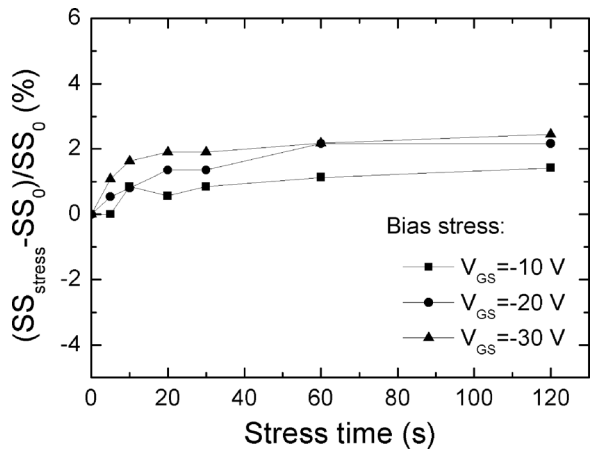

FIG. 4. Change in subthreshold slope with stress time for different negative gate-bias stresses.

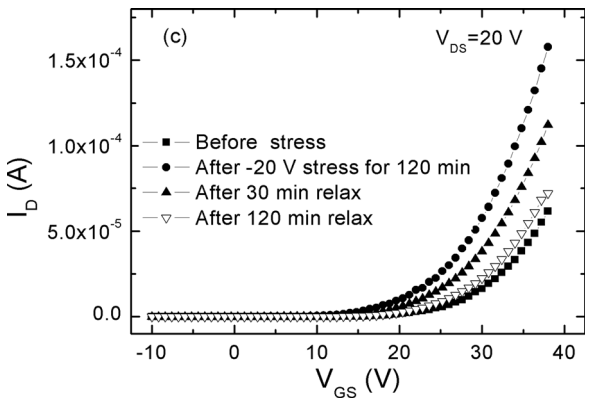

FIG. 5. Transfer characteristics of the ZnO TFT at drain voltage of 20 V for variable relaxation times after stressing for 120 min under the gate-bias stress of $V_{GS} = -20$ V.

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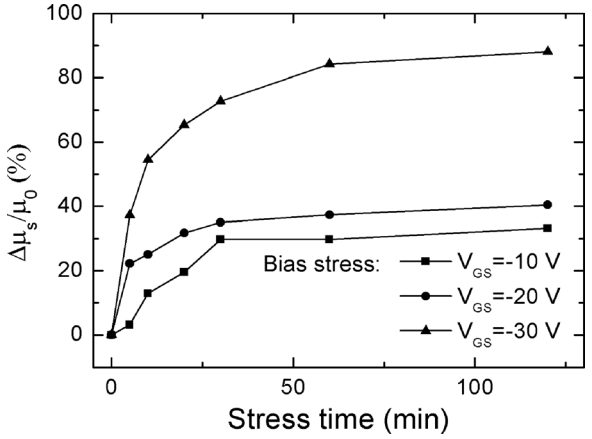

FIG. 6. Effect of stress voltage and stress time on the carrier mobility of the ZnO TFT.

electrons in the conducting channel, respectively. When new trap states generated by the negative gate-bias stress are too few to cause a clear change in mobility, the mobility is mainly determined by the ratio of n_f to n_i. During the negative gate-bias stress, the holes trapped at the gate-dielectric/channel interface or in the dielectric can induce electrons in the channel, and then these electrons can partially fill up defect states in the channel. Once occupied, these defect states will not act to trap electrons, and so the density of the free electrons will increase under same gate voltage. From Eq. (4), this would result in an increase of the mobility. Since the trapped holes increase with increasing stress time and stress voltage, the mobility also increases with stress time and stress voltage.

In order to further clarify the mechanism of the instability in the threshold voltage, the hysteresis test of transfer curve is conducted before and after stressing with different negative gate-bias stresses applied to the ZnO TFT for 120 min. The transfer curves are obtained by sweeping the gate voltage from negative to positive (forward sweeping) and then in the opposite direction (reverse sweeping) under a fixed drain voltage of 20 V, as shown in Fig. 7. For the two stress voltages of −10 and −20 V, V_{th} shifts toward a more positive voltage for the reverse sweep of the hysteresis loop before and after stressing, and the variation of V_{th} shift increases subtly after stressing, which is slightly influenced by the stress voltage. The positive shift of V_{th} could be explained as follows: negative charge carriers are trapped at the channel/gate-oxide interface or injected into the dielectric from the channel during forward sweeping,[22] thus resulting in a V_{th} shift toward positive direction for the reverse sweep. But for the stress voltage of −30 V, a clear hump in the transfer curve appears in subthreshold region after stressing only for the reverse sweeping, and the hump becomes more significant as the stress time increases. In previous works, the hump generated by positive gate-bias stress was proposed to be due to the parasitic transistor developed in the back channel by adsorbing H_2O molecule[23] or metastable oxygen vacancies induced near the semiconductor/gate-insulator interface by gate-bias stress.[24] According to the above analysis on the threshold-voltage shift and

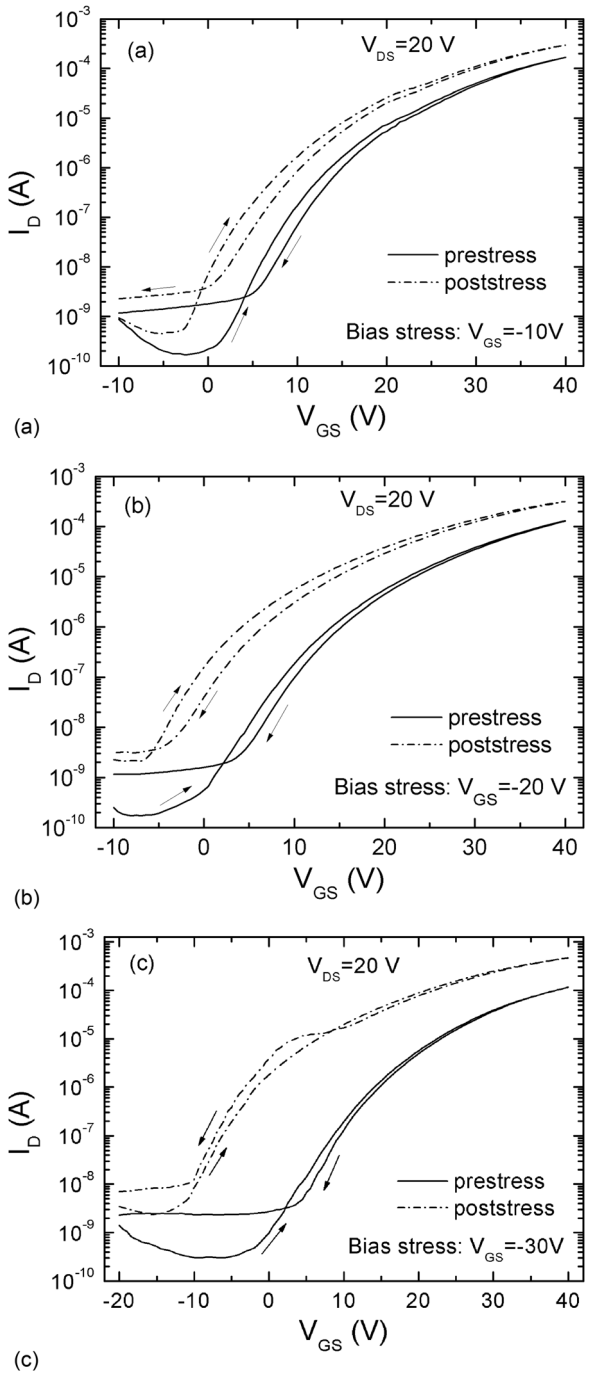

FIG. 7. Hysteresis loop of transfer curves before (full line) and after (dotted line) stressing at a fixed drain voltage of 20 V when different negative gate-bias stresses were applied to the ZnO TFT for 120 min at room temperature, (a) bias stress of $V_{GS} = -10$ V, (b) bias stress of $V_{GS} = -20$ V, and (c) bias stress of $V_{GS} = -30$ V. The arrows indicate the sweep direction of the gate bias voltage.

subthreshold slope before and after stressing, the new trap states at the channel/dielectric interface induced by the negative gate-bias stress are not significant. We have thereby determined that the hump should be due to the metastable oxygen vacancies in the channel induced by high gate-bias stress. The electrons in the channel are trapped in the metastable oxygen vacancies during forward sweeping, and then the trapped electrons emit during reverse sweeping for the

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gate voltage less than the threshold voltage, thus resulting in the hump in the transfer curve only for the reverse sweeping.

Normally, capacitance–voltage measurement is intrinsically a useful technique for investigating the charge phenomena in TFTs because measured capacitance varies with the trapped charges in the semiconductor bulk and at the insulator/semiconductor interface as well as applied gate voltage.[25,26] To further investigate the effects of negative gate-bias stress on the charge states at the gate-dielectric/ZnO interface in the ZnO TFT, Fig. 8 shows the C-V hysteresis curve of the ZnO TFT before and after different gate-bias stresses at a frequency of 500 kHz. It can be seen that the C-V curve shifts parallelly toward the negative direction after stressing, and the shift increases with the increase of negative gate bias, but the distortion of the C-V curves is not obvious (i.e., hysteresis size and direction, and the slope from accumulation to depletion are unchanged), indicating again that the negative gate-bias stress does not generate new defect states at the interface between the channel and dielectric layer, and the shift in threshold voltage after stressing should be attributed to the trapping of positive charge carriers in the defect states at the gate-dielectric/channel interface or in the dielectric. In addition, it is noted that the C-V hysteresis (negligible) is much smaller than that of the transfer characteristics. This is because negatively charged carriers in the channel are easily trapped in the defect states at the gate-dielectric/channel interface when a fixed drain voltage ($V_{DS} = 20$ V) and gate-sweep voltage ($V_{GS} = -10$ to 40 V) are applied to the device during the forward sweep of the transfer curve shown in Fig. 6, thus leading to a larger hysteresis.[27]

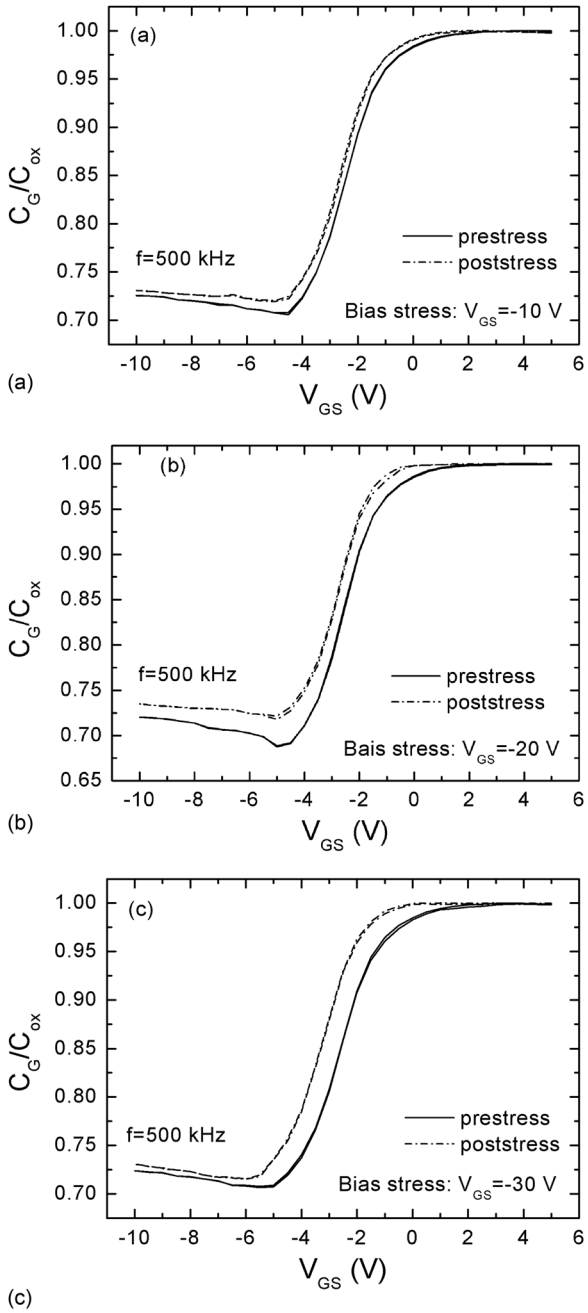

FIG. 8. C-V hysteresis curves of the ZnO TFT before (full line) and after (dotted line) stressing under different gate bias stresses for the test frequency of 500 kHz. (a) bias stress of $V_{GS} = -10$ V, (b) bias stress of $V_{GS} = -20$ V, and (c) bias stress of $V_{GS} = -30$ V.

IV. SUMMARY AND CONCLUSIONS

The electrical instability of ZnO TFT under negative gate-bias stress has been investigated as a function of stress time and stress voltage. Experimental results show that with the increase of stress voltage or stress time, the carrier mobility and OFF-state current of the TFT increase. Moreover, its threshold voltage shifts toward the negative direction, but the change of subthreshold slope is not significant. The time dependence of threshold-voltage shift on various bias stress conditions could be described by a logarithmic equation. Based on the analysis of hysteresis behaviors in current–voltage and capacitance–voltage characteristics before and after the gate-bias stress, it can be clarified that the threshold-voltage shift is predominantly attributed to the trapping of positive charge carriers in the defect states at the gate-dielectric/channel interface or in the dielectric.

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