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Nb-Doped La$_2$O$_3$ as Charge-Trapping Layer for Nonvolatile Memory Applications

Runru Shi, X. D. Huang, Member, IEEE, C. H. Leung, Johnny K. O. Sin, Fellow, IEEE, and P. T. Lai, Senior Member, IEEE

Abstract—Charge-trapping properties of Nb-doped La$_2$O$_3$ (LaNbO) are investigated using an Al/Al$_2$O$_3$/LaNbO/SiO$_2$/Si structure. Compared with the memory device with La$_2$O$_3$, the one with LaNbO shows better charge-trapping characteristics, including larger memory window (6.0 V at ±16 V sweeping voltage), higher programming speed (9.1 V at ±16 V for 1 ms), and better retention property (94% charge retained after 10$^8$ s at 120 °C), due to its higher trapping efficiency resulted from increased trap density and suppressed formation of a silicate interlayer at the LaNbO/SiO$_2$ interface by the Nb doping. Therefore, LaNbO is a promising candidate as the charge-trapping layer for nonvolatile memory applications.

Index Terms—Nonvolatile memory, charge-trapping, Nb-doped La$_2$O$_3$ (LaNbO), high-k dielectric.

I. INTRODUCTION

Metal-oxide-nitride-oxide-silicon (MONOS)-type flash memories with discrete traps in the nitride dielectric as charge-trapping medium show stronger scaling ability and higher reliability than the floating-gate type memories. Si$_3$N$_4$ is the first dielectric as charge-trapping material for MONOS devices. However, the small conduction-band offset relative to SiO$_2$ dielectric as charge-trapping material for MONOS devices. However, the small conduction-band offset relative to SiO$_2$ dielectric, thus consuming some of the SiO$_2$ TL [5], [6]. The absence of SiO$_2$ consumption in the LaNbO sample indicates that Nb doping suppresses La oxide’s scavenging behavior towards SiO$_2$ and thus helps to maintain the desired TL. It should be noted that although an interlayer could be formed at the Al/Al$_2$O$_3$ interface, it should have the same influence on the properties of both samples.

Fig. 2 shows the SIMS depth profile of the two samples after going through all the processing steps. In Fig. 2(a), the La content displays two local peaks and one of them overlaps with the peak of SiO$_2$, suggesting that La diffuses into the TL. In Fig. 2(b), La and Nb display only one peak farther away from the TL, indicating the suppression

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of La$_2$O$_3$ diffusion by the Nb doping. The quality of the interface between the CTL and TL is improved by the Nb doping, because the suppression of La$_2$O$_3$ diffusion protects the interface from the formation of poor-quality silicate interlayer, which is consistent with the TEM results in Fig. 1.

Fig. 3 shows the 1-MHz hysteresis characteristics of the MONOS capacitors under various sweeping voltages. The equivalent oxide thickness (EOT) of the two samples is calculated by:

$$EOT = T \left( \frac{\varepsilon_{SiO_2}}{K} \right)$$

where $T$ is the total physical thickness of the TL, CTL and BL; $\varepsilon_{SiO_2}$ is the dielectric constant of SiO$_2$; and $K$ is the equivalent dielectric constant of the TL, CTL and BL calculated from the measured capacitance of the samples. Sweep starts from inversion region to accumulation region, and back to inversion region again. For the LaNbO sample, as the sweeping voltage increases from ±8 V to ±16 V, the memory window increases from 2.5 V to 6.0 V. On the contrary, the memory window of the LaO sample is only 0.8 V at ±8 V sweeping voltage, which is much smaller than that of the LaNbO one. The much larger memory window of the LaNbO sample indicates that niobium doping increases the trap density of the charge trapping layer (CTL), thus increasing its charge-trapping efficiency. Moreover, the LaNbO sample can endure higher voltage up to ±16 V, while the LaO sample breaks down at 12 V as shown in Fig. 3 mainly due to the thinner SiO$_2$ TL and the silicate interlayer of low quality in the LaO sample (shown in Fig. 1). Another phenomenon worth mentioning is that the initial $V_{FB}$ of both samples increases with increasing sweeping voltage. It is due to electron injection from the gate to the CTL in the accumulation region, which is consistent with the results in Fig. 4 and will be explained in detail later.

Fig. 4 shows the program/erase (P/E) characteristics of the MONOS capacitors. The LaNbO sample always displays much larger $V_{FB}$ shift than the LaO one under the same operating conditions. It is worth emphasizing that the $V_{FB}$ shift of the LaNbO sample is larger even when the sample has thicker TL (shown in Fig. 1), which results in longer distance for charges to tunnel from the substrate through the TL to the CTL. The reason for the larger $V_{FB}$ shift is that the LaNbO sample has higher charge trap density, which is consistent with the conclusion drawn from Fig. 3. The higher trap density in the LaNbO sample can accommodate more charges, leading to larger $V_{FB}$ shift. In addition, the $V_{FB}$ shift of the LaO device hardly increases with increasing positive gate voltage, while that of the LaNbO one does not have the saturation phenomenon and increases significantly with the gate voltage. This phenomenon further confirms the high trap density of the LaNbO sample, indicating that Nb incorporation in La$_2$O$_3$ helps overcome the trap deficiency problem of the La oxide. The charge-trap density ($N_t$) can be estimated by assuming that the trapped-charge centroid is located at the center of the CTL [8], [9]:

$$N_t = \frac{\Delta V_{FB}}{q} \left( \frac{T_{BL}}{\varepsilon_{BL}} + \frac{T_{CT}}{2\varepsilon_{CT}} \right)^{-1}$$
suggesting that thermionic emission plays an insignificant role in the LaNbO sample, retention is hardly dependent on testing temperatures, back to its original value.

where $\Delta V_{FB}$ is the $V_{FB}$ shift with respect to the fresh $V_{FB}$, $q$ the elementary charge, $\varepsilon_0$ the permittivity of vacuum, $T_{BL}$ and $\varepsilon_{BL}$ the thickness and dielectric constant of the BL respectively, $T_{CT}$ and $\varepsilon_{CT}$ the thickness and dielectric constant of the CTL respectively. $N_2$ of the LaNbO sample under $\pm 12$ V sweeping is calculated to be $1.91 \times 10^{13}$ cm$^{-2}$, which is much higher than the value $(3.56 \times 10^{12}$ cm$^{-2}$) for the LaO sample. Furthermore, by erasing at $-16$ V for 1 ms, the LaNbO sample has a $V_{FB}$ shift of $-4.1$ V, while the LaO one has a positive shift of 3.3 V and shows normal erasing behavior only at $-8$ V with a small shift of $-0.1$ V. This abnormal positive $V_{FB}$ shift of the LaO sample is the result of undesirable electron tunneling from the gate to the CTL, which is called erase saturation [10]. It indicates a nonideal CTL/BL interface, which is an important problem to be solved in enhancing the erasing function of memory devices [11], [12]. For comparison, the abnormal positive shift does not exist in the LaNbO sample due to high trap density. The moving electrons during erasing can be divided into two parts: some escape from the CTL through the TL to the substrate, while others flow into the CTL from the gate electrode. For the LaNbO sample with a large number of traps in the CTL, the former outnumbers the latter so that the erase saturation is partially overcome. The overall dynamic equilibrium is a normal erasing behavior with a negative $V_{FB}$ shift. Besides the trap density, the quality of the CTL/BL interface also affects the electron flow from the gate to the CTL. The Nb doping can improve the quality of CTL/BL interface and therefore suppress the undesirable electron flow. Additionally, the electrons injected from the gate to the CTL are of CTL/BL interface and therefore suppress the undesirable electron flow from the gate to the CTL. The Nb doping can improve the quality of the interlayer-free TL with fewer defects. The charge-trapping properties of LaO sample are investigated based on MONOS capacitor. The memory device with Nb-doped La$_2$O$_3$ as CTL shows better characteristics than that with La$_2$O$_3$ in terms of memory window, P/E speed, endurance and data retention, which are resulted from higher trap density in CTL and better TL/CTL interface (both induced by the Nb doping). Therefore, Nb-doped La$_2$O$_3$ is a promising candidate as CTL for high-performance nonvolatile memory applications.

Fig. 5 shows the retention characteristics of the LaO and LaNbO samples at room temperature, 85 °C and 120 °C.

IV. CONCLUSION

The charge-trapping properties of La$_2$O$_3$ with and without Nb doping have been investigated based on MONOS capacitor. The memory device with Nb-doped La$_2$O$_3$ as CTL shows better characteristics than that with La$_2$O$_3$ in terms of memory window, P/E speed, endurance and data retention, which are resulted from higher trap density in CTL and better TL/CTL interface (both induced by the Nb doping). Therefore, Nb-doped La$_2$O$_3$ is a promising candidate as CTL for high-performance nonvolatile memory applications.
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