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Resonant Augmentation Circuits for a Buck Converter Achieving Minimum-Time Voltage Recovery from Load Transients

Zhenyu Shan*, Siew-Chong Tan†, Chi K. Tse‡ and Juri Jatskevich*

*Department of Electrical and Computer Engineering, The University of British Columbia, Vancouver, BC, Canada
†Department of Electrical and Electronic Engineering, The University of Hong Kong, Pokfulam, Hong Kong
‡Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Kowloon, Hong Kong

Email: zhenyus@ece.ubc.ca

Abstract—This paper presents the use of a resonant circuit for fast voltage recovery of power supplies under large-signal load transients. Previous works have shown that an augmentation circuit (or auxiliary circuit) for voltage recovery may be used to improve the dynamic response, while the main converter is operating for current recovery with load current feedforward control. A compact, low cost and magnetic-coreless topology with a simple control algorithm to achieve an augmentation circuit is presented. In the prototype, the inductors are realized using printed copper wires. The control algorithm is realized by a low cost and low density logic device. Simulation and experimental results validate the feasibility and effectiveness of the circuit.

I. INTRODUCTION

Low voltage digital intelligent ICs, e.g., digital signal processors or microprocessors, are widely used in industrial and consumer electronics. To feed high-speed digital electronics loads, high performance power supplies are needed. The power converter needs to track high-slew-rate and large-step load transients to limit voltage deviations within a narrow tolerance band [1]–[3]. The physical limit to the transient response of a traditional buck converter is the internal slew rate of the inductor.

While the time-optimal control scheme can push the dynamic performance to its physical limit [4], augmentation circuits [5]–[9] (or auxiliary circuits [10]–[17]) for dc–dc converters have been proposed to break the limit and achieve minimum-time recovery under fast-load-transient conditions. In Fig. 1, the augmentation circuits provide the short-fall charges of the filter capacitor \( C_o \) while the main converter inductor current is recovering. Therefore, the response of such an augmented converter is better than that of a fixed-topology converter which uses a time-optimal control algorithm.

To reduce the converter complexity and the extra space needed, the augmentation circuits and its control stage should be as simple and small as possible. Additionally, the trend of power technology development is moving towards integrating the high performance microprocessor together with its power supplies on the same wafer [18]. However, it is still a challenge to implement the augmentation circuits as an IC chip. The reasons are two folds.

First, the inductor may be operating in non-resonant mode to regulate the augmentation current. In this circumstance, the inductance value is in hundreds of nH, which is too large for IC implementation. Second, some methods use switches with diverse resistance to achieve current regulation. To enlarge the current regulation range, the number of switches and the space occupied by the circuit will be large, which also hinders IC implementations.

A set of resonant auxiliary circuits serving as augmentation branches to achieve minimum-time recovery of a converter is proposed in this paper. The circuit operating in resonant mode with an event driving control algorithm generates unified quasi-sinusoidal pulses. Comparing with previous methods [5]–[17], advantages of the proposed approach are as follows:

- The circuit generates unified discontinuous pulses so that the controller is easy to design and realize.
- The quasi-sinusoidal current generated by a resonant circuit has lower \( di/dt \) than the sharp-edge current generated by a pure-resistive current path.
- Small capacitors (\( \mu \)F) and inductors (tens of nH, achieved by stray inductance) are used such that the circuit power stage will occupy a smaller space.
The proposed method takes advantage of a resonant circuit and gives a paradigm shift in the implementation of augmented converter, catered for the power-supplies-on-chip trend. In this work, the small inductors are realized by coreless printed spiral windings (CPSW).

II. RESONANT AUXILIARY CIRCUIT

A. Overview of Topology and Realization

The two basic cells of the proposed auxiliary circuit shown in Fig. 2 function as the two augmentation branches. “Cell A” operates as the high-side branch to mitigate the positive transient; “Cell B” operates as the low-side branch to mitigate the negative transient. Each cell is comprised of three components: two switches $S_{ao}$ and $S_{ai}$ and a capacitor $C_o$. Additionally, two inductors $L_{ai}$ and $L_{ao}$ are realized using the distributed inductance of wires on a printed circuit board (PCB) or a silicon wafer. In this analysis, the resistance of all conducting components are represented by $R_t$ and $R_o$. The input voltage source $V_i$ and output capacitor $C_o$ of the main converter are shown in Figs. 2(a) and (b), while other elements of the main converter are not shown to avoid cluttering figures. Since capacitance $C_o$ is much bigger than $C_a$, the output voltage $V_o$ of the converter is assumed to be constant when the proposed cells are active.

The energy transfer between the cell and $C_o$ is achieved in two phases, i.e., $T_1$ (charging phase) and $T_2$ (discharging phase). The normalized waveforms of the two cells are shown in Fig. 2(c). During $T_1$, $S_{ai}$ is on and $C_a$ is charged by a full cycle damped sinusoidal current $i_{ai}$. At the end of $T_1$, $v_{Ca}$ rises to $V_{Ca1}$ which is slightly under $V_i$. During $T_2$, $S_{ao}$ is on and $C_a$ is discharged, generating a half cycle quasi-sinusoidal current $i_{ao}$. In Cell A, $i_{ao}$ is flowing into $C_o$; in Cell B, $i_{ao}$ is flowing out of $C_o$. The levels of $V_{Ca2}$ in Cell A and Cell B are slightly under $V_o$ and $V_i - V_o$, respectively.

B. Energy Pulses

During $T_2$, the precise $i_{ao}$ can be expressed as

$$i_{ao} = \frac{e^{-\alpha t}}{L_{ao} \omega_d} V_d \sin \omega_d t \quad (0 \leq t \leq \pi/\omega_d)$$

(1)

where $\alpha = \frac{R_o}{2L_{ao}}$, $\omega_d = \sqrt{\omega_o^2 - \alpha^2}$, $\omega_o = 1/\sqrt{L_{ao} C_o}$ and $V_d = V_{ca1} - V_o$ in Cell A or $V_d = V_i - V_{ca1} + V_o$ in Cell B. When

$$C_o \ll \frac{4L_{ao}}{R_o^2}$$

(2)

is satisfied, it can be assumed that $\omega_d \approx \omega_o = 1/\sqrt{L_{ao} C_o}$, and $T_2 \approx \pi/\omega_o C_o$. The average value of $i_{ao}$ is derived and given as (3). $V_i$ can be approximated as either $V_i - V_o$ in Cell A or $V_o$ in Cell B, as $V_{ca1} \approx V_i$. If $R_o$ is sufficiently small, $I_{aovg}$ can be further simplified as

$$I_{aovg} \approx \frac{2}{\pi} \sqrt{\frac{C_o}{L_{ao}}} (V_i - V_o).$$

(4)

Similarly, the approximate $I_{bavg}$ value of Cell B can be derived as

$$I_{bavg} \approx \frac{2}{\pi} \sqrt{\frac{C_o}{L_{ao}}} V_o.$$  

(5)

C. Determination of Parameters of Auxiliary Circuits

According to above analysis, the parameters $L_{ao}$ and $C_o$, determine the $I_{aovg}$ value and other properties of the energy pulses. The amount of transferred electrical charge per pulse is constrained by the voltage tolerance, and the duration of the pulses is constrained by switching frequency at which the components can operate. Therefore, the values of $L_{ao}$ and $C_o$ depend on all the factors mentioned above.

1) $\Delta V_{o,max}$ Determines $C_o$. The load will change with variable-size steps, while the auxiliary circuit generates fixed-amplitude pulses. When the load transient is relatively small, the pulses from the auxiliary circuit may introduce extra voltage ripples on $V_o$. Therefore, the amount of transferred charge per pulse (denoted as $Q_{aov}$) must be limited by the tolerance of $V_o$ deviations (assumed to be $\Delta V_{o,max}$), and is given as

$$\Delta V_o = Q_{aov}/C_o = I_{aovg} T_2/C_o \leq \Delta V_{o,max}. $$

(6)

$$I_{aovg} = \frac{1}{T_2} \int_{0}^{T_2} i_{ao} dt \approx \frac{1}{\pi \sqrt{L_{ao} C_o}} \int_{0}^{\pi \sqrt{L_{ao} C_o}} e^{-\alpha t} \sqrt{C_o/4L_{ao}} V_d \sin \frac{t}{\sqrt{L_{ao} C_o}} dt \approx \frac{1 + e^{-\alpha \pi \sqrt{L_{ao} C_o}}}{\pi \sqrt{R_o} \sqrt{L_{ao} C_o}} C_o V_d \sqrt{L_{ao} V_d}

(3)$$
where \( V_o \) is assumed to be relatively constant and much larger than \( \Delta v_o \). After substituting \( I_{aavg} \) by the result of (4) and (5), the derived constraints on \( C_o \) for Cell A is
\[
C_o \leq \frac{\Delta V_{o\text{max}}C_o}{2(V_i - V_o)}
\]
and for Cell B is
\[
C_o \leq \Delta V_{o\text{max}}C_o.
\]

2) \( \Delta I_{o\text{max}} \) Determines \( \frac{2V_o}{I_{aavg}} \): To achieve a voltage-deviation-free response to load transients, the current provided by the auxiliary circuit should make up the mismatch between the inductor and the load current \( [6] \). The value of \( I_{aavg} \) should be determined by the maximum load transient (assumed to be \( \Delta I_{o\text{max}} \)). The limit on inductance \( L_{a} \) can be derived from
\[
I_{aavg} \geq k_{aoo} \Delta I_{o\text{max}},
\]
where \( k_{aoo} \) is the scaling factor to cope with the error existing in the estimated value of \( I_{aavg} \). The factor of
\[
M_s = \frac{1 + e^{-\frac{2\pi}{\Delta I_{o\text{max}}}}}{{\pi [1 + R_o^2 C_a/(4L_{a})]}}
\]
in (3) is approximated as \( 2/\pi \) in (4) and (5). In a circuit with a set of general parameters, \( R_o = 0.2 \Omega, C_a = 2 \mu F \) and \( L_{a} = 30 \) nH, the \( M_s \) value drops to 0.6/\( \pi \) which is one-third of \( 2/\pi \). As a result, the values of \( I_{aavg} \) obtained from (4) and (5) are overestimated. A reasonable \( k_{aoo} \) should be in the range from 2 to 4 to compensate the overestimation of \( I_{aavg} \). Finally, the constraints on \( L_{a} \) in Cell A and Cell B are
\[
L_{a} = C_a \left[ \frac{2(V_i - V_o)}{k_{aoo} \Delta I_{o\text{max}} \pi} \right]^2
\]
and
\[
L_{a} = C_a \left[ \frac{2V_o}{k_{aoo} \Delta I_{o\text{max}} \pi} \right]^2,
\]
respectively.

3) \( R_o, R_i \) and \( L_i \) Effects: In the above guidelines, \( R_o \) is not considered. However, the presence of \( R_o \) causes errors in (4) or (5) such that the actual \( I_{aavg} \) is lower than its calculated value. The \( I_{aavg} \) value should be verified using (3) with the estimated \( R_o \). Normally, \( R_o \) of around 100 m\( \Omega \) is reasonable. The existence of \( R_i \) and \( L_i \) will limit the magnitude and the slew rate of \( i_s \). Values of a few m\( \Omega \) for \( R_i \) and a few nH for \( L_i \) are suitable for most applications where \( C_o \) is around 1 \mu F. Particularly, the stray inductance from the connection lines among the elements and the power may achieve a satisfied \( L_i \). In summary, the constraints on \( R_i, R_o \) and \( L_i \) are not strict, but should be considered.

4) Duration of \( T_1 \) and \( T_2 \): In both cells, the precise duration of \( T_1 \) and \( T_2 \) can be calculated by
\[
T_1 = \frac{2\pi}{\sqrt{1/(L_i C_a) - R_i^2/(4L_i^2)}},
\]
and
\[
T_2 = \frac{\pi}{\sqrt{1/(L_i C_a) - R_i^2/(4L_i^2)}},
\]
respectively. The values of \( T_{1/2} \) are expected to range within the component-switching-time limits. The chosen parameters should be substituted into (11) and (12) to ensure that the switches are capable of achieving the designed switching speed.

### III. CONTROL SCHEME FOR AUGMENTED CONVERTER

Taking advantage of the load feedforward control method, the control loop of main converter and augmentation circuits are simplified for design. The main converter achieves the minimum-time recovery of its inductor current, while the augmentation circuit is facilitating the voltage recovery. As a result, the augmented converter recovers from its load transient in a minimum time.

#### A. Review of Load Feedforward Control for Main Converter

Peak current with load feedforward control applied to converter with an augmentation scheme has been proposed by Kapat and Krein [5], [6]. This strategy is capable to make the inductor current recover to its steady state from large load transients in minimum time. The load current \( i_L \) feedforward is functioning as the dominant component of the peak current reference. The peak current of \( i_L \) will refer to
\[
i_p = i_o + k_i (V_{ref} - V_o) + k_i \int (V_{ref} - V_o)dt.
\]

#### B. Event Driving Control of Augmentation Circuits

The voltage recovery of the system will be achieved by the augmentation that is controlled by a fast non-linear loop, e.g., bang-bang control [5], [6]. Thus, an event driving method is developed for the control of the proposed auxiliary circuit. There is only one threshold to start the circuit actions. Cell A in Fig. 2(a) and the diagram in Fig. 3, for instance, illustrate the approach. The circuit will be standing by unless \( v_o \) is lower than a fixed threshold \( V_{thl} \). When the circuit enters the \( P_2 \) state, it will stay there with the switch \( S_{ao} \) on until a pre-set time period \( T_2 \) has elapsed. Then, the circuit will shift to the \( P_1 \) state with the switch \( S_{ai} \) on and remain as it is until the time period \( T_1 \) has elapsed. The control of Cell B is the same as that of Cell A except for the event (\( v_o \) becoming higher than \( V_{thh} \)) to drive the state turning to \( P_2 \) from a stand-by state.
IV. SIMULATION AND EXPERIMENTS

The simulation and experimental measurements based on a traditional sync-buck converter are performed to verify the proposed method. The parameters of the main converter are $V_i = 12 \text{ V}$, $V_o = 5 \text{ V}$, $f_{sw} = 200 \text{ kHz}$, $L = 10 \mu\text{H}$ and $C_o = 280 \mu\text{F}$. The auxiliary circuit is designed for 5 A load transients. Parameters of Cell A are $L_{ao} \approx 50 \text{ nH}$, $L_{ai} \approx 5 \text{ nH}$ and $C_a = 0.8 \mu\text{F}$, and that of Cell B are $L_{ao} \approx 40 \text{ nH}$, $L_{ai} \approx 5 \text{ nH}$ and $C_a = 1 \mu\text{F}$. Other common parameters of the two cells are $k_{iao} = 3.5$, $\Delta V_{o,\text{max}} = 0.05 \text{ V}$, $V_{thl} = 4.97 \text{ V}$, $V_{thh} = 5.03 \text{ V}$, $R_i \approx 50 \text{ m}\Omega$ and $R_o \approx 160 \text{ m}\Omega$.

A. Simulation Results

The simulation is implemented in Matlab/Simulink. The key waveforms in a large time scale are given in Fig. 4. In both cases (with and without the augmentation) the load feedforward control is applied and the inductor current recovers from large load transients in the minimum time. By using the proposed circuit, the voltage recovery time has been shortened from 100 $\mu$s to 10 $\mu$s which is approaching the current recovery time. Also the voltage overshoots or dips have been reduced from 90 mV to 30 mV, which is significant.

The enlarged waveforms of the output current and capacitor voltage of the two cells are shown in Fig. 5. In discharging phase $T_2$, one quasi-sinusoidal current pulse is generated by the capacitor $C_a$ discharging through the inductor $i_{ao}$. In charging phase $T_1$, $v_{Ca}$ rises back to the initial level approaching $V_i$. The circuit operation is repeated cycle by cycle providing the required transient energy.

B. Prototype and Experimental Results

The schematic diagram of the prototype is shown in Fig. 6. The main converter is a general sync-buck converter. Two auxiliary circuits configured as Cell A and Cell B operate
respectively as “AugHigh” and “AugLo” shown in Fig. 1. The components comprising Cell A are denoted as $L_{aiA}$, $L_{aoA}$, $C_{aA}$, $T_{aiA}$ and $T_{aoA}$ and the components comprising Cell B are denoted as $L_{aiB}$, $L_{aoB}$, $C_{aB}$, $T_{aiB}$ and $T_{aoB}$.

The inductor $L_{aoA/B}$ is implemented by a CPSW as shown in Fig. 7. To reduce the parasitic resistance, the windings printed on four copper layers are paralleled. The space ratio of the central hollow and the winding has been optimized according to the principle given in [19]. The control loop of the main converter is achieved purely by analog circuits. The proposed event driving control algorithm for the augmented circuits is achieved by a low cost complex programmable logic device (EPM240T100C5) plus analog comparators.

Figs. 8 and 9 are the experimental waveforms obtained from the prototype. As it can be seen in these figures, the proposed approach successfully achieves minimum time recovery and suppresses voltage deviations under fast load transients. Some high frequency ripples on $v_o$ are observed from the waveforms when the augmentation circuits are operating. This problem can be improved by tuning the switching dead time or adding a small capacitor at the connection line between the augmentation and the filter capacitor bank.

V. CONCLUSION

This work describes the design of a new circuit to achieve minimum-time recovery from fast load dynamics in the framework of an augmented converter. The compact resonant cells that generate fixed-width current pulses are used to handle the voltage recovery. An event driving strategy is developed to control such cells. The experimental results confirm the effectiveness of the proposed methodology. It is further envisioned that the proposed approach may lead to a paradigm shift that the augmentation method based on small inductors are designed together with the main converter on chip.
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